

In the final step of the wafer fabrication the entire surface is passivated (overglass layer, not shown here) to protect the surface from contaminants and scratches. Then openings are etched to the bond pads to allow for wire bonding. Of course, this requires another lithographic mask which is not shown in the Figure.

The composite layout and the resulting cross-sectional view, and the electrical diagram of the CMOS inverter implemented in the n-well technology described above are shown in Fig. 5-12. Note that in this particular drawing as in the previous drawings connections between the GND line and the substrate of n-channel transistors are not shown. In the actual circuit such connections exist and are created in the form of a contact similar to the contact between the V_{DD} line and the n-well, shown in Fig. 5-12 (b), or as a separate contact common for several different cells.

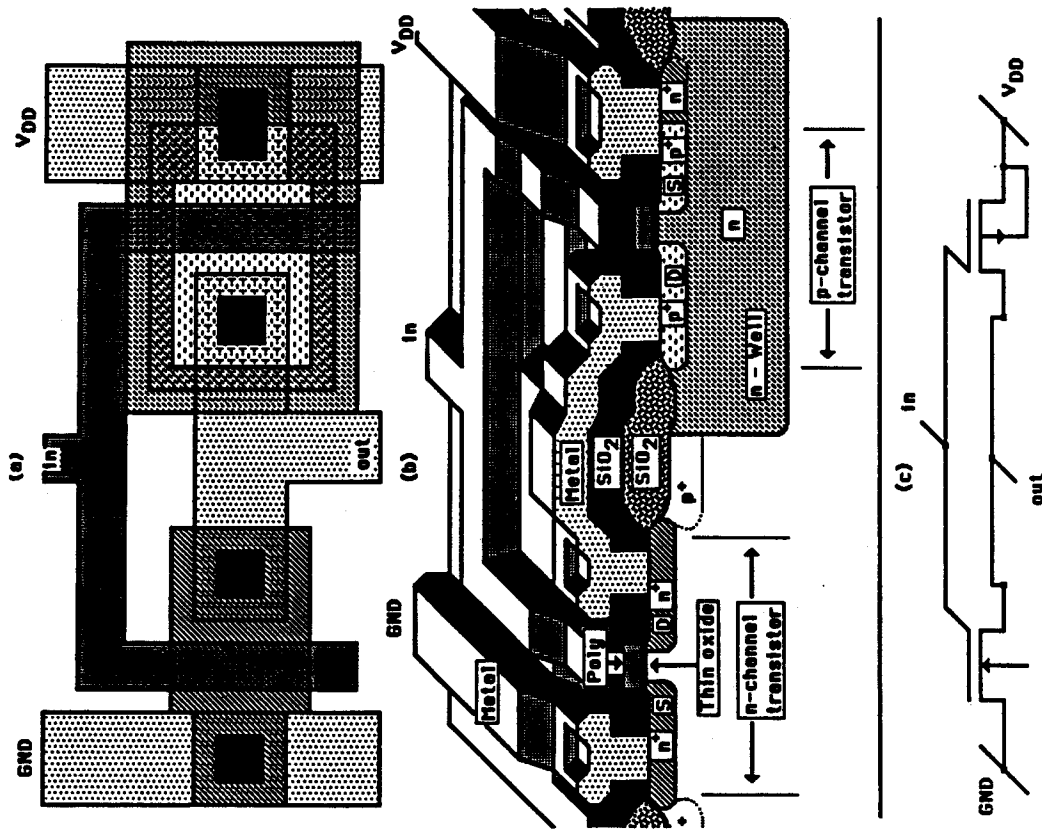


Figure 5-12: CMOS inverter. Composite layout (a), cross-section (b), and electrical diagram (c).