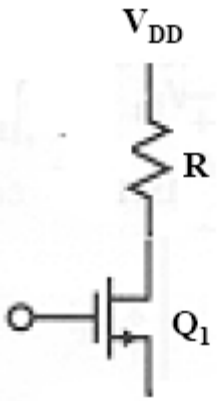
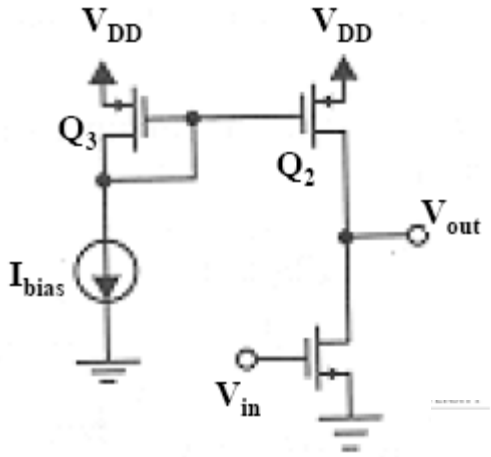
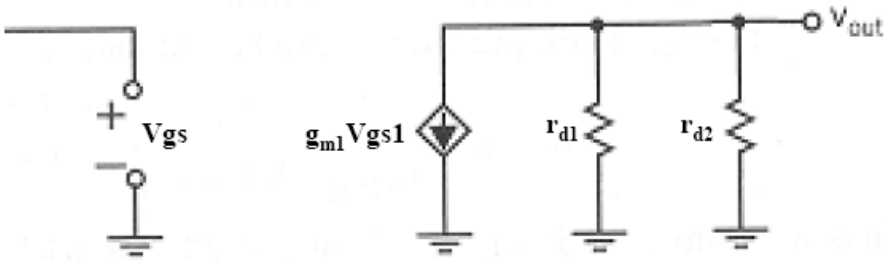
Common source amplifier





Gain= $- g_m R$

Small-signal equivalent circuit



Gain= $- g_{m1} (r_{d1} // r_{d2})$

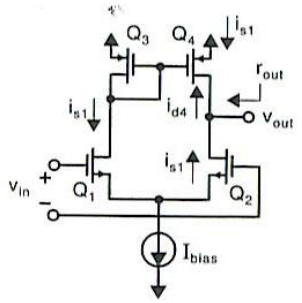


Fig. 3.19 A differential-input, single-ended-output MOS gain stage.

Note that a positive small-signal current is defined as the current going into the drain of a transistor. Using (3.60) and the fact that $i_{d2} = -i_{s1}$, we have

$$v_{out} = (-i_{d2} - i_{d4})r_{out} = 2i_{s1}r_{out} = g_{m1}r_{out}v_{in} \tag{3.61}$$

This result assumes that the output impedance is purely resistive. If there is also a capacitive load, C_L, then the gain is given by

$$A_v = \frac{v_{out}}{v_{in}} = g_{m1}z_{out} \tag{3.62}$$

where $z_{out} = r_{out} \parallel 1/(sC_L)$. Thus, for this differential stage, the very simple model shown in Fig. 3.20 is commonly used. This model implicitly assumes that the time constant at the output node is much larger than the time constant due to the parasitic capacitance at the node at the sources of Q_1 and Q_2. This assumption is usually justified, because the impedance at the output node, r_{out}, is much larger than the impedance at the Q_1, Q_2 source node (i.e., $1/g_{m1} \parallel 1/g_{m2}$). Also, the capacitance at the output node, C_L, is usually larger than the parasitic capacitance at the Q_1, Q_2 source node. However, when high-frequency effects are important (which may be the case when compensating an opamp to guarantee stability), then this assumption may not be justified.

The evaluation of the output resistance, r_{out}, is determined by using the small-signal equivalent circuit and applying a voltage to the output node, as seen in Fig. 3.21. Note that the T model was used for both Q_1 and Q_2, whereas Q_3 was replaced by an equivalent resistance (since it is diode-connected), and the hybrid-π model was used for Q_4.

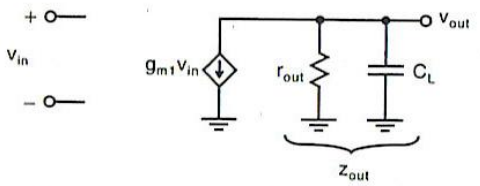


Fig. 3.20 A small-signal model for the differential-input amplifier.

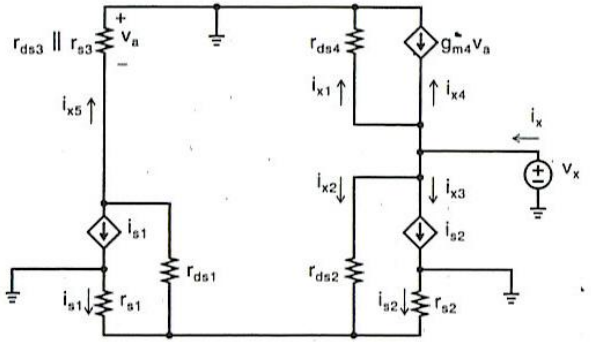


Fig. 3.21 The small-signal model for the calculation of the output impedance of the differential-input, single-ended-output MOS gain stage.

As usual, r_{out} is defined as the ratio v_x/i_x, where i_x is given by the sum $i_x = i_{x1} + i_{x2} + i_{x3} + i_{x4}$. Clearly,

$$i_{x1} = \frac{v_x}{r_{ds4}} \tag{3.63}$$

implying that the resistance seen in the path taken by i_{x1} is equal to r_{ds4}. Now, assuming that the effect of r_{ds1} can be ignored (since it is much larger than r_{s1}), we see that the current i_{x2} is given by

$$i_{x2} \cong \frac{v_x}{r_{ds2} + (r_{s1} \parallel r_{s2})} \cong \frac{v_x}{r_{ds2}} \tag{3.64}$$

where the second approximation is valid, since r_{ds2} is typically much greater than $r_{s1} \parallel r_{s2}$. This i_{x2} current splits equally between i_{s1} and i_{s2} (assuming $r_{s1} = r_{s2}$ and once again ignoring r_{ds1}), resulting in

$$i_{s1} = i_{s2} = \frac{-v_x}{2r_{ds2}} \tag{3.65}$$

However, since the current mirror realized by Q_3 and Q_4 results in $i_{x4} = i_{x5}$ (assuming $g_{m4} = 1/r_{s4} = 1/r_{s3}$ and r_{ds3} is much larger than r_{s3}), the current i_{x4} is given by

$$i_{x4} = -i_{s1} = -i_{s2} = -i_{x3} \tag{3.66}$$

In other words, when the current splits equally between r_{s1} and r_{s2}, the current mirror of Q_3 and Q_4 causes the two currents i_{x3} and i_{x4} to cancel each other. Finally, the output resistance, r_{out}, is given by

$$r_{out} = \frac{v_x}{i_{x1} + i_{x2} + i_{x3} + i_{x4}} = \frac{v_x}{(v_x/r_{ds4}) + (v_x/r_{ds2})} \tag{3.67}$$

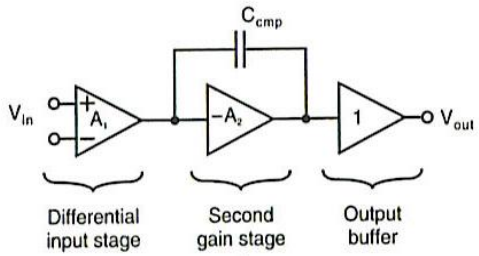


Fig. 5.1 A block diagram of a two-stage opamp.

when the opamp is used with feedback. Because C_C is between the input and the output of the high-gain second stage, it is often called a Miller capacitance since its effective capacitive load on the first stage is larger than its physical value.

An example of a practical CMOS version of the two-stage opamp is shown in Fig. 5.2. This example is used to illustrate many of the important design principles when realizing the two-stage amplifier.

It should be noted that the first stage has a p-channel differential input pair with an n-channel current-mirror active load. This is a complementary differential gain stage to that shown previously in Fig. 3.19. The trade-offs between having p-channel input transistors versus this stage and the alternative stage of Fig. 3.19 will be discussed later in this section. Also, the numbers next to the transistors represent reasonable transistor widths for a 1-μm process. Reasonable sizes for the lengths of the transistor might be somewhere between 1.5 and 2 times the minimum transistor length

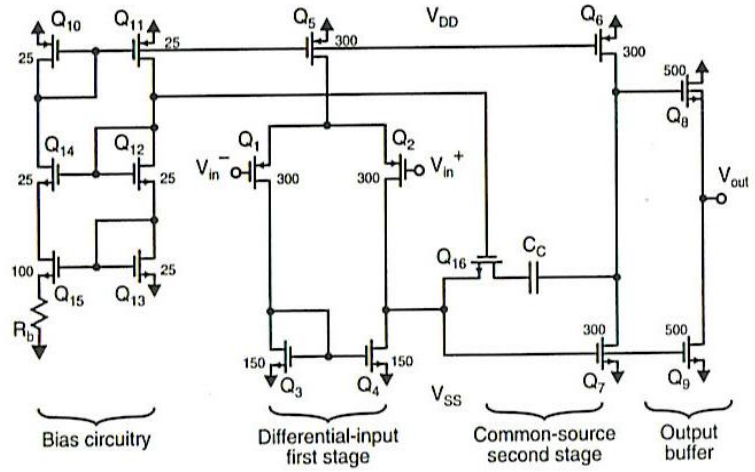


Fig. 5.2 A CMOS realization of a two-stage amplifier. All transistor lengths are 1.6 μm.

of a particular technology, whereas digital logic typically makes use of the minimum transistor length.

Opamp Gain

First we discuss the overall gain of the opamp. For low-frequency applications, this gain is one of the most critical parameters of an opamp.

The gain of the first stage has already been derived, resulting in (3.70), and is repeated here for convenience:

$$A_{v1} = g_{m1}(r_{ds2} \parallel r_{ds4}) \tag{5.1}$$

Recall from Chapter 1 that g_{m1} is given by

$$g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \frac{I_{bias}}{2}} \tag{5.2}$$

Also, an approximation to the finite output impedance, r_{ds1}, of transistor Q_1 is given by

$$r_{ds1} \approx \alpha \frac{L_1}{I_{D1}} \sqrt{V_{DG1} + V_{t1}} \tag{5.3}$$

where α is a technology-dependent parameter of around $5 \times 10^6\ \sqrt{\text{V}}/\text{m}$. This equation is at best approximate and ignores all short-channel effects that become more important for shorter channel lengths in modern technologies.

The second gain stage is simply a common-source gain stage with a p-channel active load, Q_6. Its gain is given by $(-g_{m7})(r_{ds6} \parallel r_{ds7})$. Thus, we have

$$A_{v2} = -g_{m7}(r_{ds6} \parallel r_{ds7}) \tag{5.4}$$

The third stage is a common-drain buffer stage. This stage is often called a *source follower*, because the source voltage follows the gate voltage of Q_8, except for a level shift. As shown, the substrate of Q_8 is at the same voltage as the source of Q_8. This connection is only possible when Q_8 is realized in a well that is isolated from the bulk. Thus, for this example opamp, one would require a p-well or twin-well process to realize this output stage. Tying the substrate of Q_8 to its source eliminates gain degradations due to the body effect. This connection also results in a smaller dc voltage drop from the gate to the source of Q_8, which is a major limitation on the maximum positive output voltage. As Chapter 3 shows, the gain of this source-follower stage is given by

$$A_{v3} \cong \frac{g_{m8}}{G_L + g_{m8} + g_{ds8} + g_{ds9}} \tag{5.5}$$

where G_L is the load conductance being driven by the buffer stage. When it is not possible to tie the substrate of Q_8 to its source, as is the case when an n-well process is used (currently, a popular process), then the gain of the buffer stage is given by

Small signal model of real Op Amp can be close to that of a common source amp.

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Op Amp Schematic - Real World Example

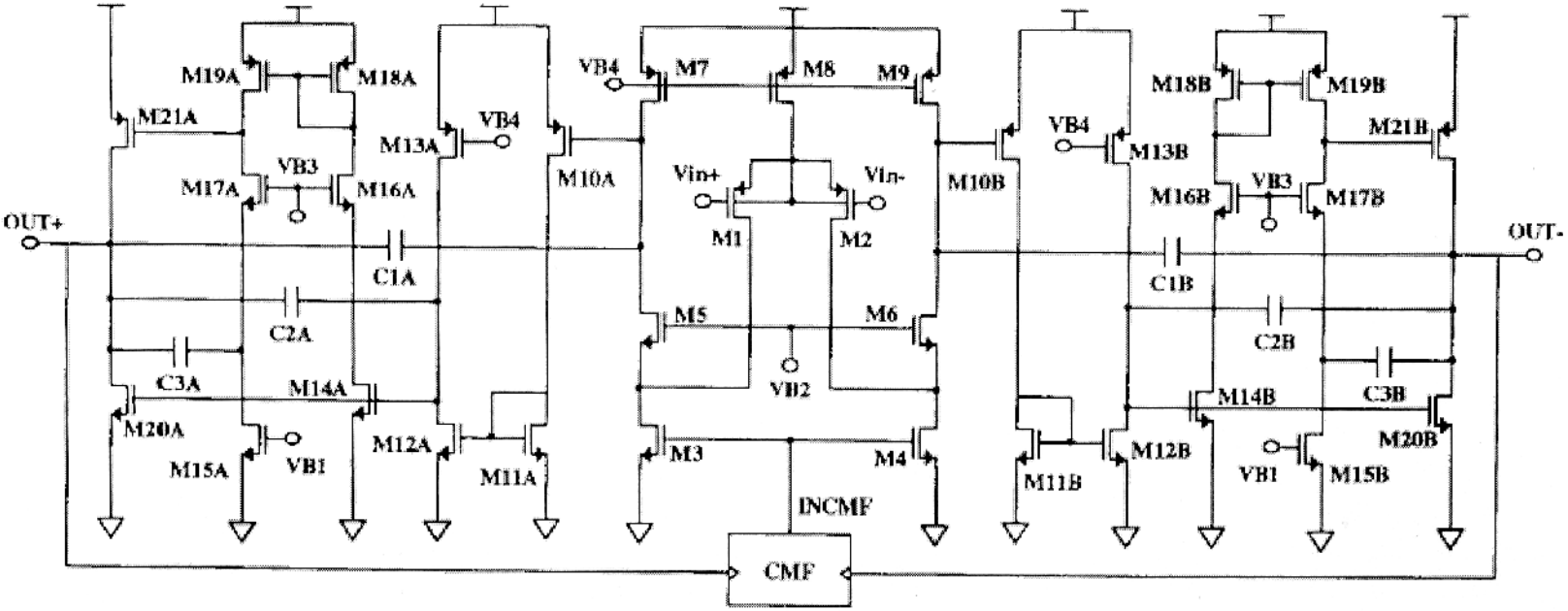

Fig. 4. Overall amplifier schematic.