ECE3020 Final Design Report Guidelines.

1. Perform a design report comparing a MOS inverting amplifier in Figure 1 to one where a BJT substitutes for the MOSFET. The Vswitch substitution is optional. Note that for a BJT, there can be a DC convergence issue in the DC sweep if Vin is too high. Either restrict Vin or add a 1 ohm resistor between Vin and the base input. Compare and contrast gain and bandwidth. For the MOS case, this is known as a common source amplifier, while for the BJT, this is a common emitter amplifier.

2. Add an inductor in parallel with the load resistor any of the single transistor amp circuit and analyze the new AC frequency response. Run a parametric step on the resistor and describe the gain-bandwidth tradeoff. Compare gain in frequency response with a transient response with sinusoidal input around the resonance frequency. The parametric step responses in the transient enables you to describe the delay-bandwidth tradeoff.

3. Add negative feedback to any of the single transistor amp circuit. Compare DC, AC, and transient behavior (sinusoid input) with different amounts of feedback.

Note the common source behavior is useful for the MOS differential pair amplifier circuit in Figure 2, as shown on the last page.

The report should have the following sections:

Abstract – write this last, it's the main things the reader wants to know.
Short problem statement and its answers.

Introduction – Problem context, requirements, and set up.

Results and Discussion – All the technical details.

Conclusion – Review your main results.

The main section is Results and Discussion. This section contains your detailed technical content, such as simulation set ups, plots, tables, hand calculations, and your explanations of your technical content. For example, every plot or figure should have some sentences which direct the reader to the main point of the plot or figure.

Analysis tips.

To find gm for MOS you use the same formulas as before, gm = 2*Ib/Vov . For a BJT, use gm = Ib/25mV (thermal voltage).

Ib is the bias current, a designer usually chooses a desired Ib. For a BJT, Ib sets gm. For MOS, more is needed: Vov = VGS – Vt, where VGS is the dc value. (Vov is the voltage over Vt, same as Veffective). To find Vov, one can set Ib = (1/2)*kp*(W/L)*(Vov)^2 and solve for Vov. However, a designer usually choose Vov to be small ~200mV. Thus, the designer actually calculates the needed W/L for the transistor. Note that W/L turns out on the order of 100, and you can set kp in the nmos model (the TopSpice default is kp = 20uA/V^2).

The remaining notes (optional) are for the differential pair in Figure 2 (as in an op amp) analysis. The differential pair behaves very much like a common source amplifier. This is discussed in textbook (Section called: Small-Signal Operation of the MOS Differential Pair) if you want more detail.

From a more simple approach, the 3dB frequency is the same result we've seen in a common source amp (low pass filter), equal to 1/RC.

For the AC gain at low frequencies, the gain is equal to gm*R/2. The ½ factor is because Vin is divided evenly in half by the two matched transistors in the differential pair. This is explained in ece5021.

As long as the DC voltage to both input transistors are the same, each transistor will have ½ of the total bias current, eg. 40uA = 0.5*80uA. This is the main advantage of this circuit, the DC input voltage can be adjusted and the bias is independent of Vt.

Finally, keep in mind this circuit is just the main part of an op amp. A better op amp is shown in figure 7.40 and 9.1 (in SedraSmith 5th. ed. Summary Slides), where the input transistors are pMOS instead of nMOS. pMOS inputs are often used, that's why we studied the pMOS common source amp. Figure 9.1 shows a second amplifier stage after the diff. Pair. The second stage can have a gain of about 20, so it's input doesn't need to vary by more than 0.25v (for 5v supply). That means the differential pair output doesn't need to vary by more than 0.25v, so it's not a problem that the outputs you see in the DC sweep have a limited useful range of 1-2volts at different Vb settings. It's more than enough.

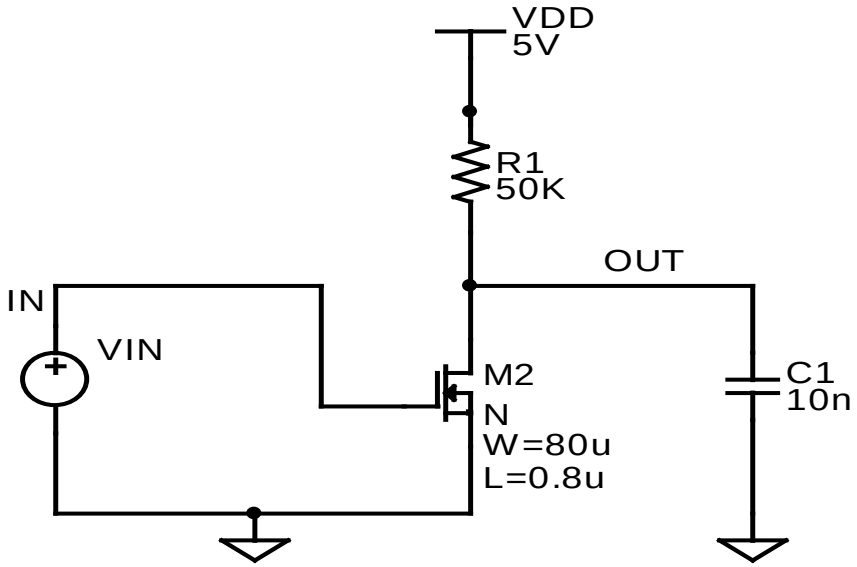

Fig. 1. Common source inverting amplifier.

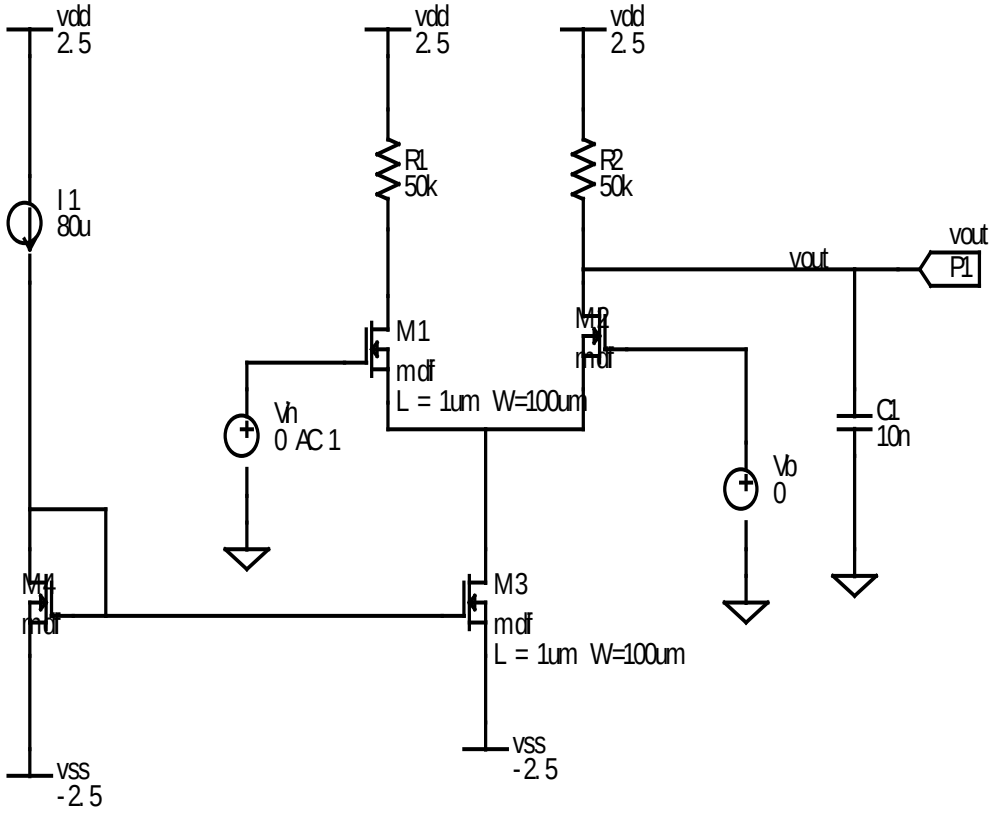

Figure 2. Differential pair amplifier