Frequency Domain UWB Multi-carrier Receiver

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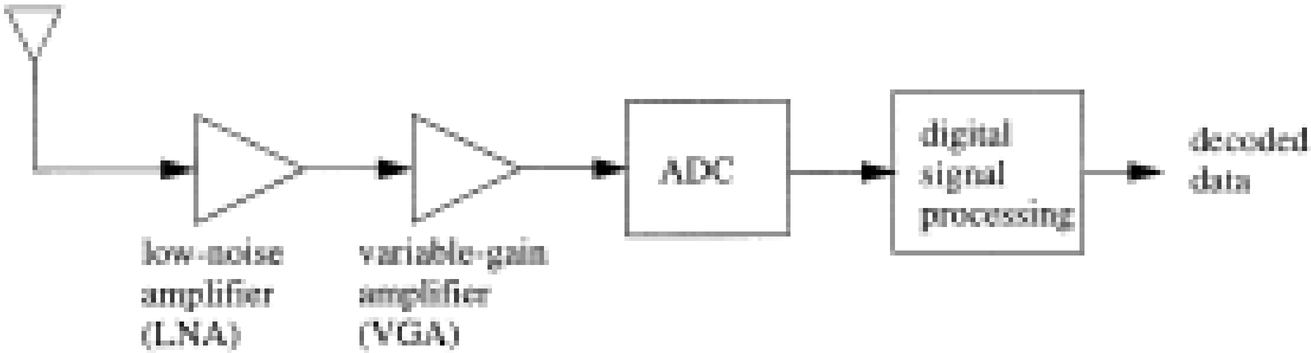
Research Purpose

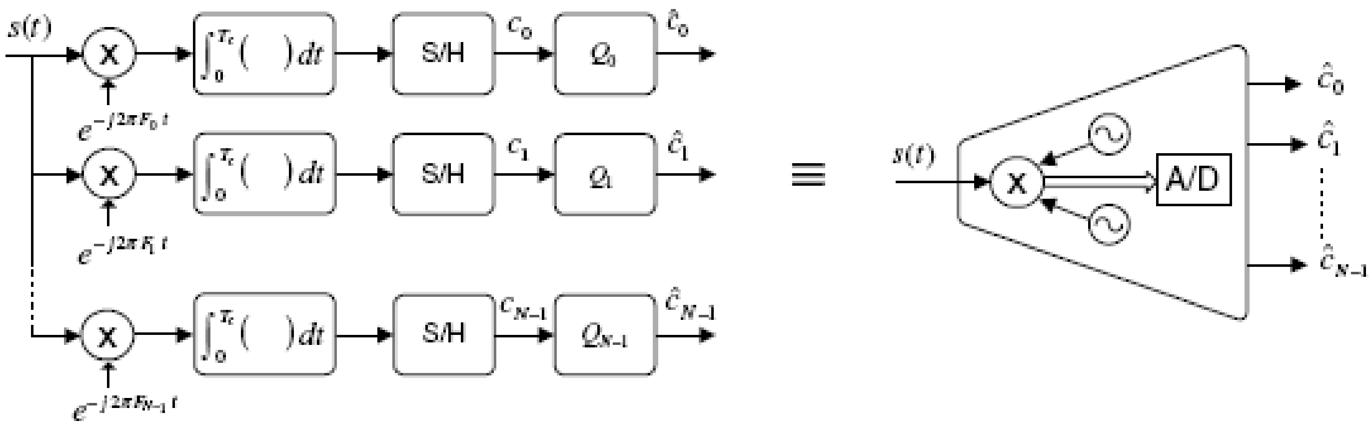
- Explore UWB multi-carrier receiver architectures that can work in very noisy environment
- Design of RF front-end circuit that maximize the dynamic range
- Design of high linearity UWB LNA with excellent robustness in presence of strong narrow band interferers

UWB receiver based on ADC in the time domain



- Require very high speed ADC and DSP module
- Strong narrow band interferers can saturate the ADC

Concept of ADC in the time domain



$$x(t) = \sum_{s=0}^{S-1} a_s e^{j2\pi f_s t}, \qquad 0 \le t \le T,$$

$$c_n = \int_0^{T_c} s(t) e^{-j2\pi F_n t}\, dt, \qquad n = 0, \cdots, N-1.$$

Problems of sampling S frequencies using S channels

- 2S mixer, S/H, integrator and ADC are needed
- Unrealistic chip area
- Huge power consumption
- Overheat is a big problem for packaging
- Results in very low bandwidth for each ADC, which is not necessary

- Solution:
  - Sample S frequencies using N channels

How to sample S frequencies using N channels

- If use one ADC per carrier

  $N=S$
- To prevent aliasing

  $T_c=S/W=T$
- If reduce the number of ADC by a factor of M

  $N=S/M$
- To prevent losing any information

  $T_c=(S/M)/W=T/M$

- Sampling of the frequency coefficient in time domain is used to estimate the frequency coefficients of nearby carriers

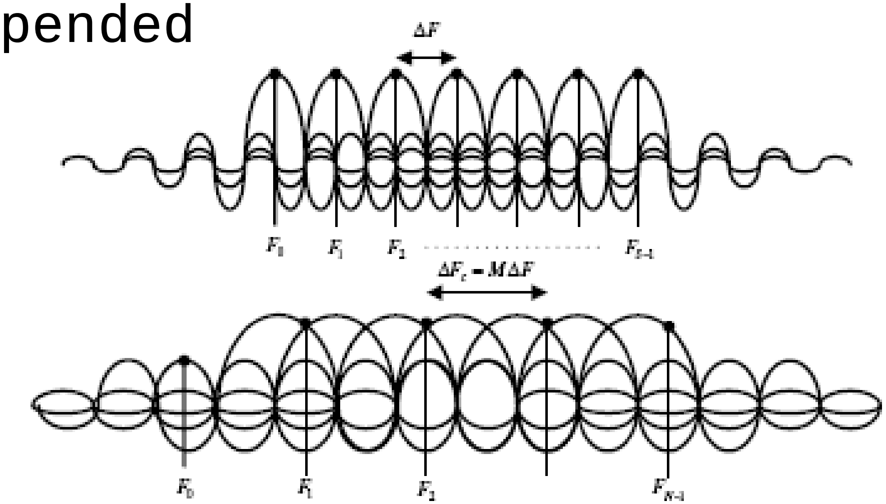
Effect of reduced conversion time

- Spectrum of each carrier is expended

$$x(t) = \sum_{s=0}^{S-1} a_s e^{j2\pi f_s t}, \qquad 0 \le t \le T,$$

$$w_m(t) = \begin{cases} 1 & mT_c \le t \le (m+1)T_c \\ 0 & \text{elsewhere} \end{cases}$$

$$X_m(F) = \mathcal{F}\{x(t)\} * \mathcal{F}\{w_m(t)\}$$

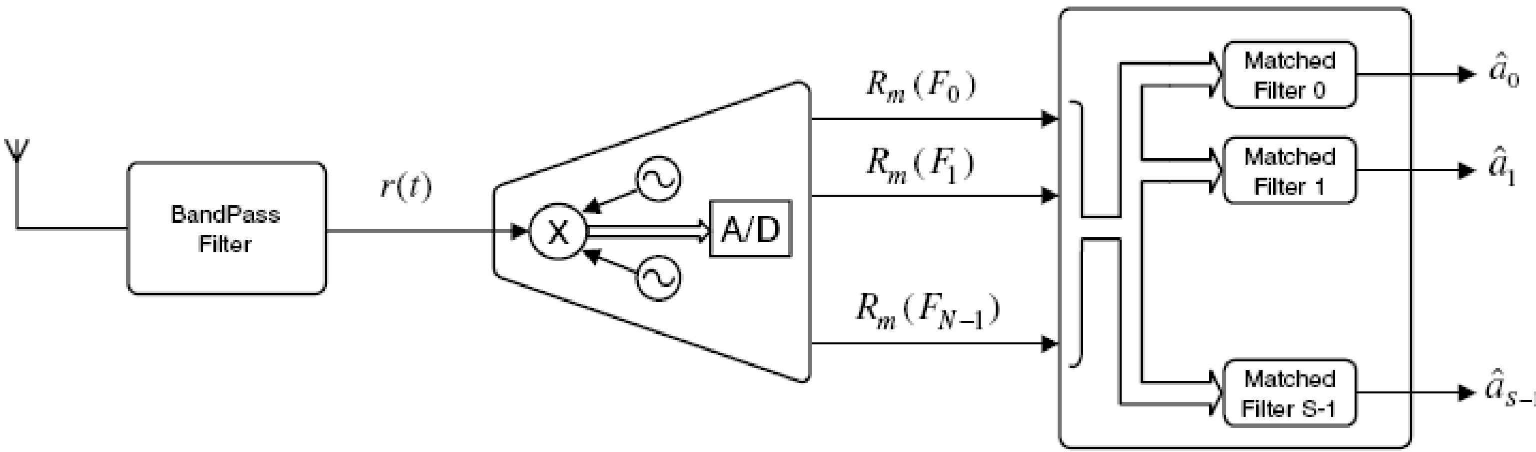


- The spectrum of the UWB signal is expended, slightly

$$W = (S + M - 1)\Delta F$$

- The multi-carrier signal is not longer orthogonal
  - Not a problem.
  - Signal can be resolve by matched filter in DSP module

Multi-carrier receiver based on ADC in the frequency domain



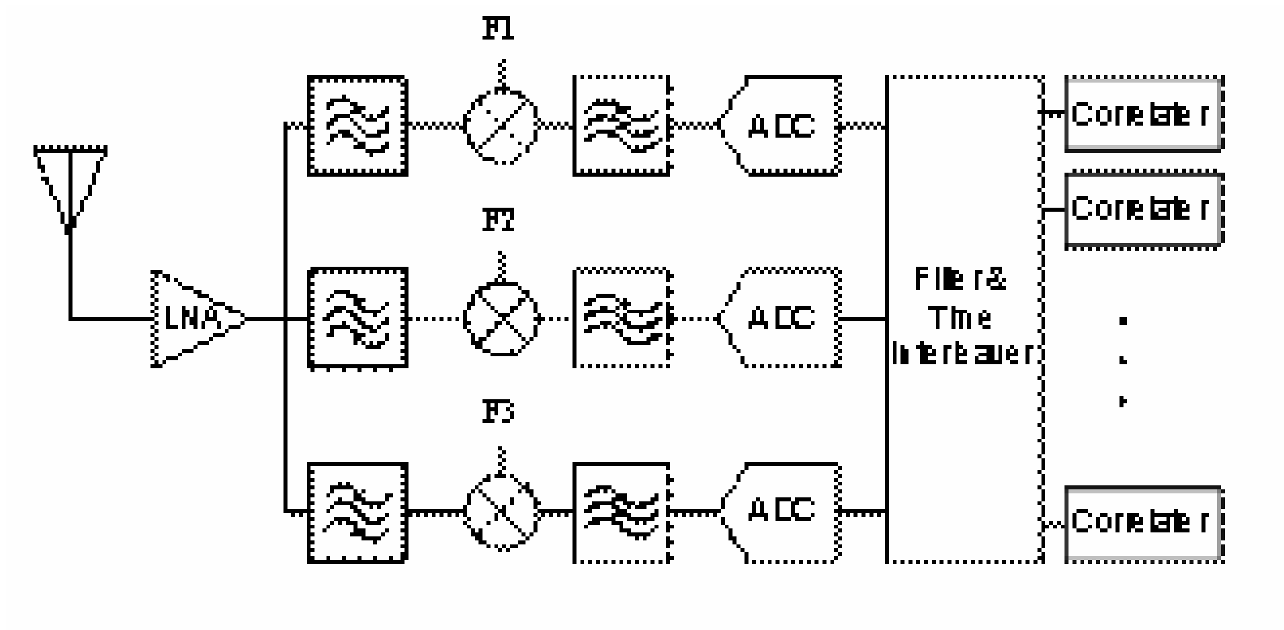
$$x(t) = \sum_{s=0}^{S-1} a_s e^{j2\pi f_s t}$$

$$r(t) = x(t) * h(t) + z(t) \qquad g_s^*(t) = e^{-j2\pi f_s t} * h^*(t)$$

$$r_m(t) = r(t) w_m(t), \quad g_{s,m}(t) = g_s(t) w_m(t),$$

$$\bar{a}_s \approx \sum_{m=0}^{M-1} \Delta F_c \sum_{n=0}^{N-1} \left(R_m(F_n) G_{s,m}^*(F_n) + R_m(-F_n) G_{s,m}^*(-F_n) \right)$$

Proposed UWB Receiver Architecture



Advantages

- Reduce the number of ADC
- Relax the sampling Rate for S/H & ADC
- Less power consumption and chip area
- Robustness to frequency offset

Most importantly:

If one channel is saturated, symbols can still be received from other channels.

Robust to strong narrow band interferers

System level simulation

Goal:

evaluate the proposed UWB receiver at the system level, study the effects of nonidealities of the components on the receiver performance

- Use VerilogA to built behavioral model of LNA, mixer, bandpass filter, integrator, etc.
- Instantiate the components in Cadence and run simulation in time domain
- Use of spectreRF is possible, but convergence is very difficult

Example: VerilogA code for integrator

```
`include "discipline.h"
`include "constants.h"


module integrator(sigin, sigout);
input sigin;
output sigout;
electrical sigin, sigout;
parameter real sigout0 = 0;
parameter real gain = 1;

  analog
        V(sigout) <+ gain*idt(V(sigin), 0) + sigout0;

endmodule
```

Front-end Circuit Design Considerations

- LNA should provide sufficient gain
- LNA should exhibit excellent noise performance
- Good interstage impedance matching between LNA and multiple mixers at difference frequency should be maintained.
- LNA should keep simultaneous input and noise match over wide frequency range
- LNA should exhibit superior linearity such that it won’t be saturated by strong narrowband interferers

Previously Reported LNA Linearization Methods

- Optimum gate biasing
- Derivative superposition method

→ Effective only at relatively low frequency

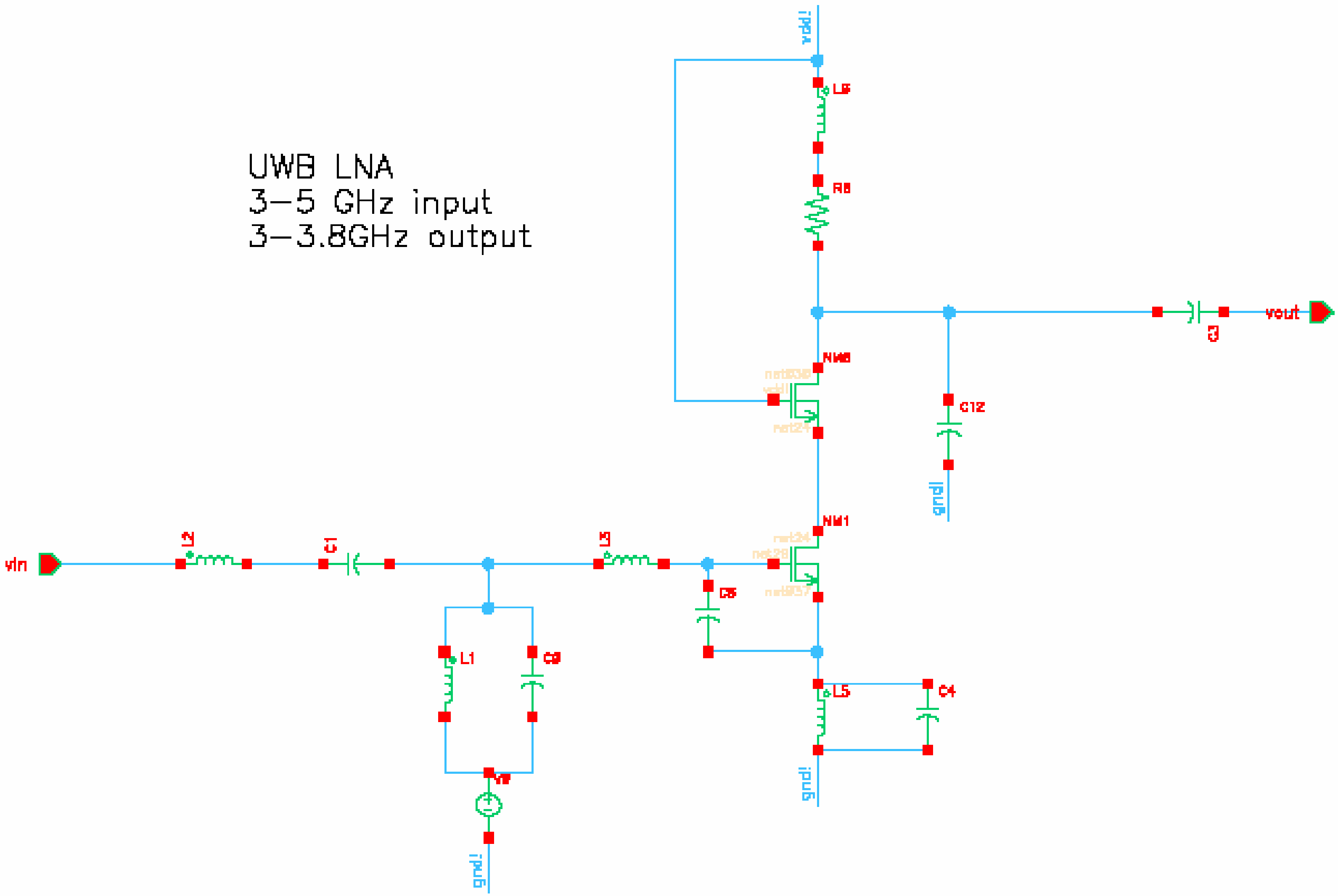
- Active post distortion
- Feed forward distortion cancellation

→ Not applicable for UWB application

Proposed techniques for UWB LNA linearization

- Choose small device channel length for improved linearity
- Increase the gate biasing to achieve a more linear device I-V curve
- Use passive network for output impedance match

Proposed UWB LNA Circuit



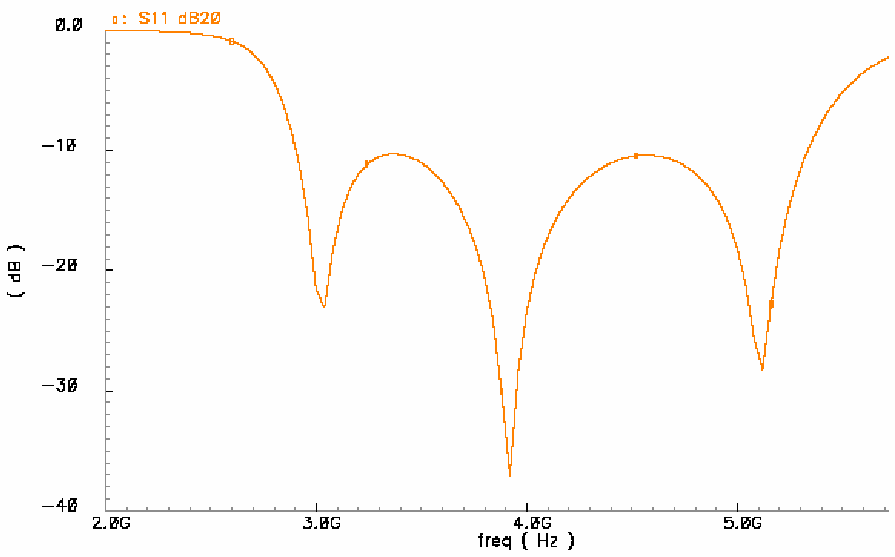
UWB LNA Simulation Results

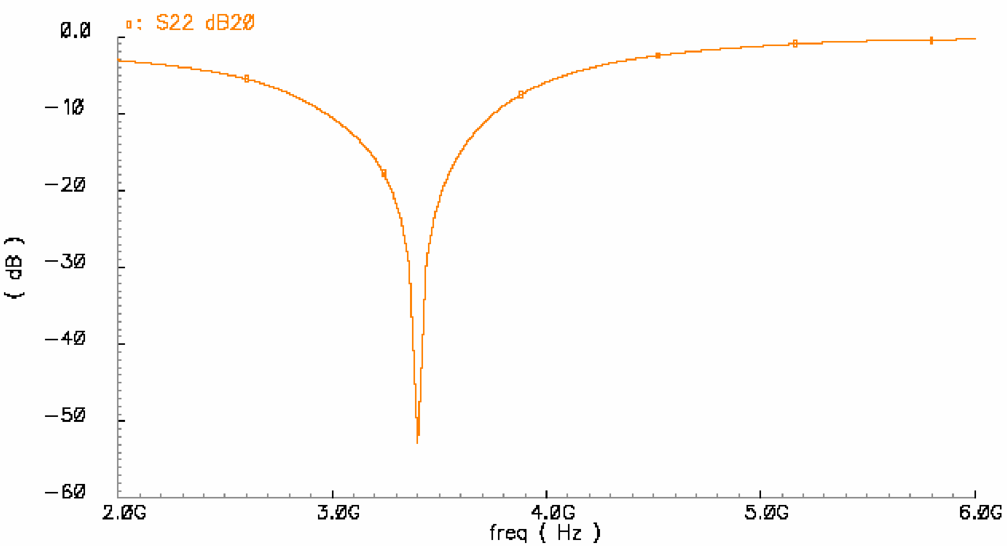
Input impedance match

the S11 < –10 dB in frequency range of 3-5 GHz.

Output impedance match

the S22 < –10 dB in frequency range of 3.0-3.8 GHz.





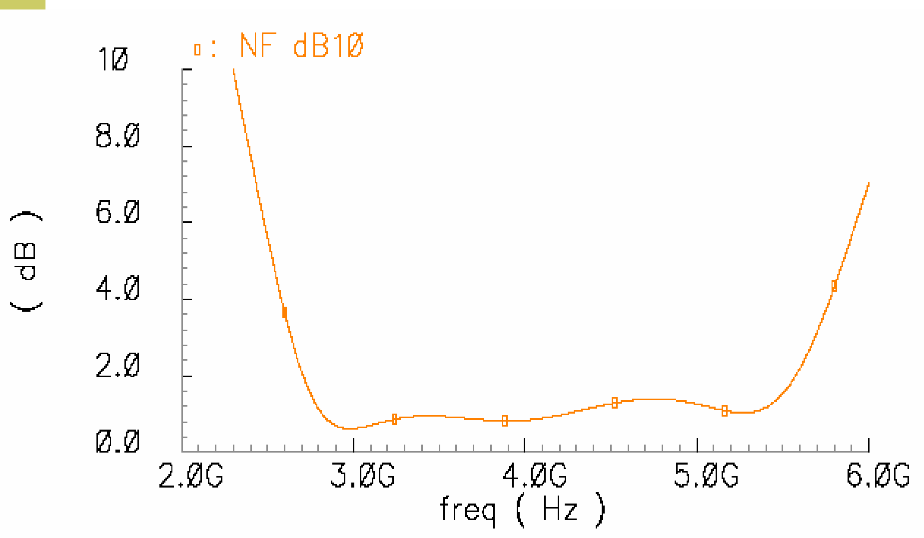
UWB LNA Simulation Results

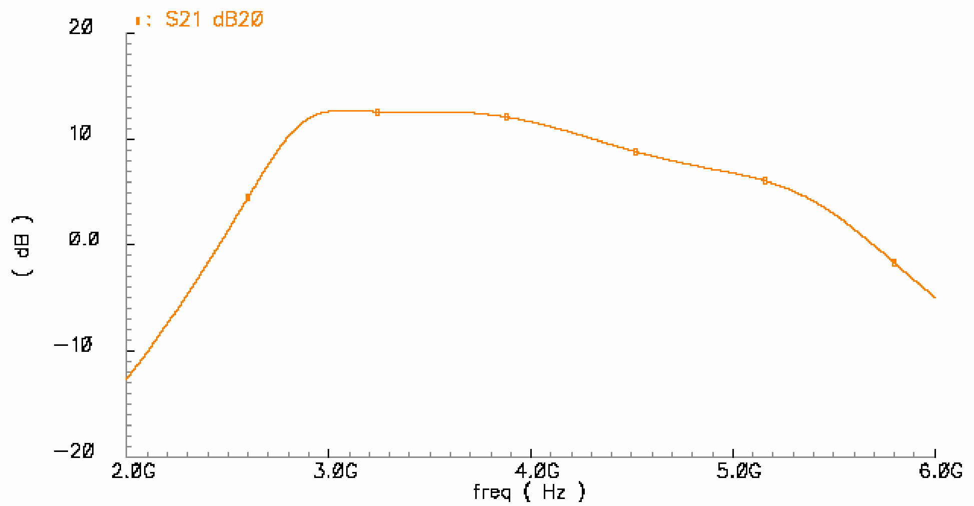
Noise performance

Low noise figure (0.63-1.4 dB) over the frequency range from 2.9-5.3 GHz

Gain

Flat gain (12.3-12.6 dB) over 3-3.8 GHz.





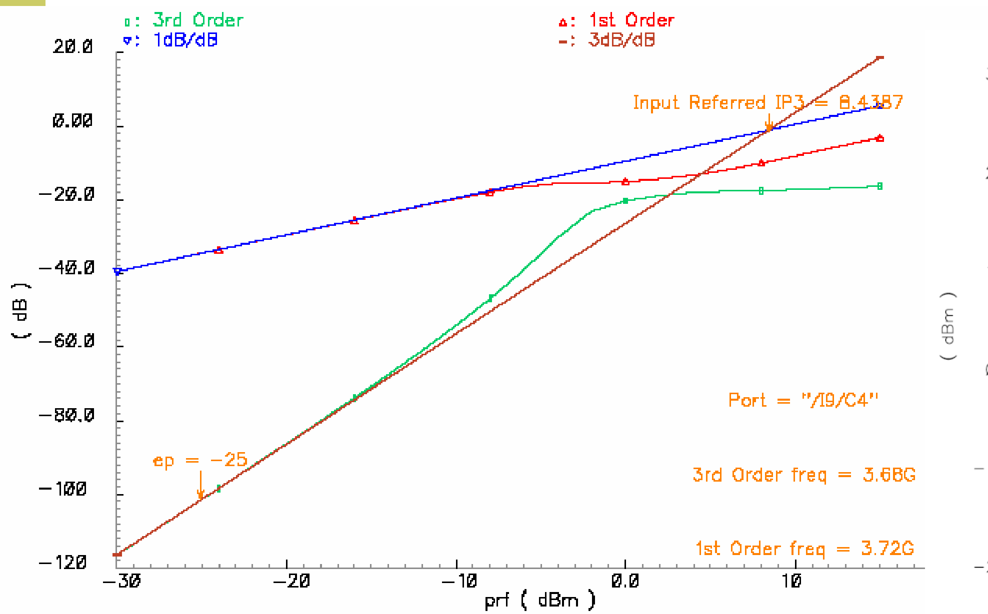
UWB LNA Simulation Results

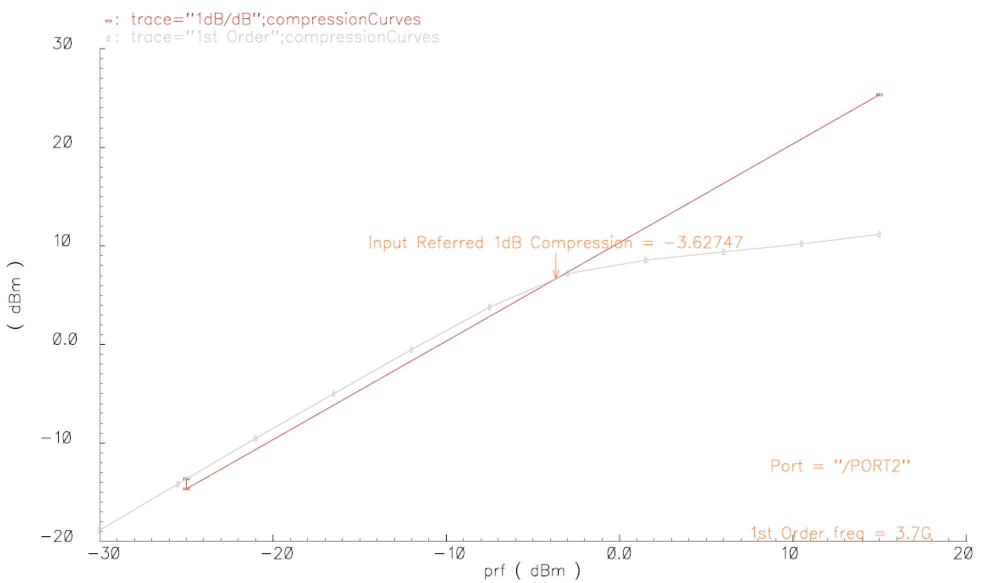
IIP3

IIP3 is 8.487 dBm at 3.7 GHz, which is about 10 dBm higher than the currently reported UWB LNAs

1 dB compression point

1dB compression point is –3.627 dBm at 3.7 GHz





Comparison with Other Works

	This Work	[1]	[2]	[3]	[4]	[5]
Process	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
$S21_{peak}$ (dB)	12.6	9.3	11.6	13.2	10.9	13.5~15.9
S11 (dB)	<-10	<-9.9	<-9	-5.3	<-11.5	<-12.19
S22 (dB)	<-10	NA	<-12	<-10.3	NA	<-10.1
NF (dB)	0.63-1.4	4.0	4.75	2.59	3.5	4.7~6.7
Frequency Range (GHz)	3~5	2.3~9.2	6~10	5.6~5.96	2.6~9.2	3~6
BW	50%	NA	50%	6%	NA	67%
Power Consumption (mW)	29	9	11.6	22.2	7.1	59.4
IIP3 (dBm)	7.5~11.25	-6.7	1.15	NA	-5.1	-5
1dB CP (dBm)	-3.6	-15	-11.1	-14.0	-15.3	-14

Summary

- A multi-carrier receiver architecture based on frequency domain ADC is discussed
- A frequency domain UWB receiver architecture is proposed
- Approaches for system level simulation of the receiver is discussed
- Techniques to improve LNA linearity were explored
- A high linearity, low noise, flat gain LNA is designed in tsmc0.18 process
- Significant improvement in IIP3 and 1 dB compression point is observed