Analog/Mixed Signal Synthesis for High-Speed Input/Output Channels

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Abstract—— **High-speed input/outputs (I/O) are in demand due to advances in integrated circuits (ICs), which made it possible to obtain multi gigahertz clock speeds. However, as very large scale integration (VLSI) technology scales down, the pin bandwidth does not scale accordingly. Some factors to consider in designing of high-speed I/Os are the integration of analog and digital circuitry, the interconnect performance, the precision required in processing of analog signals, and the sensitivity of analog circuit to noise, crosstalk and interference. Given that I/O design involves the emergence of both analog and digital circuitry, the design flow is comprised of a mixed-signal scheme. Less experienced designers usually use ad hoc methods to simulate the trade-offs between digital and analog modules, since there is a lack of standard simulation test-benches. Recent research in analog synthesis has demonstrated that goal oriented test-benches are the key enabler for analog re-use. This paper address a system methodology that can be used to set up a common simulation platform such that test-benches created for system model may be directly used for testing the spice modules.**

I. INTRODUCTION

Simulation and modeling have different stages depending on the design objective. During the conceptualization of the design, simulation is typically used to explore "what if" scenarios. Also, simulations are needed to implement design standards. In both cases, the objective is to characterize the system and it is well known that characterizations are divided into ideal and non-ideal behaviors. The characterization of an ideal behavior is basically used for design exploration. On the other hand, non-ideal behaviors of various components and subsystem are modeled for physical verification.

Today, most high-speed input/output (I/Os) use standards such as RapidIO, Hypertransport, PCI Express and others which utilize three approaches 1) packet switching, 2) point-to-point and 3) minimal pin count [2]. These different types of serial I/Os are distinguished by the formatting of the data, the type of timing and the ancillary analog-to-digital/digital-to-analog (ADC/DAC); nevertheless, the simulation test-benches are similar. The need for more bandwidth to support inter-device communication requires design exploration. For example, the use of one interconnects technology rather than bridging several interconnect technologies can be explored during the conceptualization process. The exploration of one standard or combination of standards can be characterized in a timely basis if standard simulation for high-speed I/Os exist.

This paper focuses on system development that standardizes the simulation procedure using a point-to-point multilevel signaling scheme as an example. The key blocks are the transmitter, receiver and channel. The main concentration is the system methodology, which emphasize both the early system development that uses equation based models in HDL and a realizable system architecture that contain detail model for spice integration and verification.

II. SYSTEM DEVELOPMENT

The implementation of high-speed I/Os in the giga bit range requires engineers to have knowledge on inter-device communication, and the impact of system topology. This involves the merging of various disciplines such as communication system engineering, circuit design, PCB board design, etc. Most of the time, each discipline uses different languages and have different simulation goals. Also, in large high-speed design, signal-path challenges and simulation speed are always important issues [3].

A. The Art of Mixed Signal System Design

System models are needed in two places in the design flow. First, in the early stages, system model (A) is used to make high level design decisions by evaluating architectural tradeoffs. Secondly, after the circuit level design phase (after

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spice), system model (B) is used in the system integration and verification stage of the design to speed up simulation. The A type models are only needed to make some design decisions and any high level language can be used to help the designer make quick decisions and then proceed to the detailed schematic entry. If a cluster simulation methodology is not amenable to the design group then B type models are developed. In some cases, B type models can be derived from A type models. The main requirement for the system B type model is the integration of system simulations and spice simulations where the spice simulations are used for the detailed schematic design. Thus, some form of hardware description language (HDL) is often used. The most useful part of the B type models is the creation of test-benches that can calibrate the B type models to the detailed schematic design. Unfortunately, there is no standard language for these test-benches, although what is often used is some combination of spice control/post processing commands and vendor specific constructs.

B. System Development for Multi-level Chip-to-chip Interface

The system model A of a high-speed I/O can be based on communication concepts shown in the block diagram of Figure 1. The system consist of a transmitting filter having an impulse response $p_T(t)$, a channel filter and a receiving filter with an impulse response $p_R(t)$.

Figure 1: Block diagram representing a system A type model of data transmission over a bandlimited system.

The output of the transmitting filter (the input to the channel) may be express as

$$s(t) = \sum_{m=-\infty}^{\infty} b_m \cdot p(t - mT) \qquad (1)$$

where T= k/Rb is the symbol interval (1/T = Rb/k is the symbol rate), Rb is the bit rate and $\{b_m\}$ is a sequence of amplitude levels. The channel output, which is the received signal at the demodulator, may be express as

$$r(t) = \sum_{m=-\infty}^{\infty} \left(b_m \cdot h(t - mT) + n(t)\right) \qquad (2)$$

where h(t) is the convolution of the impulse response of the transmitted filter and the channel filter, $h(t)=c(t)*p_T(t)$ and n(t) represent Gaussian noise.

The received signal passes through a linear receiving filter, if this filter is matched to h(t), then its output SNR is maximum at the proper sampling instants. The output of the receiving filter may be express as

$$y(t) = \sum_{m=-\infty}^{\infty} \left(b_m \cdot x(t - mT) + \eta(t)\right) \qquad (3)$$

where $x(t)=h(t)*p_R(t)=p_T(t)*c(t)*p_R(t)$ and $\eta(t) = w(t)*p_R(t)$ denotes the additive noise at the output of the receiving filter.

To recover the information symbols $\{b_m\}$, the output of the receiving filter is sampled periodically, every T seconds. Thus the sampler produce

$$y(nT) = \sum_{m=-\infty}^{\infty} \left(b_m \cdot x(nT - mT) + \eta(nT)\right) \qquad (4)$$

which can be rewritten as

$$y_n = x_0 \cdot b_m + \sum_{(m \neq n)} \left(b_m \cdot x_{n-m} + \eta_n\right) \qquad (5)$$

The first term on the right hand side (RHS) of equation 4 is the desired signal. If the receiving filter is matched then the x_0 is scaled to the received signal energy [4]. The second term on the RHS of equation 4 represents the effects of other symbols overlapping due to the sampling instant, t = nT is called intersymbol interference (ISI). This system demonstrates a mathematical representation of the system A type model, which captures the modulation scheme for the transmitter, the gaussian noisy channel and the signal response of transmitted signal. One of the goals of the system A type model is to quickly make high level design decisions by evaluating the functional blocks. The performance criteria and constraint of the system A type model varies based on modulation, bandwidth, data rate and channel characteristics. For instance, the chip-to-chip interfaces have a static channel characteristic, which enables a symbol-signaling scheme. In this example, the pulse amplitude modulation (PAM) scheme was chosen due to its easy physical implementation in CMOS technology.

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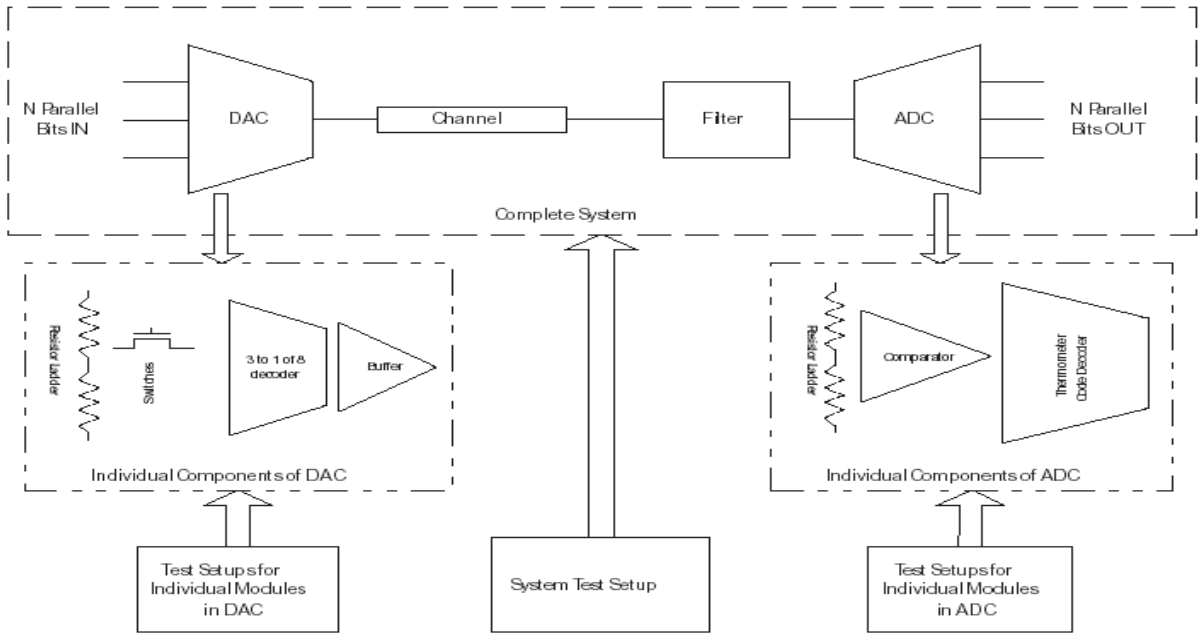

Figure 2: Practical implementation of a multilevel system

The above system A type model can be produced in languages such as Matlab, Excel, C++, HDL and various combinations. The language chosen in this paper is verilog-AMS which is a mixed signal HDL (HDL-AMS). The signals given in equations 1-5, give the underlining structure in which the signal libraries are built in verilog-AMS. Some of these libraries include the pulse shape of raised-cosine, sinc and rectangular pulse. In languages such as Matlab, these pulse shape libraries already exist. However, the system model must be able to integrate with spice simulations which can be done, in the, digital domain in languages such as Matlab or requires a co-simulator such as simulink pspice (SLPS). Using HDL-AMS creates a common platform such that B type model can be generated from A type model and the test-benches developed can be used to calibrate the detailed schematic design. As a result, there is an initial effort needed to create libraries using HDL-AMS.

The most useful physical design implementation process requires the system B type model to be able to simulate and integrate with the circuit level (spice) simulation. Figure 2 captures the practical implementation of a multilevel system using sub-systems of the ADC, DAC and Filter. Inside each sub-system there are architectural building blocks of the circuit. For example, the inside of the ADC (assume flash ADC) consists of a resistive ladder, comparator and thermometer circuitry. In addition, Figure 2 is an architectural representation (system B type model) of Figure 1, the equation representation (system A type model) which requires a mixed signal design flow. For instance, the DAC generates the PAM signal at the transmitter, the ADC represents both the receiver and sampler and the band limitation of the channel is depicted by a low pass filter. With regards to the analog portion of the mixed signal system, the system models should be done minimally, since they are not as useful as the digital system models. The reason for this is, in a full tapeout design flow, the detailed analog schematic will still need to be generated by the designer, in order to perform layout vs schematic (LVS) and other cell level design verification operations. This is not the case for digital design, in which the detailed schematics for LVS are generated automatically, that is once the system HDL as been created, the circuit schematic and layout are generated automatically. These detailed schematics with the attached transistor models can then be used to perform system simulations using computer clusters. Hence, Figure 2 depicts an experienced view of a top-level system that conveys the mixing of levels of abstraction.

III. CONCLUSION

In any new system development, the system designer should be able to quickly integrate the functional blocks of the design to explore the conceptualization process. However, this requires large libraries of pre-built and tested blocks. Initially it requires lots of time and effort to develop and test libraries within a uniform platform, and to document the design. In addition, the questions that system engineers face are as follows: what are the system models sufficiency

requirements and how useful are the HDL-AMS models in early system design development. These questions are usually answered more efficiently with experience. Ironically, the system B type models are developed as part of a bottom up design activity and the HDL-AMS finds it most common use in the bottom up portion of the design flow, where the integrations take place.

The methodology discussed in this paper requires both top-down and bottom-up design flow, that is the use of simulations and verification process at both the system and circuit level of abstraction. This type of methodology allows for 1) the exploration of the high-speed I/O at the same time setting up parametric libraries using HDL-AMS 2) creation of test-benches for design re-use and 3) the integration of analog and digital circuitry.

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