Extending CMOS: Quantum Functional Circuits Using Si-Based Resonant Interband Tunnel Diodes

Paul R. Berger
Department of Electrical and Computer Engineering
Department of Physics
The Ohio State University
Columbus OH, 43210 USA
Collaborators

**Naval Research Laboratory**
Phillip E. Thompson, Karl Hobart, and Brad Weaver

**Rochester Institute of Technology**
Sean L. Rommel, Santosh K. Kurinec, and Karl D. Hirschman

**University of California, Riverside**
Roger Lake

**NIST, Gaithersberg**
David Simons
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Phillip E. Thompson (Naval Research Laboratory),
Motivation: Extending CMOS?

- CMOS cannot be scaled indefinitely.
- Solutions: either replace or augment scaled CMOS
- Tunnel diodes married with CMOS offer enhancements
The Limitation of CMOS

- As CMOS dimensions are reduced, evolutionary changes will stop when quantum effects dominate and alternative revolutionary paradigms will be sought. Examples of CMOS salient issues:
  - Gate oxide tunneling
  - Dopants fluctuations
  - Channel quantization effect

- The 2001 ITRS Roadmap expects CMOS can shrink to channel lengths of 20-30nm before a new type of device will replace CMOS.
ITRS: Emerging Research Devices

- Monolithic Integration of Si-based tunnel diodes with Si-based transistors

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**Table: Emerging Research Devices**

<table>
<thead>
<tr>
<th>Device</th>
<th>Resonant Tunneling Diode – FET</th>
<th>Single Electron Transistor</th>
<th>Quantum Cellular Automata</th>
<th>Nanoscale Devices</th>
<th>Molecular Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Types</td>
<td>3-terminal</td>
<td>3-terminal</td>
<td>Electronic QCA</td>
<td>FET</td>
<td>2-terminal and 3-terminal</td>
</tr>
<tr>
<td>Advantages</td>
<td>Density, Performance, RF</td>
<td>Density, Power, Function</td>
<td>High power density</td>
<td>Density, Power</td>
<td>Identity of individual switches (e.g., size, properties) on sub-nm level. Potential solution to interconnect problem</td>
</tr>
<tr>
<td>Challenges</td>
<td>Matching of device properties across wafer</td>
<td>Low temperatures, Fabrication of complex, dense circuitry</td>
<td>Limited fan out, Dimensional control (room temperature operation), Architecture, Feedback from devices, Background charge</td>
<td>Now device and system, Difficult route for fabricating complex circuitry</td>
<td>Thermal and environmental stability, Two terminal devices, Need for new architectures</td>
</tr>
<tr>
<td>Maturity</td>
<td>Demonstrated</td>
<td>Demonstrated</td>
<td>Demonstrated</td>
<td>Demonstrated</td>
<td>Demonstrated</td>
</tr>
</tbody>
</table>

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International Technology Roadmap for Semiconductors (ITRS), which is a consortium of international semiconductor manufacturers and semiconductor equipment vendors, annually forecasts future semiconductor technology

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NOEL

Si-Based RITDs (Berger)  March 11, 2005
Basic Physics: Esaki Tunnel Diode (Interband)

Degenerate Doping Required – Difficult with conventional epitaxy

Basic Physics: Resonant Tunneling Diode (Intraband)

Large Band Offset Required

Si/SiGe heterojunction has limited band offset without a thick relaxed buffer

Alternative barriers (i.e. SiO$_2$) present difficult heteroepitaxy of single crystal Si quantum well atop amorphous barrier

Three Interband TD Current Components


- Desired: optimize structure for efficient quantum mechanical tunneling
- Undesired: excess current comprised partially of defect related tunneling
- Thermal diffusion current eventually takes over at higher biases

**Basic TD Figure-of-Merit**

- Peak-to-valley current ratio (PVCR) = \( I_p/I_v \)
- Peak current density (PCD or \( J_p \)) = \( I_p/A \), where \( A \) is the diode area
Excess Current of an Esaki Diode

Figure adapted from Sze, Physics of Semiconductor Devices, pg. 528 (1981).

• Excess current limits PVCR.
• Excess current is a tunneling phenomena via defect or midgap states

Application: Tunnel Diode Memory

- One Transistor Tunnel Diode SRAM (1T TSRAM)
- Compact replacement for 6 transistor SRAM cell
- Refresh-free – Low Power Consumption


LATCHED COMPARATOR 25 GHz DESIGN
(Courtesy A. Seabaugh, formerly Raytheon Systems)

Quantum
- Latching behavior is inherent to RTD
- Settling time is determined by RTD switching speed

• Regenerative feedback gives latching
• Feedback loop has long settling time

2 RTDs
2 HFETs
Area=1

Conventional

12 HFETs
6 Schottky Diodes
Area=6

SPICE Simulations
The Payoff: TDs Integrated with Transistors

More computational power per unit area

☑ Fewer devices required
☑ Faster circuits and systems
☑ Reduced power consumption

Result: Extension of CMOS if a Si-Based TD is available that is compatible with CMOS!
Prior Art: Lack of Si-Based TDs that can be Monolithically Integrated with Si transistors

- Vintage 1960’s alloy technology prevents large-scale batch processing
- Discrete Esaki diodes are ideal for niche applications.
- However the alloy process does not lend itself to an integrated circuit.
First Si-Based Resonant Interband Tunnel Diodes

<table>
<thead>
<tr>
<th>Approach</th>
<th>$\Delta E_C$ (eV)</th>
<th>Upper Barrier Crystalline</th>
<th>Quantum Well Crystalline</th>
<th>Lower Barrier Crystalline</th>
<th>Production Potential</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$/a-Si/SiO$_2$</td>
<td>3.2</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>High</td>
<td>Abandoned - High scattering in quantum, no room temperature PVR</td>
</tr>
<tr>
<td>Ca$_2$/Si/CaF$_2$</td>
<td>2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Low</td>
<td>Abandoned - Tendency for island growth, defect-assisted transport below 10 nm</td>
</tr>
<tr>
<td>ZnS/Si/ZnS</td>
<td>1</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Med.</td>
<td>ZnS on Si growth established, Si quantum well growth under study</td>
</tr>
<tr>
<td>SiO$_2$/Si/SiO$_2$ Lateral overgrowth</td>
<td>3.2</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Med.</td>
<td>Process for forming oxide islands established, overgrowth process under development</td>
</tr>
<tr>
<td>ZnS/Si/ZnS Lateral overgrowth</td>
<td>1</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Med.</td>
<td>ZnS islands have been prepared for first overgrowth experiments</td>
</tr>
<tr>
<td>SiO$_2$/SiGe(C)/SiO$_2$ Lateral overgrowth</td>
<td>3.2</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Med.</td>
<td>Oxide islands have been prepared for first overgrowth experiments</td>
</tr>
<tr>
<td>Si/SiGe resonant interband tunnel diode</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>High</td>
<td>World’s first demonstration on Si; room temperature peak-to-valley current ratio of 1.6</td>
</tr>
</tbody>
</table>

A paradigm shift from other approaches was spearheaded by a team of researchers lead by Berger (then at the University of Delaware), Naval Research Laboratory and Raytheon Systems.

- DARPA Award of Excellence (1998)
- Late News at International Electron Devices Meeting.
- Best Science/Engineering Dissertation
- Special Invitation to 2003 ITRS Meeting

Front page of the Wall Street Journal (October 1, 1998).

A ‘TUNNEL’ VISION for faster circuitry nears reality, researchers say.

In 1957, Nobel laureate Leo Esaki discovered that electrons could “tunnel” through solid barriers via tiny electrical devices and the “semiconductor tunnel diode” was born. Now, researchers at the University of Delaware, the Naval Research Laboratory and Raytheon Systems Co. say they can mass-produce tunnel diodes on silicon wafers, advancing the possibility of broad commercial use.

“This is the first tunnel diode that is compatible with a silicon integrated-circuit process,” says Alan Seabaugh, a Raytheon scientist. The new tunnel diodes will replace previously cumbersome ones, allowing them to meld with high-tech transistors on chips, says Prof. Paul Berger of Delaware. Initial use could include high-speed data-transfer, such as converting analog date to digital format in radar receivers.

Down the road, the new technology could mean fewer battery recharges for laptops and other consumer devices.
World’s First Si-Based Resonant Interband Tunnel Diode (1998)

- Low growth temperature (320 °C)
- CMOS process compatibility

Modeling of First RITD Band Diagram
Roger Lake, now at UC Riverside

- 33% of dopants are assumed active
- Calculated by solving the effective mass Schrödinger equation and iterating to converge with Poisson’s equation.
- 0.3 V taken to be the peak voltage

- δ-doping allows degeneracy condition to be satisfied
- δ-doping can provide QWs that allow resonant interband tunneling

V = 0.3 V
T = 300K

EXz = -0.269
EHH = -0.244
ELH = -0.254

March 11, 2005
5 Key Features of the Original RITD Design

- An **intrinsic layer** is used as the central tunneling spacer, which reduces carrier scattering. Both Si and Si/Si$_{1-x}$Ge$_x$ composite spacers have been explored. The addition of Ge provides greater momentum mixing and therefore higher current densities.

- A pair of δ-doping planes of B and P (or Sb) provide highly degenerate doping levels which can confine quantum states in potential energy wells. The gap between δ-doping planes is assumed the tunneling distance.

- Fixed offsets between the δ-doping planes and the tunneling spacer were introduced in some SiGe designs to minimize the outdiffusion of dopants and impurity accumulation into the central tunneling spacer.

- Samples were epitaxially grown by **low-temperature molecular beam epitaxy (LT-MBE)** to allow for greater dopant incorporation and abrupt interfaces minimizing segregation and diffusion.

- Short post growth **rapid thermal annealing (RTA) heat treatments** were introduced to reduce the point defect density associated with low temperature growth. Diffusion during annealing may decrease the spacer thickness and reduce as-grown δ-doping levels.

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Isothermal Annealing Effects with Cladding

Diffusion barrier cladding surrounding the δ-doping spike raises the process thermal budget and allows for greater defect annihilation before interdiffusion becomes serious.


Annealed 825 °C for 1 minute
High Peak-to-Valley Current Ratios

Si/Si$_{0.6}$Ge$_{0.4}$/Si RITDs
Grown at 320 °C

100 nm n+ Si
P δ-doping plane
2 nm undoped Si
4 nm undoped Si$_{0.6}$Ge$_{0.4}$
B δ-doping plane
1 nm undoped Si$_{0.6}$Ge$_{0.4}$
100 nm p+ Si
p+ Si substrate

MBE Heterostructure

Greater defect annihilation leads to less excess current in valley region and therefore higher PVCRs

PVCR: 3.8
$J_p$: 2 kA/cm$^2$

OSU/NRL RITDs
50 µm diameter diodes
800°C, 1 min anneal

Si-Based RITDs (Berger) March 11, 2005
Very High Peak Current Densities

Si/Si$_{0.6}$Ge$_{0.4}$/Si RITDs Grown at 320 °C

- 100 nm n+ Si
- P $\delta$-doping plane
- 1 nm undoped Si
- 2 nm undoped Si$_{0.6}$Ge$_{0.4}$
- B $\delta$-doping plane
- 1 nm undoped Si$_{0.6}$Ge$_{0.4}$
- 100 nm p+ Si
- p+ Si substrate

By reducing tunnel barrier, over 150 kA/cm$^2$ current density!

High current densities valuable for fast switching and RF Mixed Signals


March 11, 2005
NSF Press Release on High Jp RITDs

January 15, 2004

For more information on these science news and feature story tips, contact the public information officer listed at (703) 292-8070. Editor: Josh Chamot

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- RESEARCHERS USE BACTERIA TO PRODUCE POWERFUL, ELUSIVE CATALYST
- ARMING COMPUTERS WITH TOOLS FOR SELF-DEFENSE

Researchers Break Electronics Speed Record

New diode may lead to new generation of faster, cheaper, smaller electronics

Engineers have fused a 1950s concept with modern semiconductor processing and design to create a diode that can move electrical current at record-breaking rates.

At room temperature, the diode (a device that behaves like a valve for electricity traveling within a circuit) can transmit current equivalent to 150,000 amps per square centimeter, three times the rate of its closest competitors. For comparison, standard wiring in a home carries a maximum current density of only 700 amps per square centimeter.

Known in the research community as a "resonant interband tunneling diode," the silicon-based semiconductor has applications in computers and other electronic devices, and may eventually boost cellular phone signals to reach communications towers now beyond their range.

Paul Berger, Xia Jin (lead author) and their colleagues at Ohio State University in Columbus, Philip Thompson at the Naval Research Laboratory in Washington, D.C., and Roger Lake at the University of California at Riverside announced their world record in the Journal of Applied Physics Letters.

The researchers developed the diode with the support of the National Science Foundation (NSF), the independent federal agency that supports fundamental research and education across all fields of science and engineering.

Tunneling diodes have been around since the late 1950's when Leo Esaki, then at Sony Corp. in Japan, discovered that a property called tunneling can increase a diode's output current. Esaki later won the Nobel Prize, in part for this work.

Tunneling is a process that takes place at the level of the atom, in the realm of quantum physics. At that scale, the familiar rules of classical physics that guide rocket design, snowfall and baseball give way to less intuitive rules based on probability and energy packets.

Under the rules of quantum physics, an electron on one side of a barrier can travel through to the other side, "which would be like a tennis ball coming out the other side of a brick wall," says Berger. The property is called tunneling, and while somewhat mysterious, researchers have been taking advantage of the phenomenon for years, although only in niche applications.

By breaking the properties of semiconductors, researchers can create materials that increase the chances that tunneling will occur. Berger and his team have optimized the diode design and the process for creating the device with few imperfections. The researchers also developed a manufacturing process to create tunneling diodes that, in addition to being incredibly fast, are silicon-based and easy to mass produce.

The original tunnel diodes were difficult to mass produce and were not compatible with the silicon-based microchips that run

Si-Based RITDs (Berger)

March 11, 2005
Very Low Peak Current Densities

Current densities can be engineered over $\sim 7$ orders of magnitude by controlling RITD spacer thickness between the $\delta$-doping pair from 1 nm up to 16 nm.

By widening spacer, below 20 mA/cm² current density!

Low current densities valuable for memory and low power consumption.
Results highlighted here demonstrate the **highest reported peak current density** for Si-based interband tunnel diodes that is 3 times larger than the previous world **record**. A high current density is needed to generate **large amounts of microwave power output** for radio transmission in **small distributed sensor networks**.

Solid circles (●) indicate prior work by Berger group, open squares (□) indicate prior work by other groups, and stars (*) indicate recent work by Berger group.

Two NDR regions are achieved by vertically stacking 2 RITDs, being careful to minimize dopant segregation into top RITD.

Monolithic Integration of RITDs with CMOS

• In cooperation with Rochester Institute of Technology (RIT), RIT reports the first Si/SiGe RITDs are monolithically integrated with Si CMOS.

• Functional MOBILE latches are also realized.


Low Voltage Operation to Reduce Power Consumption
Voltage at sense node vs. applied clock voltage of a NMOS-RITDs MOBILE latch with 84% voltage swing of the applied $V_{CLK}$ at 0.5 V.
Integration of RITDs with SiGe HBTs

- The first Si/SiGe RITDs are monolithically integrated with SiGe heterojunction bipolar transistors (HBT) by vertically stacking the RITD atop the HBT.

Fig 1. Layer structure of the SiGe RITD with SiGe HBT.

- 100nm n+ Contact
- 2nm undoped Si
- 4nm undoped Si$_{0.6}$Ge$_{0.4}$
- 1nm p+ Si$_{0.6}$Ge$_{0.4}$
- 116nm p+ Si
- 48nm p++
- 50nm n++
- 75nm n+ Emitter (E')
- 15nm undoped Si$_{0.2}$Ge$_{0.8}$ Spacer
- 35nm p+ Si$_{0.2}$Ge$_{0.8}$
- 15nm undoped Si$_{0.2}$Ge$_{0.8}$ Spacer
- 5nm Si buffer
- 1850nm n- Collector
- 450nm n++ Si Sub-collector

p- substrate (resistivity of 2000 Ω-cm)

Fig 2. Band diagram of RITD / HBT.

HBT-RITD: Three Terminal NDR Device Provides Adjustable PVCR

Fig. 3. RITD and HBT emitter current load lines for fixed base current, \( I_B \). (a) Low \( I_B \) with bistable latching behavior. (b) Large \( I_B \) with infinite PVCR in \( I_C \).


Finalist for Best Student Paper Award!

Fig 4. I-V characteristics measured demonstrate PVCR, PCD and even the voltage span can be controlled.
**HBT-RITD: Latching Properties**

**Latch property: Bi-stability with** $I_B$ **between** $I_{\text{PEAK}}$ **and** $I_{\text{VALLEY}}$ **of RITD**

**Switching operation:**
- Low (B) $\rightarrow$ High (C) with the increase of $I_B$
- High (D) $\rightarrow$ Low (A) with the decrease of $I_B$

Multi-valued Quantum Logic For Compact and Energy Efficient Circuitry

Reduced device count potential.

However, there is a large series resistance created by the vertical stacking and a lower noise margin from P2 → P3 than P1 → P2

Multi-valued Quantum Logic For Compact and Energy Efficient Circuitry

- The large peak voltage shift observed earlier in vertically integrated RITD pairs is now greatly reduced. No hysteresis was observed in the NDR region.
- Large peak current and valley current differences were observed, which makes the modified RITD pair more suitable for circuit implementation using a constant-current-source load.
- The upper diode shows a PVCR of 3.5 with $J_p$ of 155 A/cm$^2$, and the lower diode shows a PVCR of 3.6 with $J_p$ of 515 A/cm$^2$.

**Improved operational voltage and increased noise margin**

Key Results of Our Effort

• Demonstration of **room temperature NDR** in **epitaxially grown** families of Si-based tunnel diodes.

• Devices have shown **PVCRs up to 3.8** and the peak current density can be engineered from **high current densities** (\( \geq 150 \text{ kA/cm}^2 \)) to **low current densities** (\( \leq 20 \text{ mA/cm}^2 \)).

• **Si-based RITDs** have been monolithically integrated with CMOS and SiGe HBT processing for **efficient and low power consumption circuitry**.
Si-Based RITD Results Summary

**Device Optimization**
- High PVCR (3.8)
- High PCD (≥ 150 kA/cm²)
- Low PCD (≤ 20 mA/cm²)

**Device Integration**
- Monolithic integration with CMOS
- Monolithic Integration with SiGe HBTs

**Hybrid Circuit Prototyping**
- Vertically stacked back-to-back RITDs for symmetric NDR
- Tri-state logic with vertically stacked RITDs
- Low voltage MOBILE latches (CMOS-RITD)
- Adjustable PVCR (HBT-RITD)

March 11, 2005
For Further Reading


