Strain engineered Si/SiGe resonant interband tunneling diodes with outside barriers grown on $Si_{0.8}Ge_{0.2}$ virtual substrates

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(Received 31 July 2008; accepted 20 August 2008; published online 11 September 2008)

Si-based resonant interband tunneling diodes (RITDs) grown on commercially available $Si_{0.8}Ge_{0.2}$ virtual substrates were studied. Peak-to-valley current ratios (PVCRs) were improved by utilizing strain induced band offsets to 3.5 with a peak current density (J_p) of 161 A/cm^2. More specifically, a tensilely strained Si layer on the *p*-side and a compressively strained $Si_{0.5}Ge_{0.5}$ layer on the *n*-side were added to the design to form enhanced potential barriers away from the tunneling junction. The outside barriers deepen the respective hole and electron quantum wells and also block nonresonant tunneling current, which improved the PVCR significantly. However, due to the large surface roughness of the SiGe virtual substrates used in this study, the RITDs grown on $Si_{0.8}Ge_{0.2}$ substrates exhibit a smaller PVCR overall than RITDs optimized on standard Si substrates. Better performance is expected by using higher quality SiGe substrates with smaller surface roughness. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2981211]

Si-based resonant interband tunneling diodes (RITD) grown by low temperature molecular beam epitaxy (MBE) were first demonstrated by Rommel *et al.*[1] Since then, numerous studies have been carried out to improve their dc/rf performance (Refs. 2 and 3, and references therein) as well as realize monolithic integrations of RITDs with HBTs (Ref. 4) and complementary metal-oxide semiconductor.[5] Strain induced band offset changes in the Si/SiGe system was documented by People and Bean in 1986.[6] This discovery led to tremendous flexibility in Si-based device design and has given rise to a number of novel devices, such as modulation-doped field effect transistors,[7] and resonant tunneling diodes.[8] Recently, we reported a strained RITD grown on commercially available $Si_{0.8}Ge_{0.2}$ virtual substrates with tensilely strained Si layers cladding the P δ-doping plane, which showed superior performance than its counterpart.[9] The added Si cladding was attributed with deepening the *n*-type quantum well (QW) and suppressing vacancy-mediated outdiffusion. In this letter, we report strain engineered Si-based RITDs grown on virtual $Si_{0.8}Ge_{0.2}$ substrates with additional outside tunneling barriers. This approach was similarly employed in III-V double QW RITDs to block the nonresonant tunneling current component and hence improve the peak-to-valley current ratio (PVCR).[10] Strain engineering atop SiGe virtual substrates permits great flexibility in tailoring the Si/SiGe band diagram by inverting the strain component, which is not permissible on Si substrates alone. The measured results show significant performance improvements in Si-based RITDs are possible with SiGe virtual substrates.

The commercial *p*-type $Si_{0.8}Ge_{0.2}$ virtual substrates were grown on Si substrates (Boron doped, 0.010–0.015 Ω cm) by the chemical vapor deposition (CVD) technique. The CVD epilayers consist of 0.5 μm Si buffer layer (*p*-type doping $>7\times10^{17}$ cm^{-3}), 2 μm graded SiGe layer (*p*-type doping $>7\times10^{17}$ cm^{-3}), 1.2 μm $Si_{0.8}Ge_{0.2}$ uniform layer (*p*-type doping $<1\times10^{15}$ cm^{-3}), and a 17.5 nm Si cap layer (*p*-type doping $>1\times10^{15}$ cm^{-3}). The SiGe uniform cap relaxation is greater than 98%. The total threading dislocations is expected to be less than 2×10^{6} cm^{-2}. The RITD structures were grown on *p*-type $Si_{0.8}Ge_{0.2}$ virtual substrates with a MBE growth system using elemental Si and Ge in electron-beam sources. The doping level for both n^+ and p^+ injector layers is nominally 5×10^{19} cm^{-3}, while both the B and P δ-doping sheet carrier concentrations were targeted at 1×10^{14} cm^{-2}. Prior to device fabrication, portions of the as-grown wafers were annealed using a forming gas ambient (N_2/H_2) in a Modular Process Technology Corporation RTP-600S furnace at various temperatures for 1 min. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography to permit a top contact. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO_3 wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was also evaporated on all of the samples to complete the device fabrication.

Previous reports of III-V double QW RITDs utilized outside barriers to effectively block the nonresonant tunneling current component and hence improve the measured PVCR.[10] The use of a $Si_{0.8}Ge_{0.2}$ virtual substrate enables the introduction of outside barriers by employing strain induced band offsets. Two epilayer structures were designed to study the effect of these outside barriers. The control structure (structure A) is shown in Fig. 1(a), which is actually quite similar to the recently reported structure with Si layers cladding the P δ-doping layer,[9] except for a small modification to

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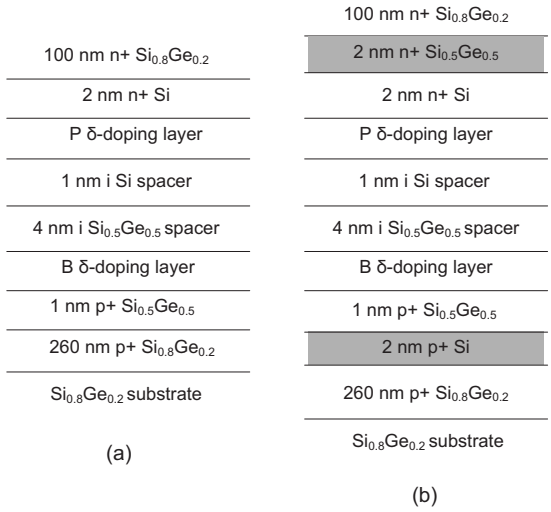

FIG. 1. Schematic of RITDs grown on $Si_{0.8}Ge_{0.2}$ substrates. (a) Structure A, the control RITD. (b) Structure B, a strained RITD with outside barriers included. The additional strained outside barrier layers are shaded.

the overall tunnel spacer thickness (6 to 5 nm) and the Ge percentage was reduced (60% to 50%). In structure B, shown in Fig. 1(b), outside barriers are formed by a 2 nm tensilely strained Si layer on the *p*-side and a 2 nm compressively strained $Si_{0.5}Ge_{0.5}$ layer on the *n*-side. The band diagram is calculated using a one-dimensional Poisson–Schrödinger solver that self-consistently obtains the solution to the Poisson–Schrödinger equations with a finite-difference method and a nonuniform mesh size.[11,12] Calculated band parameters for energy band gap, band offsets, and effective mass of strained $Si_{1-x}Ge_x$ on relaxed $Si_{1-y}Ge_y$ substrate[13] were used for the simulation. The calculated band diagrams are plotted in Fig. 2. Structure A includes a strain induced conduction band discontinuity, ΔE_c, and strain induced valence band discontinuity, ΔE_v, of 0.2 eV, respectively, pointed away from the tunneling junction. Structure B, however, enhances these barriers with ΔE_c rising to 0.28 eV and ΔE_v climbing to 0.26 eV, as shown in Fig. 2(b). The outside barriers block the nonresonant tunneling component, often termed the excess current, by increasing its effective tunneling barrier width.[10] Excess current is a major contributor to the valley current[14] and therefore suppresses PVCR. Furthermore, the outside barriers also deepen the QW, so that a more well-defined quantum state is achieved and more free carriers can accumulate that contribute to and elevate the tunneling current. For instance, modeling each δ-doping region as a 1 nm thick slab doped at 10^{21} cm^{-3} results in two confined electron eigenstates for structure A residing at −111 and 27.8 meV in Fig. 2(a). In contrast, structure B indicates a third electron state is created, with eigenstates residing at −111, 27.3, and 156 meV in Fig. 2(b).

Figure 3(a) clearly shows that the measured peak current densities (J_p) of structure B with the outside barriers annealed at various temperatures are significantly higher than the control sample, structure A, while the valley current densities of structure B are also lower than the control. The increased peak current density and decreased valley current density affirm that the outside barriers both deepen the QW to accumulate more charge for band-to-band tunneling while effectively blocking a portion of the nonresonant tunneling current. As a result, the PVCR of RITDs with outside barriers (structure B) are significantly higher than for the control RITDs, (structure A), as shown in Fig. 3(b). The highest recorded PVCR of 3.5 (J_p=161 A/cm^2) for structure B was obtained using an 825 °C RTA annealing for 1 min, while the comparator, structure A, exhibited a PVCR of only 2.8 (J_p=155 A/cm^2). Structure B also exhibits a seemingly greater robustness to thermal cycling, recording a PVCR of 2.7 with an 835 °C RTA annealing for 1 min, while structure A plummeted to a PVCR of 1.6. All electrical measurements were performed at room temperature.

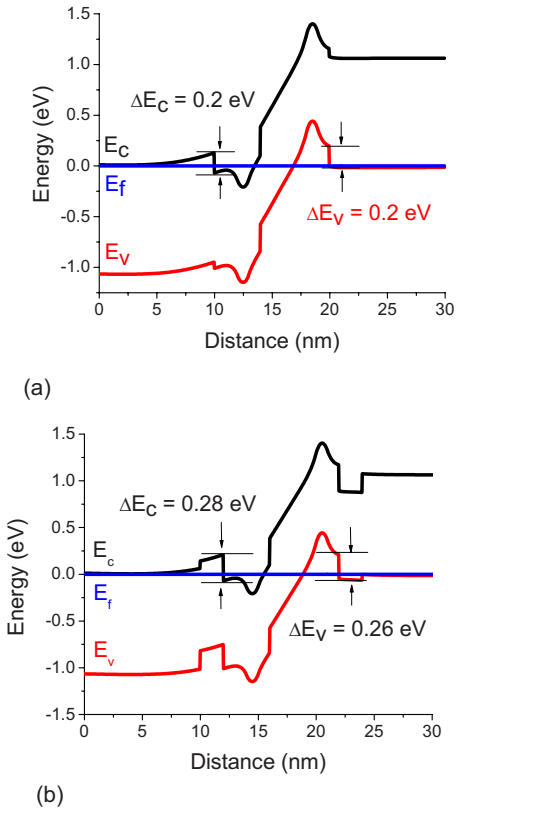

FIG. 2. (Color online) The calculated band diagrams of structures A and B examined in this study. The conduction and valence band QW offsets are illustrated for clarity.

Structure B, with outside tunneling barriers, shows improvement over its control sample. Although its PVCR, 3.5, is the highest achieved on a $Si_{0.8}Ge_{0.2}$ substrate, which is

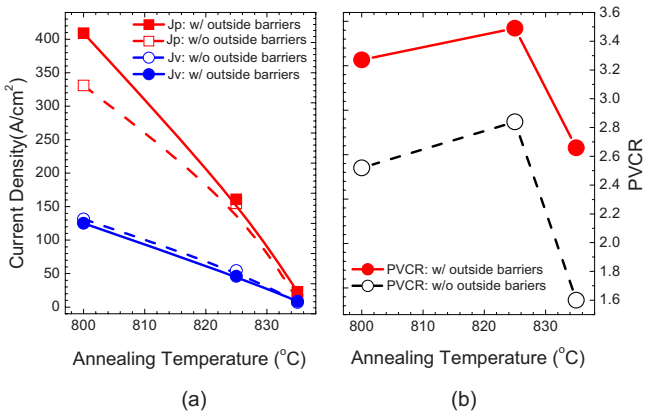

FIG. 3. (Color online) A comparison of the measured room-temperature PVCR performance of representative RITDs both with and without outside barriers, structures A and B, respectively.

significantly higher than previous reports of strained SiGe PVCR of 1.36 (J_p=1.8 A/cm^2) using a higher 30% Ge virtual SiGe substrate,[15] it is slightly lower than the PVCR of 3.6 (J_p=300 A/cm^2). reported for an equivalent RITD grown on a Si substrate.[2] The suppressed overall performance of all the strained RITDs developed on $Si_{0.8}Ge_{0.2}$ virtual substrates[9] is attributed to the modest quality of their dislocation engineering and residual surface roughness.

The clearly evident cross-hatching pattern on the wafer surface of the epitaxially grown RITD is indicative of a large surface roughness. Atomic force microscopy (AFM) was used to characterize the surface roughness before and after the MBE growth. The AFM data for the RITDs grown on Si and $Si_{0.8}Ge_{0.2}$ substrate, respectively, showed that the R_{max} (peak-to-peak magnitude) and root mean square surface roughness of RITDs on a Si substrate are about 8.5 and 1.9 nm, respectively, while these values increased to 35.1 and 7.2 nm for RITDs on $Si_{0.8}Ge_{0.2}$ substrate over a scan range of a 10×10 μm^2 square region. Note that the total thickness of the active RITD structure is only about 6–10 nm, which is much smaller than the peak-to-peak roughness of the RITD on the $Si_{0.8}Ge_{0.2}$ substrate. It is not surprising that the overall device performance is significantly degraded compared to previous reports on conventional Si (100) substrates. A much higher PVCR should be possible if the RITDs were grown on higher quality SiGe substrates with smaller surface roughness.

In conclusion, strained Si-based RITDs grown on commercially available $Si_{0.8}Ge_{0.2}$ virtual substrates were realized that incorporated outside tunneling barriers that effectively deepen the QWs and block the nonresonant tunneling current, hence improving PVCR by increasing the peak current density and suppressing the valley current density simultaneously. However, due to the large surface roughness of the SiGe substrates used here, the RITDs grown on SiGe substrate exhibit inferior performance to RITDs grown on conventional Si substrates. Better performance is expected by using higher quality SiGe substrates.

The Ohio State University was supported by the National Science Foundation (DMR-0103248 and ECS-0323657). The work at NRL was supported by the Office of Naval Research.

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