

Xilinx ISE 9.1i Getting Start Tutorial

1. Starting the ISE Software

To start ISE, double-click the desktop icon,



or start ISE from the Start menu by selecting:

Start → **All Programs** → **Xilinx ISE 9.1i** → **Project Navigator**

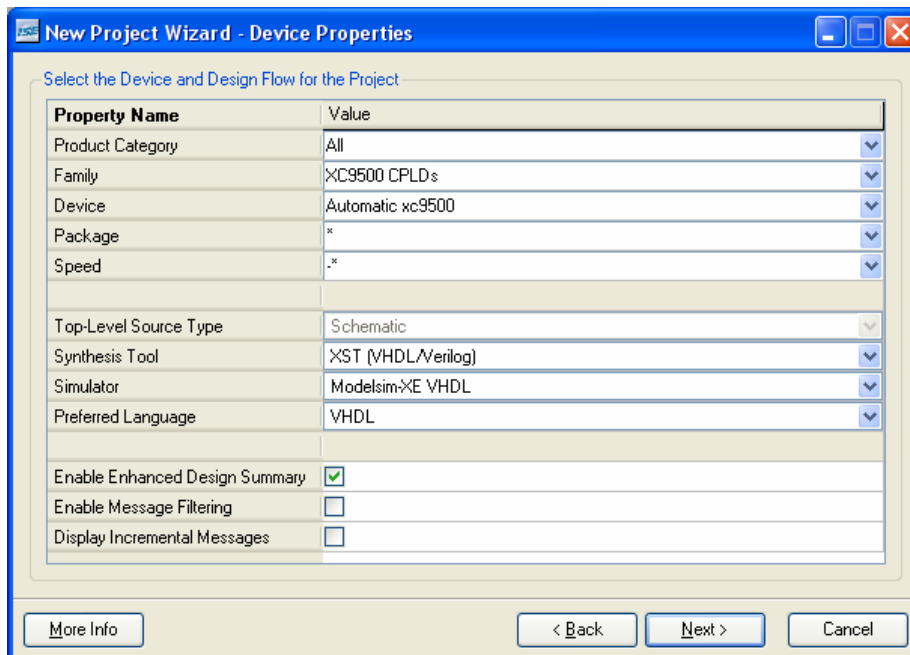
Note: Your start-up path is set during the installation process and may differ from the one above.

2. Create a New Project

Create a new ISE project which will target the CPLD device

To create a new project:

1. Select **File** > **New Project...** The New Project Wizard appears.
2. Type **tutorial** in the Project Name field.
3. Enter or browse to a location (directory path) for the new project. A tutorial subdirectory is created automatically.
4. Verify that **Schematic** is selected from the Top-Level Source Type list.
5. Click **Next** to move to the device properties page.
6. Leave the default options in the device properties page as shown below.

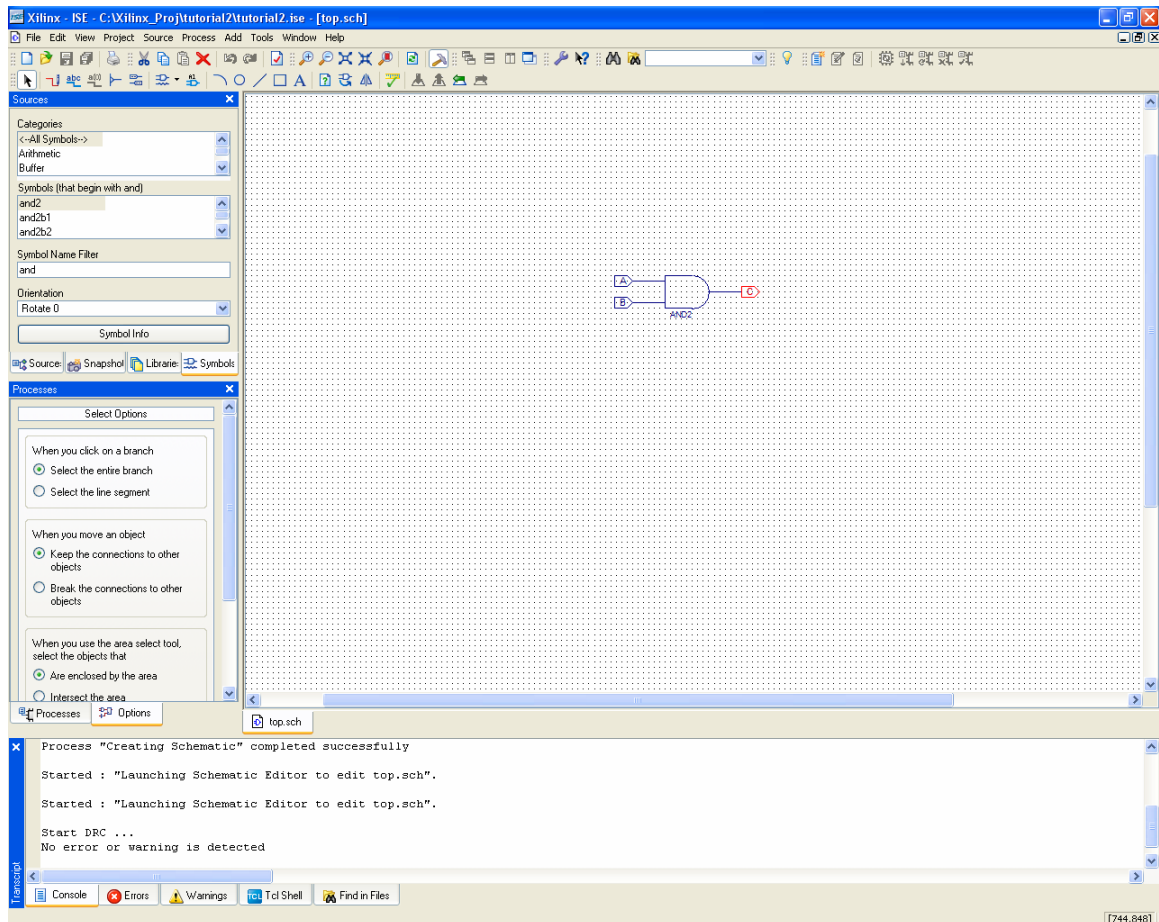


7. Continue clicking **Next** to proceed to the Create New Source window in the New Project Wizard. At the end of the next section, your new project will be complete.

3. Create a Schematic Source

Create a Schematic source file for the project as follows:

1. Click the **New Source** button in the New Project Wizard.
2. Select **Schematic** as the source type.
3. Type in the file name **top**.
4. Verify that the **Add to project** checkbox is selected.
5. Click **Next**.
6. Click **Finish** in the New Source Wizard - Summary dialog box to complete the new source file template.
7. In Schematic window, select Add → Symbol to bring up symbol library.
8. Connect input/output ports to the circuit.
9. After complete the circuit, click on Tools → Check Schematic to verify the circuit.
10. Save the file by selecting File → Save.

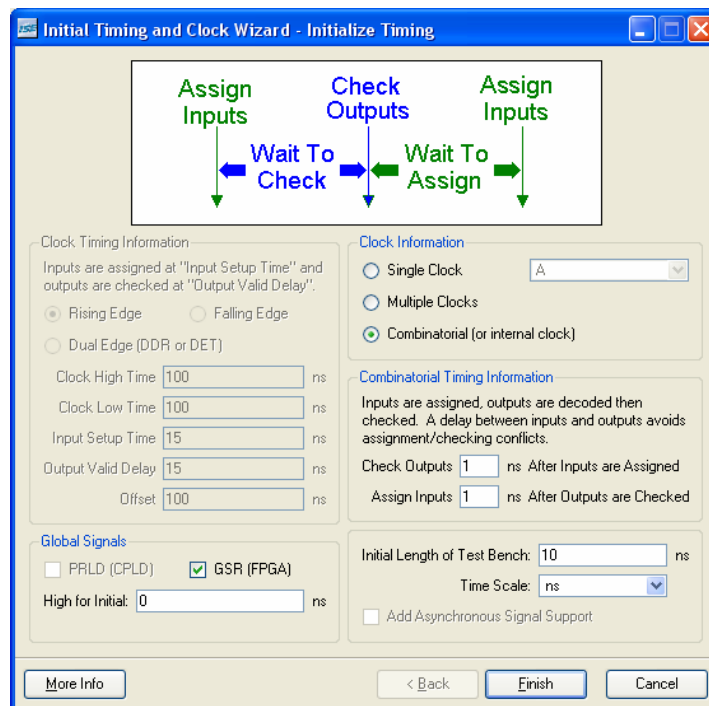


4. Design Simulation

Create a test bench waveform containing input stimulus you can use to verify the functionality of the top schematic. The test bench waveform is a graphical view of a test bench.

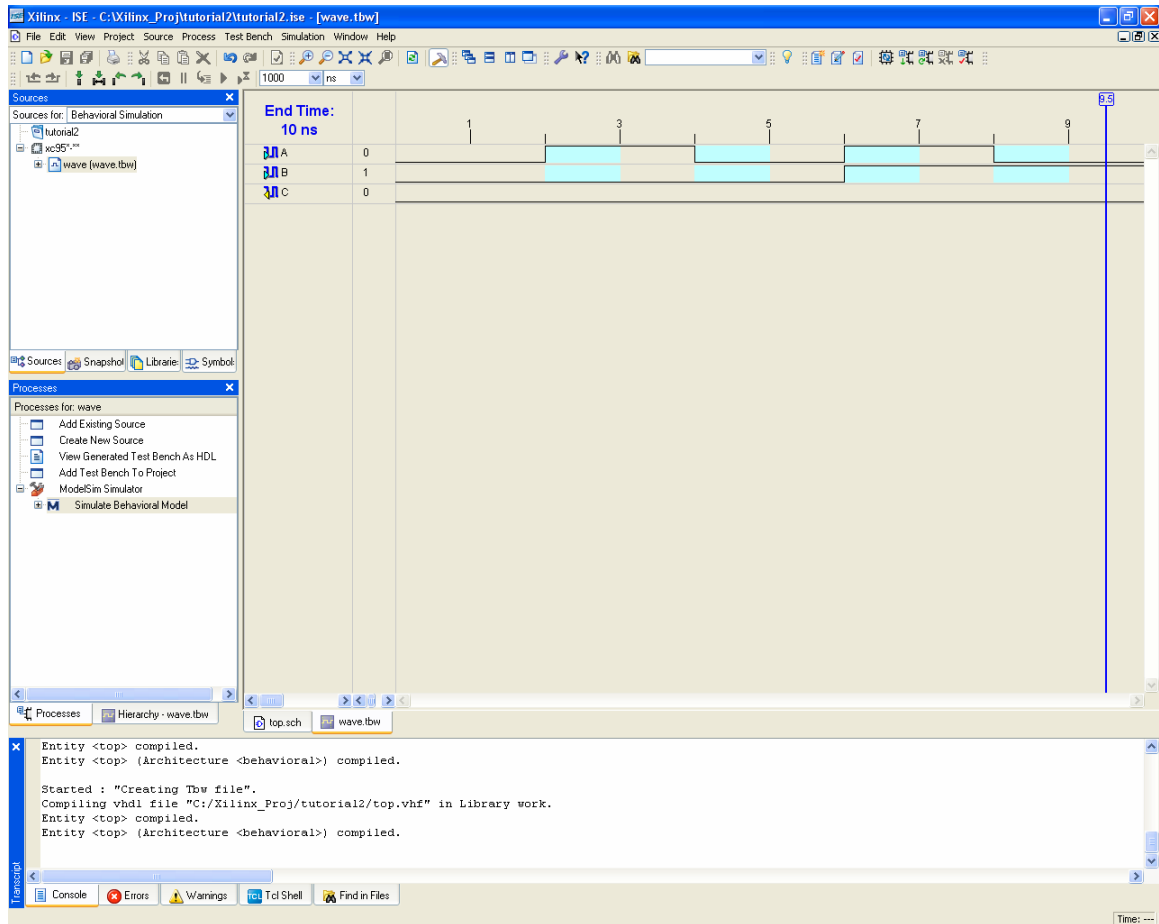
Create the test bench waveform as follows:

1. Select the **top** schematic file in the Sources window.
2. Create a new test bench source by selecting **Project** → **New Source**.
3. In the New Source Wizard, select **Test Bench WaveForm** as the source type, and type **wave** in the File Name field.
4. Click **Next**.
5. The Associated Source page shows that you are associating the test bench waveform with the source file **top**. Click **Next**.
6. The Summary page shows that the source will be added to the project, and it displays the source directory, type and name. Click **Finish**.
7. Since this project simulates the **and** gate, you need to set **Clock Information** as *Combinatorial*, **High for Initial** to 0 ns, and **Combinatorial Timing Information** in the Initialize Timing dialog box as shown below.



8. Click **Finish** to complete the timing initialization.
9. Click on blue shade in the waveform window to assert the signals.
10. Save the waveform.
11. In the Sources window, select the **Behavioral Simulation** view to see that the test bench waveform file is automatically added to your project.

Simulating Design Functionality



Verify that the counter design functions as you expect by performing behavior simulation as follows:

1. Verify that **Behavioral Simulation** and **wave** are selected in the Sources window.
2. In the **Processes** tab, click the “+” to expand the Xilinx ISE Simulator process
3. To change the default Simulation Run Time, select **Simulate Behavioral Model** → **Properties...**
4. To simulate the circuit, double-click on the **Simulate Behavioral Model** process.

The ISE Simulator opens and runs the simulation to the end of the test bench.

5. To view your simulation results, select the **wave - default** tab and right click for zoom full.