

Tutorial: Using *Xilinx ISE 10.1* for State Machine Based Design

Xilinx includes StateCAD software that allows a state machine to be specified graphically, and then translated into the appropriate VHDL/ABEL/Verilog design language. This tutorial outlines the technique. In addition, you will learn to test the functional design by using HDL Benchner and *ModelSim*.

Introduction

As an example, we will use a simple Moore machine. This machine has four states **S00**, **S01**, **S10**, **S11**, an input **MODE**, and a Moore-type output **DIFF** that is asserted if **MODE** has held two different values at the two previous triggering edges of the clock. The states are named suggestively; S_{ij} is the state you are in if **MODE** had the value j at the previous triggering edge and a value of i at the edge before that. Clearly, the Moore-type output **DIFF** is asserted when we are in state **S01** or **S10**, and is not asserted otherwise.

Table 1 shows the state table for our state machine. Figure 1 shows the final state diagram in a StateCAD window.

Input MODE	Current State	Next State	Output DIFF
0	S00	S00	0
0	S01	S10	1
0	S10	S00	1
0	S11	S10	0
1	S00	S01	0
1	S01	S11	1
1	S10	S01	1
1	S11	S11	0

Table 1: State Table

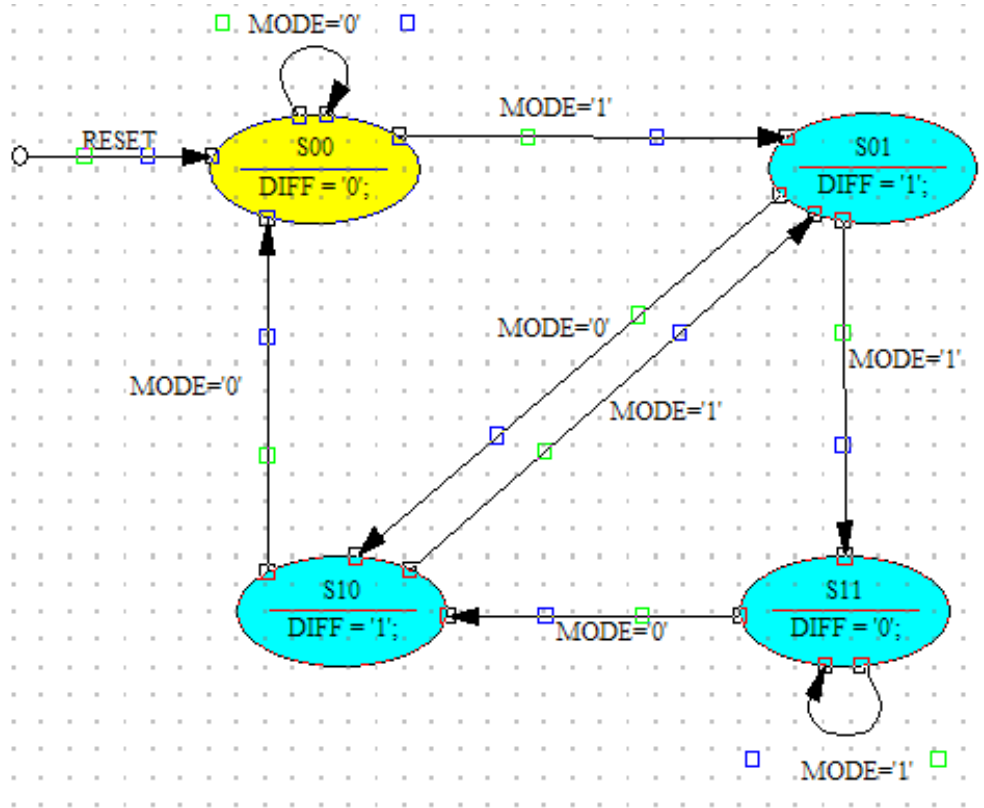


Figure 1: Final State Diagram

Step 1 – Starting *Xilinx ISE* and Opening a New Project

To start the *Xilinx ISE* tools, click on Start → Programs → Xilinx ISE Design Suite 10.1 → ISE → Project Navigator. In the Project Navigator window, click on File → New Project. This will bring up a New Project window. In the *Project Name* field, type *SM_tut*. Specify *HDL* as the *Top-Level Module Type*. After clicking *Next*, specify *XC9500 CPLDs* as the *Device Family* and *XST (VHDL/Verilog)* as your *Synthesis Tool* from the pull-down menus, and *VHDL* as the *Preferred Language*. We will not create new sources for this project at this point. Continue clicking *Next*, *Next* and then *Finish* to end the new project setup process.

Step 2 – Create the State Diagram using StateCAD

To create new source, click on Project → New Source. In the pop-up window, select the entry *State Diagram* and give the name *sim_sm.dia* in the *File Name* field. Click *Next* and in the next window click *Finish*. If a pop-up window opens, select *Yes* to view the tutorial and close the tutorial window. Once you do that a blank State Diagram window (Figure 2) will open.

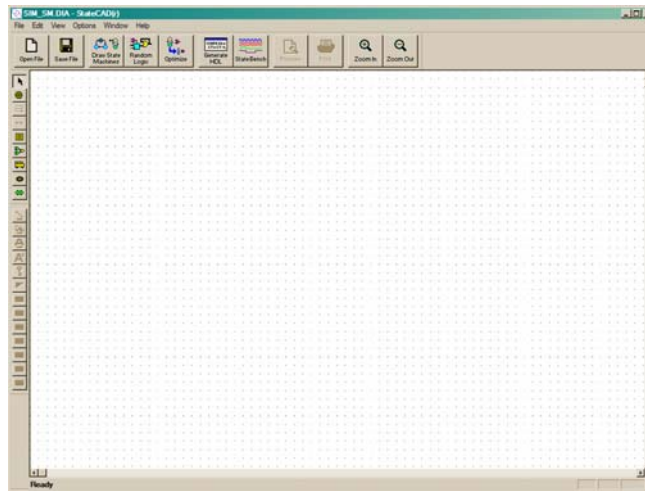



Figure 2: StateCAD diagram window

Click on the *Draw State Machines* button  on the toolbar. For ECE lab users, click on Select File → Design Wizard. Answer *Yes* for using current diagram. Click *Next* to continue. You should have the template state diagram. This will open the State Machine Wizard window (Figure 3). Select *Geometric* for the *Shape of state machine* and *4* for *Number of states*, and then click *Next*.

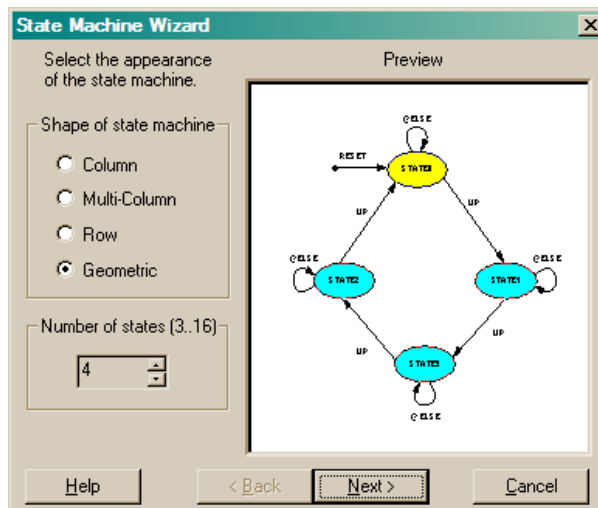


Figure 3: State Machine Wizard

Select *Asynchronous* as the Reset Mode. Click on *Next*. To set up the transitions from one state to another, select both the *Loop back* and *Next* options in the Setup Transitions window (Figure 4). Click on *Finish* to create the template state diagram. Or if you are in Optimization Wizard window, click *Cancel* to finish the Design Wizard

process. If system error [275] occurs, visit FAQ Q6 on ECE Xilinx website.
<http://www.ece.osu.edu/xilinx/faq.html>.

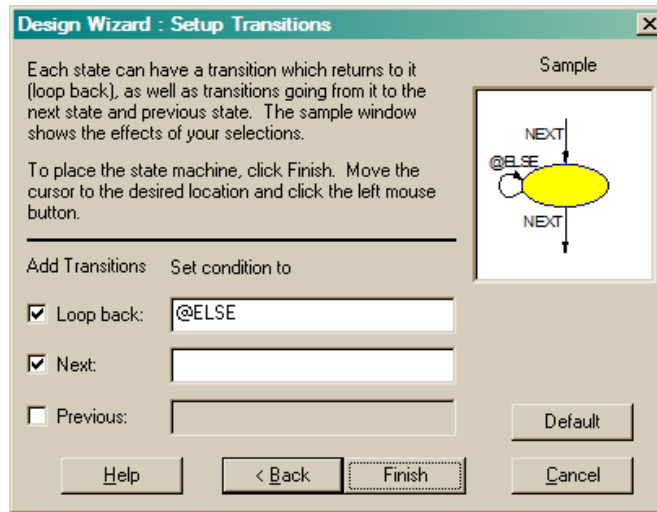


Figure 4: Setup Transitions window

Place the template state diagram onto the blank state diagram window by left clicking anywhere on the blank diagram (Figure 5).

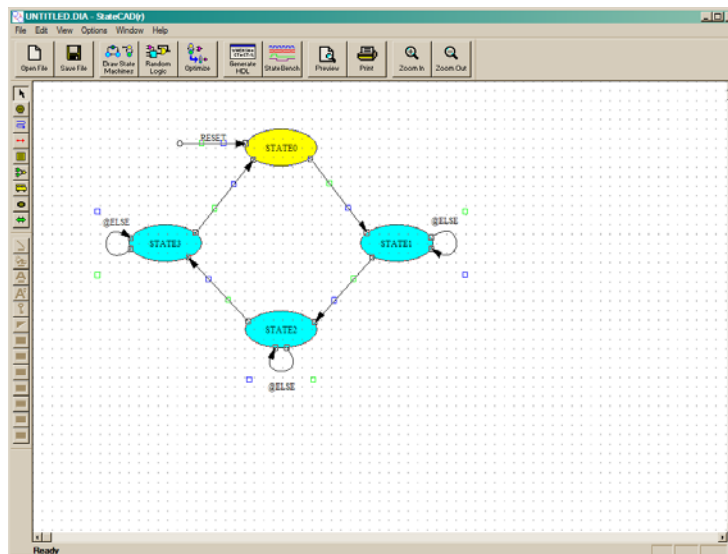


Figure 5: Template State Diagram

Now that the template is in place, you can add/remove/modify the states for correct transitions and positions. To position the states STATE0 into a square form, hold down the left mouse button and move it accordingly. All the transition connections will also move with it. Delete the loop back on STATE1 and STATE3. Position a transition link by clicking and dragging the small box at the end of the transition arrow. See Figure 6.

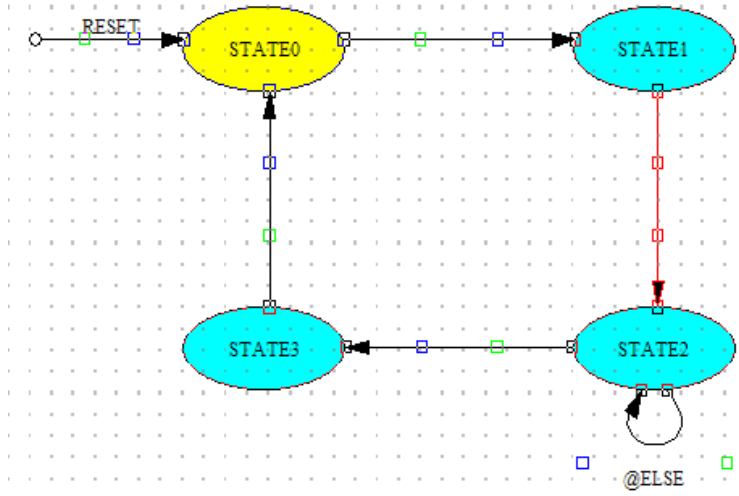



Figure 6: Reposition the States

Double click **STATE0** and change the state name to **S00**; then **STATE1** to **S01**, **STATE2** to **S11**, and **STATE3** to **S10**.

Now we are ready to add the transition links. Click on *Add-Transition* button  in the left toolbar. The mouse point will change to the Add-Transition mode. To create the loop back transition at **S00**, click on the state **S00** twice. The loop back link should appear. You can also draw it manually. However, it is more difficult than drawing a straight-line transition link. Next, draw the transition links between **S01** and **S10** by left-clicking at the edge of the state circle.

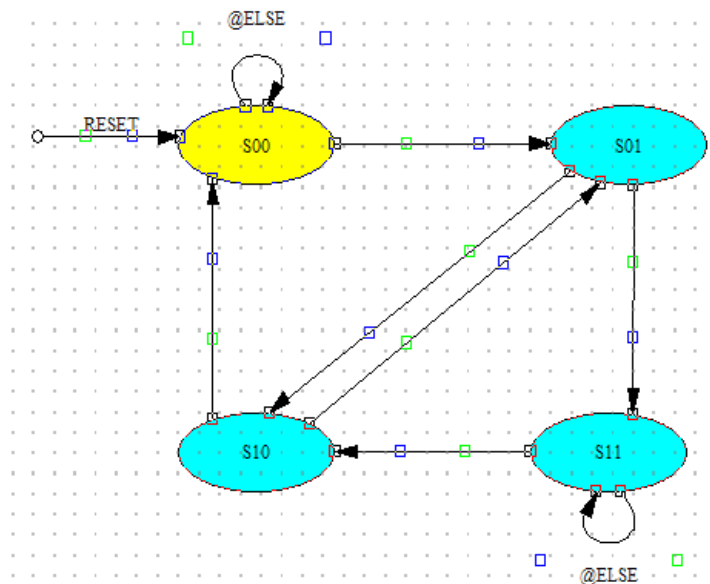


Figure 7: Rename the States and Add the Transition Links

Now left click on one of the two boxes on the transition link **S00** → **S01**. The pop-up Edit Condition window will open (Figure 8). Add the condition *MODE='1'* in the *Condition* field. Follow the state assignment in Table 1 or Figure 1 to assign all transition links.

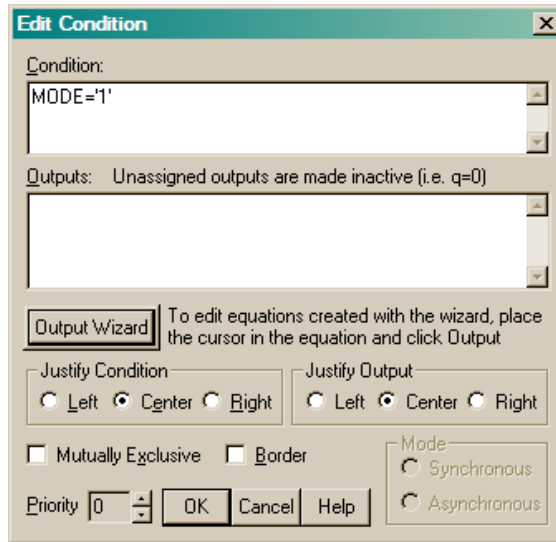


Figure 8: Edit Condition window

Next assign the output of each state by first double-clicking on **S00**. Click on the *Output Wizard* button. Select **0** in the *Constant* box and type **DIFF** in the *DOUT* box. Set the *Data path width* to 1 (Figure 9). Click on *OK*.

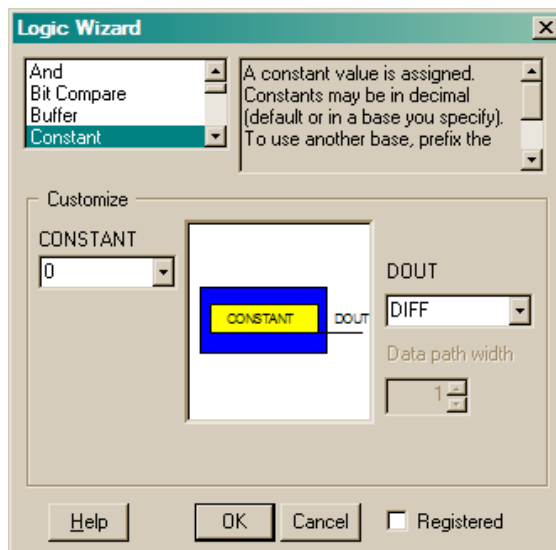



Figure 9: Output Logic Wizard

The final state diagram is shown in Figure 1. You will need to move the transition texts around to make it readable and organized. Save your final diagram.

Once the diagram is complete, we can export it to VHDL code. Click on the *Generate HDL* button . A pop-up window will appear with the output, **DIFF**, in the list of possible outputs to be registered. The “X” mark on the left of **DIFF** indicates that **DIFF** is the selected output. Click on the *Optimize* button. A successful Results window (Figure 10) is shown. Click on the *Close* button. This will bring up the VHDL source code window. Now you can exit the StateCAD program. If system error [62] occurs, ignore the error message and continue on Step 3.

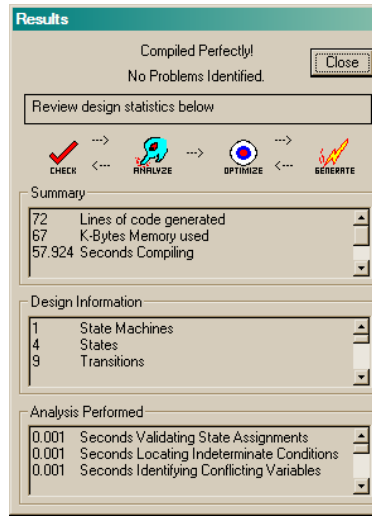


Figure 10: Results window

Step 3 – Add the VHDL Source File to the Project

Now the VHDL file has been created. In order to test the functionalities of our state machine, we will need to add the VHDL source code to our *SM_tut* project. In the Project Navigator window, click **Project** → **Add Source**. Select *SIM_SM.vhd* as the source. In the *Choose Source Type* window, select *VHDL Design file* and click **OK**. You should see *SIM_SM.vhd* in the *Sources in Project* window. Double click to open up the VHDL source code in the working window. In the same convention, you should be able to add the state diagram *sim_sm.dia* to the project file.

Step 4 – Generate the Test bench Using HDL Bencher and Simulate the Design Functionality

Next we will need to create the test bench waveform. To create the waveform in HDL Bencher, click **Project** → **New Source**. Select *Test Bench Waveform* and type *wave* in the *File Name* field. In the Select window, you should see *sim_sm*. Click **Next** and **Finish**. In the Initialize Timing window, select the *Design Type* option as *Single Clock*. You can keep the default parameter values as shown in Figure 11. After checking the parameters, click **OK**.

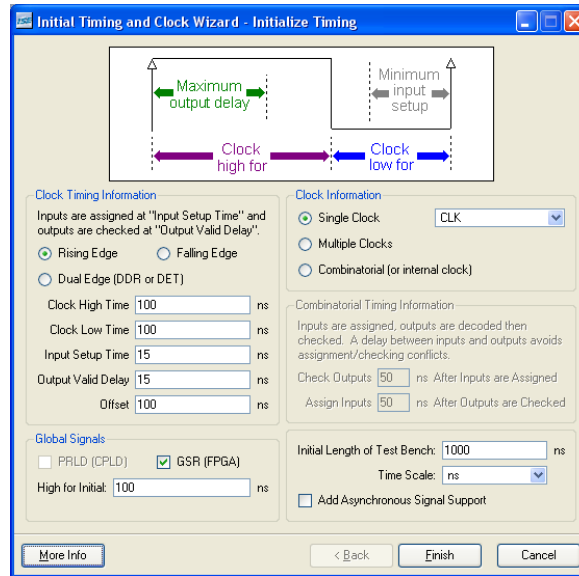


Figure 11: Initialize Timing window

In the HDL Bencher window, toggle **RESET** to high for about 1 clock periods. Then toggle it back to low for the rest of the simulation. This will set the state to **S00**. Write down the input sequence that you want to test. You can toggle the input **MODE** up and down following your sequence. Figure 12 shows an example of an input sequence.

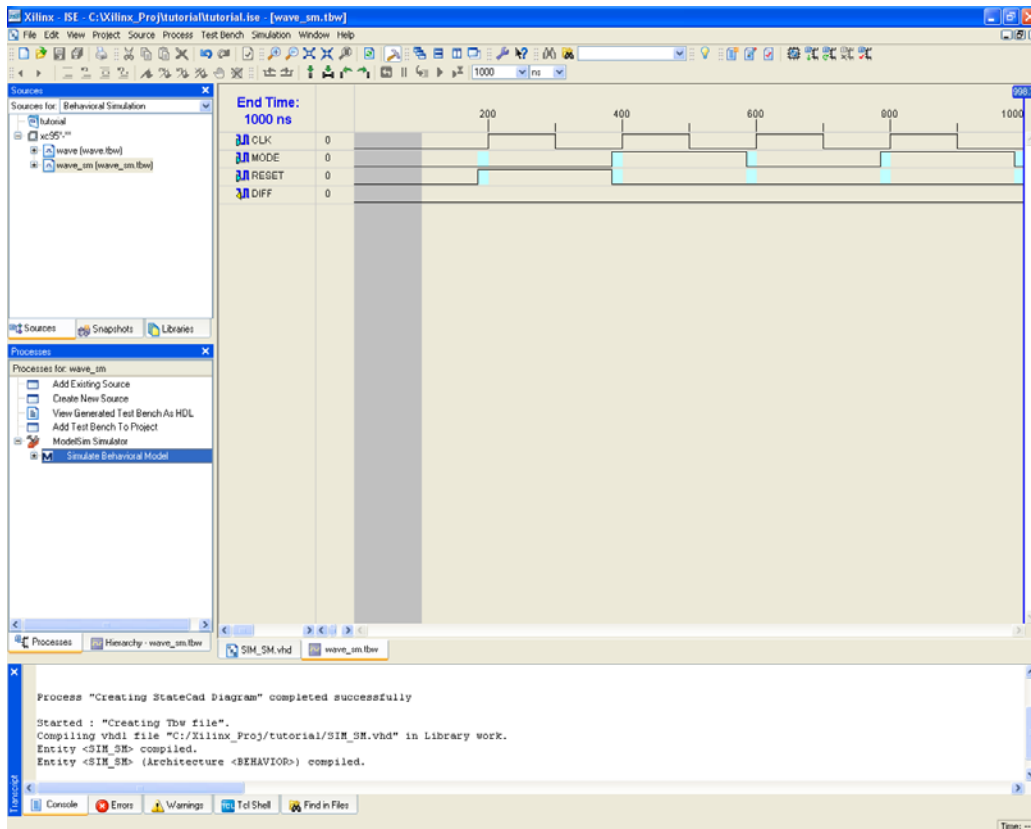


Figure 12: Waveform Output