

ECE Distinguished Seminar Series

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Advanced Si Nanotechnology and Emerging Non-Si Nanoelectronic Devices for High-Performance and Low-Power Logic Applications

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Abstract: Moore's Law states that the number of transistors per integrated circuit doubles every 24 months, and it has been the guiding principle for the semiconductor industry for more than 30 years. The sustaining of Moore's Law, however, requires continual transistor miniaturization and performance improvement. The physical gate length of the Si transistors used in the current 90nm logic generation node is about 50nm, and it is projected that the size of the transistors will reach about 10nm in 2011. Through silicon innovations such as strained-Si channels, high-K/metal-gate stacks, and the non-planar "Tri-gate" CMOS transistor architecture, CMOS transistor scaling and Moore's Law will continue at least through the middle of the next decade. By combining silicon innovations with other non-Si nanotechnologies on the same silicon platform, it is expected that Moore's Law will extend well into the next decade. Recently much progress has been made in the research of non-Si nanotechnology for future nanoelectronics applications. In particular, several emerging nanoelectronic devices such as carbon-nanotube field effect transistor (FET), semiconductor-nanowire FET, and planar III-V compound semiconductor FET, all hold promise as device candidates to be integrated onto the silicon platform for enhancing circuit functionality and for extending Moore's Law. This presentation will describe the most recent advances made in Si CMOS transistor technology, plus the challenges and opportunities presented by the recent emerging nanoelectronic devices for high-performance, low-power logic applications. A new benchmarking methodology to benchmark emerging nanoelectronic devices versus state-of-the-art Si CMOS transistors for high-performance, low-power logic CMOS applications will also be presented.

Biography: Dr. Robert Chau is an Intel Fellow and Director of Transistor Research and Nanotechnology at Intel Corporation. He is responsible for directing research and development in advanced transistors and gate dielectrics for next- and future-generation microprocessors. He is also leading Intel research efforts in emerging nanotechnologies for future device and process applications. Dr. Chau received the B.S., M.S., and Ph.D. degrees in electrical engineering from The Ohio State University. He joined Intel in 1989 and has developed seven generations of Intel gate dielectrics, plus many CMOS transistor innovations used in various Intel manufacturing processes and microprocessor products. Dr. Chau has received 6 Intel Achievement Awards and 13 Intel Logic Technology Development Division Recognition Awards for his research breakthroughs and outstanding technical achievements, and currently holds 52 United States patents in device and process technologies. Dr. Chau has also received the 2003 Alumni Professional Achievement Award from The Ohio State University Alumni Association. He was recognized by IndustryWeek in 2003 as one of the 16 "R&D Stars" in the United States who "continue to push the boundaries of technical and scientific achievement." Dr. Chau is an IEEE Fellow.

