ECE Distinguished Seminar Series

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Prof. Jesús A. del Alamo
M.I.T.

Webinar:

Nanometer Scale III-V CMOS

Abstract: In the last few years, as Si electronics faces mounting difficulties to maintain its historical scaling path, transistors based on III-V compound semiconductors have emerged as a credible alternative. To get to this point, fundamental technical problems had to be solved though there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. Among them, harnessing the outstanding electron transport properties of InGaAs, the leading n-channel material candidate, towards a high-performance nanoscale MOSFET has proven difficult; contact resistance, offstate characteristics, reliability and Si integration remain serious problems. Introducing a new material system is not the only challenge. Scalability to sub-10 nm gate dimensions also demands a new 3D transistor geometry. InGaAs FinFETs, Trigate MOSFETs and Nanowire MOSFETs have all been demonstrated but their performance is still disappointing. To compound the challenge, a high-performance nanoscale p-type transistor is also required. Among III-Vs, InGaSb is the most promising candidate. Planar MOSFETs have been demonstrated but more advanced geometries remain elusive. This talk will review recent progress as well as challenges confronting III-V electronics for future CMOS logic applications.

Bio: Jesús del Alamo is Director of the Microsystems Technology Laboratories, Donner Professor, and Professor of Electrical Engineering in the Department of Electrical Engineering and Computer Science at MIT.

He holds degrees from Polytechnic University of Madrid (Telecommunications Engineer, 1980), and Stanford University (MS EE, 1983 and PhD EE, 1985). From 1977 to 1981 he was with the Institute of Solar Energy of the Polytechnic University of Madrid, investigating silicon photovoltaics. From 1981 to 1985, he carried out his PhD dissertation at Stanford University on minority carrier transport in heavily doped silicon. From 1985 to 1988 he was research engineer with NTT LSI Laboratories in Atsugi (Japan) where he conducted research on III-V heterostructure field-effect transistors. He joined MIT in 1988. From 1991 to 1996, Prof. del Alamo was an National Science Foundation Presidential Young Investigator. In 1999 he was elected a corresponding member of the Royal Spanish Academy of Engineering. In 2005, he was elected a Fellow of the IEEE and in 2014 he was elected a Fellow of the American Physical Society. Among other activities, Prof. del Alamo was Editor of IEEE Electron Device Letters from 2005 to 2014 and since 2013 he is the Director of the Microsystems Technology Laboratories at MIT.

Hosted by: Paul R. Berger

Note: Pre-recorded Webinar Only