



ECE Distinguished Seminar Series

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1:30 PM in 260 Dreese Laboratories

History, Current Status and Remaining Challenges of III-V MOS Technology

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Abstract: In this seminar, Prof. Ye will briefly talk about the motivation for high-k/III-V MOSFET research and summarize the historical development of the field with the details on Si/Ge interfacial control layer, in-situ MBE Ga-Gd-oxide and ex-situ ALD high dielectrics. The novel application of the ALD process on III-V compound semiconductors affords tremendous functionality and opportunity by enabling the formation of high-quality gate oxides and passivation layers on III-V devices. An inversion-mode n-channel $\text{Al}_2\text{O}_3/\text{InGaAs}$ MOSFET shows a gate leakage current density less than 10^{-4} A/cm², a record high maximum drain current of 1.05 A/mm and a peak transconductance of 1.3 S/mm at deep sub-micron gate-length. Retrograde, halo-implantation and 3D FinFET structure are used to further improve the off-state performance of InGaAs MOSFETs. The review of this work and recent progress in this field can be found in *IEEE Spectrum* September 2008 and *Science* February 2009.

Bio: Peide D. Ye received the B.S. degree in electrical engineering from Fudan University, Shanghai, China, in 1988 and Ph.D. in solid state physics from Max-Planck-Institute of Solid State Research, Stuttgart, Germany, in 1996. From 1996 to 2000, he was research fellow at NTT Basic Research Laboratories and NHMFL/Princeton University. He joined Bell Laboratories, Murray Hill, NJ and then Agere Systems in 2001 as a Member of Technical Staff and became a Senior Member of Technical Staff in 2003. He joined Purdue University in 2005 as associate professor of electrical and computer engineering and became a full professor in 2010. His research activities include semiconductor physics and devices, nano-structures and nano-fabrications, quantum and spin transport, atomic layer deposition, III-V MOSFETs, graphene nanoelectronics and all-oxide electronics.

Host: Paul R. Berger