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Tunnel Transistor Based Energy Efficient Logic

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1:30 PM, 260 Dreese Laboratory

Abstract: Since 1926 it is well accepted that the continuous nonzero nature of solutions to Schrodinger's wave equation used to represent electrons, even in classically forbidden regions of negative kinetic energy, allows for a finite and tunable probability of tunneling from one classically allowed region to another (for example band to band tunneling in a semiconductor). We are investigating a novel transistor architecture based on such tunneling mechanism as a step towards demonstrating steep switching transistors for energy efficient logic and embedded memory applications. In this seminar, we will address the following topics regarding the tunnel transistor architecture: a) the choice of appropriate materials to tune the transfer characteristics over a specified gate swing b) the characteristic screening lengths in these device essential for scaling dc) an effective way to estimate the switching speed of such devices, d) digital circuit design methodologies utilizing tunnel transistors, and, finally, e) the importance of nonequilibrium carrier dynamics on the device terminal characteristics. We will present the experimental tunnel transistor results till date and show that inter-band tunnel transistor is a promising architecture for future low power computing and storage applications.

Bio: Suman Datta is the Monkowsky Associate Professor in the Department of Electrical Engineering at the Penn State University with a joint appointment in the Penn State Materials Research Institute. Suman received his Bachelors in Electrical Engineering from the Indian Institute of Technology, Kanpur, India, in 1995 and his Ph.D. in Electrical & Computer Engineering from the University of Cincinnati, USA, in 1999. As a member of the Logic Technology Development and Components Research Group at Intel Corporation, from 1999 to 2007, he was instrumental in the demonstration of the world's first enhancement and depletion mode indium antimonide based quantum-well transistors operating at room temperature with record power-delay product, the first experimental demonstration of the effect of metal gate plasmon screening and channel strain engineering in mitigating the remote soft optical phonon induced mobility degradation in high-k/metal-gate CMOS transistors and, finally, the investigation of the transport properties and the electrostatic robustness in non-planar "Tri-Gate Transistors" for extreme scalability. Since Fall of 2007 he has been at Penn State University exploring new materials, novel nanofabrication techniques and non-classical device structures for CMOS "enhancement" as well as "replacement" for future energy efficient computing applications. He has over 68 archival refereed journal and conference publications and holds 97 US patents.

Host: Paul R. Berger