



# ECE Distinguished Seminar Series

*IEEE EDS/LEOS Distinguished Lecturer*

## *Beyond Scaling – Teaching the Old Dog some New Tricks!*

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Semiconductor Research & Development Center, IBM



**Thursday, March 29, 1:30 pm**  
**Dreese Laboratory 260**

While the semiconductor industry has been focused on the challenges of scaling, it has become quite apparent that one must take a broader view of delivering productivity and performance gains in this new regime of non-classical scaling. While transistor level and interconnect performance will continue to make strides through the innovative use of stress engineering, novel materials such as high k dielectrics in the front end and low k dielectrics and high conductivity interconnects in the backend, there is much more to be gained by addressing the issues of memory integration, on-chip decoupling and autonomic chip functions.

We will address three “unconventional” approaches to provide more functional value to silicon:

- Memory technology – we will address the increasing use of embedded DRAM in the cache hierarchy, including the adapting of DRAM to SOI and the scaling of DRAMs in a logic technology
- The use of electromigration to program fuses that in turn are used for autonomic chip functions including One Time Programmable Memory
- The importance of decoupling and the use of deep trench capacitors that can provide significant performance and die size improvement

While scaling and innovative new materials will continue to provide density and performance improvements to CMOS technology, a judicious use of memory technologies, the innovative use of on chip structures such as trenches for decoupling and the innovative use of phenomena such as electromigration can provide huge benefits in altogether new dimensions.

**Subramanian (Subu) S. Iyer** is a Distinguished Engineer and Director of 45nm and eTechnology Development at the IBM Microelectronics Division, Semiconductor Research and Development Center . He obtained his B.Tech in Electrical Engineering at the Indian Institute of Technology, Bombay in 1977, and his M.S. and Ph.D. in Electrical Engineering at the University of California at Los Angeles in 1978 and 1981 respectively. He joined the IBM T. J. Watson Research Center in 1981 and was manager of the Exploratory Structures and Devices Group till 1994, when he founded SiBond LLC to develop and manufacture Silicon-on-insulator materials. Dr. Iyer has received a Corporate award and four Outstanding Technical Achievement awards at IBM for the development of the Titanium Salicide process, the fabrication of the first SiGe Heterojunction Bipolar Transistor and the development of embedded DRAM technology and the development of eFUSE technology. He holds over 35 patents and has received 18 Invention Plateau awards. Dr. Iyer is a Fellow of IEEE and a Distinguished Lecturer of the IEEE.

*Sponsored by the IEEE EDS/LEOS Chapter under its Distinguished Lecturer Program*