Abstract: This paper discusses a digital control strategy for three-phase PWM voltage inverters used in a single stand-alone AC Distributed Generation System (DGS). The proposed control strategy utilizes the perfect robust servomechanism problem control theory to allow elimination of specified unwanted voltage harmonics from the output voltages under severe non-linear load and to achieve fast recovery performance on load transient. This technique is combined with a discrete sliding mode current controller that provides fast current limiting capability necessary under overload or short circuit conditions. The proposed control strategy has been implemented on a DSP (Digital Signal Processor) system and experimentally tested on an 80 kVA prototype unit. The results showed the effectiveness of the proposed control algorithm.

Index terms – three-phase PWM inverters, digital signal processor (DSP), robust servomechanism control, and sliding mode control.

I. INTRODUCTION

Techniques for producing low Total Harmonic Distortion in PWM inverters (single-phase or three-phase) have been known to exist in several prior works. In the early days, the carrier-modulated PWM techniques such as the triangular wave comparison type PWM are very popular [4]-[6]. Microcomputer based techniques using preprogrammed PWM pattern have also been utilized [7]-[10]. In these techniques, the switching edges of the PWM pattern are computed to satisfy certain performance requirements; the most common of which is controlling the fundamental component and eliminating specified harmonics. Two main disadvantages of these techniques are: slow voltage regulation response due to average voltage control, and phase displacement between the reference sine wave and the filter output varies with the load. More recent techniques include the time optimal response switching PWM [11]-[13] and the real-time deadbeat-controlled PWM [14],[15]. These techniques have very fast response for load disturbances, but it is also known that these systems have a high THD for non-linear load (crest-load).

The voltage control technique proposed here uses the perfect control of robust servomechanism problem (Perfect RSP) theory developed in [1] to ensure perfect tracking of the output voltages under unknown load by providing means for eliminating errors at specified harmonic and at the same time ensuring good transient response. The theory is based on the internal model principle, proposed by [2] which states that asymptotic tracking of controlled variables toward the corresponding references in the presence of disturbances (zero steady state tracking error) can be achieved if the models that generate these references and disturbances are included in the stable closed loop systems. In other words, if we include the frequency modes of the references and the disturbances to be eliminated in the control loop, then the steady state error will not contain these frequency modes. Applying the internal model principle into the output voltages control in a three-phase PWM inverter means that the fundamental frequency mode (50 Hz or 60 Hz) has to be included in the controller since the references vary at this frequency. Elimination of the voltages errors due to the load currents at other harmonics frequency can then be achieved by including the frequency modes of these harmonics into the controller. The perfect RSP theory combines this internal model principle with optimal state feedback to guarantee stability of the closed loop system and providing arbitrary good transient response.

Similar techniques that use the internal model principle to achieve very low THD output voltage in single-phase PWM inverters have been reported recently in [19] and [20]. In these papers, the control development follows the repetitive control theory developed in [16] to [18]. Unlike the technique based on the perfect RSP that provides zero steady state error for references or disturbances only at finite specified frequencies, the repetitive control guarantees zero steady state error at all the harmonic frequencies less than half of the sampling period. However, the repetitive control is not easy to stabilize for all unknown load disturbances and cannot obtain very fast response for fluctuating load. In [19], the latter problem is solved by including a ‘one sampling ahead preview controller’, and [20] enhances the stability result of [19] by providing an adaptive mechanism for unknown load disturbances.
disturbances.

The authors would like to point out here that, although the perfect RSP used in this paper only eliminates voltage harmonic at a finite specified frequencies, the perfect RSP control is still a very suitable control for a three-phase PWM inverters. It is to be emphasized that in a three-phase system, most of the voltage harmonics, the even harmonics, are either non-existence and/or uncontrollable, or negligible in values. Therefore, not too many harmonics are left for the control to handle. Moreover, the closed loop stability under unknown load is easier to achieve with the perfect RSP than the repetitive control, and the perfect RSP by itself already provides a good transient response.

In this research, the authors have also successfully combined the perfect RSP control of the voltages harmonics with a fast current controller using a discrete time sliding mode controller [3] for inverting the currents under overload condition. This is one of the important features necessary for a stand-alone DGS, which is not addressed in the repetitive control work of [19] and [20]. The discrete sliding mode controller has been chosen because of the fast and no-overshoot response that it provide. The current controller acts as an inner loop to the perfect RSP control of the output voltages in the outer loop. In this case, the perfect RSP voltage control has been designed by accounting for the extra dynamic introduced by the discrete time sliding mode controller. This way, the stability and robustness of the overall control system are still guaranteed.

This paper is organized as follows. Section II provides a description of the power converter system and its state space model development. Section III explains systematically the design of the voltage and current controllers using the two control techniques. Experimental results of the proposed control strategy are given in Section IV.

II. THE POWER CONVERTER SYSTEM

The power converter system used in this research consists of a typical three-phase PWM voltage inverter with LC output filter (Linv and Cinv) and a delta-wye transformer that act both as a potential transformer and electrical isolation to the load. Fig.1 shows a circuit diagram of the system. Notice that the delta-wye transformer converts a three-wire (UVW) power system of the inverter to a four-wire (XYZ-N) system for the load. Small capacitors (denoted as Cgrass in Fig.1) are added at the load side of the transformer to provide further harmonics filtering and stabilization of the load voltages. A DSP (Digital Signal Processor) system controls the operation of the power converter, providing required PWM gating signals to the power devices. Volatges and currents measured by the DSP system for control purposes are shown labeled in Fig.1. The line-to-neutral load voltages (at points xyz-n in Fig. 1) are denoted as: \( V_{load_{an}} \), \( V_{load_{bn}} \), and \( V_{load_{cn}} \), the load phase currents as: \( I_{load_a} \), \( I_{load_b} \), and \( I_{load_c} \), the line-to-line inverter filter capacitor voltages (at points uvw in Fig. 1) as: \( V_{inv_{ab}} \), \( V_{inv_{bc}} \), and \( V_{inv_{ca}} \), the inverter phase currents as: \( I_{inv_a} \), \( I_{inv_b} \), and \( I_{inv_c} \).

For development of the control algorithm, a state space model of the system is needed. Each phase of the delta-wye transformer has been modeled as an ideal transformer with leakage inductance \( L_{trans} \) and series resistance \( R_{trans} \) on the secondary winding as shown in Fig. 2. The secondary transformer currents are denoted as \( I_{snd_a} \), \( I_{snd_b} \), and \( I_{snd_c} \).

Using the transformer model in Fig. 2, the dynamic equations of the output filter circuit in Fig. 1 can be written as in equations (1.a)-(1.d):

\[
\frac{dV_{inv_{abc}}}{dt} = \frac{1}{3 \cdot C_{inv}} I_{inv_{abc}} - \frac{1}{3 \cdot C_{inv}} T_{r1} \cdot I_{snd_{abc}} \tag{1.a}
\]

\[
\frac{dI_{inv_{abc}}}{dt} = \frac{1}{L_{inv}} V_{pwm_{abc}} - \frac{1}{L_{inv}} V_{inv_{abc}} \tag{1.b}
\]

\[
\frac{dV_{load_{abc}}}{dt} = \frac{1}{C_{load}} I_{snd_{abc}} - \frac{1}{C_{load}} I_{load_{abc}} \tag{1.c}
\]

\[
\frac{dI_{snd_{abc}}}{dt} = \frac{1}{L_{trans}} I_{snd_{abc}} \tag{1.d}
\]

where the voltages and currents vectors are defined as in (2).

\[
\begin{align*}
V_{inv_{abc}} &= [V_{inv_ab} \hspace{0.2cm} V_{inv_bc} \hspace{0.2cm} V_{inv_{ca}}]^T \\
V_{load_{abc}} &= [V_{load_ab} \hspace{0.2cm} V_{load_bc} \hspace{0.2cm} V_{load_ca}]^T \\
I_{load_{abc}} &= [I_{load_a} \hspace{0.2cm} I_{load_b} \hspace{0.2cm} I_{load_c}]^T \\
I_{snd_{abc}} &= [I_{snd_a} \hspace{0.2cm} I_{snd_b} \hspace{0.2cm} I_{snd_c}]^T \\
I_{inv_{abc}} &= [I_{inv_ab} \hspace{0.2cm} I_{inv_bc} \hspace{0.2cm} I_{inv_{ca}}]^T \\
\end{align*}
\tag{2}
\]

\[
= [I_{inv_a} - I_{inv_b} \hspace{0.2cm} I_{inv_b} - I_{inv_c} \hspace{0.2cm} I_{inv_c} - I_{inv_d}]^T
\]
Matrices $T_{q1}$ and $T_{r1}$ in equation (1.a) and (1.d) denote the currents and voltages transformations of the delta-wye transformer. Denoting the transformer’s turn ratio as $tr$, these matrices are given by (3):

$$T_{q1} = \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \\ -2 & 1 & 1 \end{bmatrix}, \quad T_{r1} = \begin{bmatrix} 0 & 0 & -1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$$ \hspace{1cm} (3)

To obtain a state space model of the system, the dynamic equations in (1) are transformed to the DQ0 stationary reference frame using the transformation:

$$\tilde{f}_{qd0} = K_s \cdot \tilde{f}_{abc},$$ \hspace{1cm} (4)

with

$$K_s = \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \\ 0.5 & 0.5 & 0.5 \end{bmatrix},$$

$$\tilde{f}_{qd0} = [\tilde{f}_d, \tilde{f}_q, \tilde{f}_0]^T, \quad \tilde{f}_{abc} = [f_a, f_b, f_c]^T$$

where $\tilde{f}_{abc}$ denotes the abc voltages and currents defined in (4), and $\tilde{f}_{qd0}$ the corresponding DQ0 stationary reference frame variables. The circuit dynamics can then be written as in (5):

$$\frac{d\tilde{V}_{inv}}{dt} = \frac{1}{3 - C_{inv}} \tilde{I}_{inv} - \frac{1}{3 - C_{inv}} T_{r1} \cdot \tilde{I}_{snd}$$ \hspace{1cm} (5.a)

$$\frac{d\tilde{I}_{inv}}{dt} = \frac{1}{L_{inv}} \tilde{V}_{pwm} - \frac{1}{L_{inv}} \tilde{V}_{inv}$$ \hspace{1cm} (5.b)

$$\frac{d\tilde{V}_{load}}{dt} = \frac{1}{C_{load}} \tilde{I}_{snd} - \frac{1}{C_{load}} \tilde{V}_{load}$$ \hspace{1cm} (5.c)

$$\frac{d\tilde{I}_{snd}}{dt} = \frac{1}{L_{trans}} \tilde{I}_{snd} + \frac{1}{L_{trans}} T_{r1} \cdot \tilde{V}_{inv}$$ \hspace{1cm} (5.d)

where the matrices $T_{r1}0$ and $T_{r1}v$ are defined as:

$$T_{r10} = [K_s \cdot T_{r1} \cdot K_s^{-1}]_{row 1,2} = tr \cdot \frac{3}{2} \begin{bmatrix} 1 & 0 & -\sqrt{3} \\ 0 & 1 & 1 \\ -\sqrt{3} & 1 & 0 \end{bmatrix}$$ \hspace{1cm} (6.a)

$$T_{r1v} = [K_s \cdot T_{r1} \cdot K_s^{-1}]_{col 1,2} = tr \cdot \frac{1}{2} \begin{bmatrix} 1 & -\sqrt{3} \\ -\sqrt{3} & 1 \\ 0 & 0 \end{bmatrix}$$ \hspace{1cm} (6.b)

Notice that, due to the three-wire system of the inverter and filter, the zero components of the inverter voltages ($\tilde{V}_{inv,0}$), the inverter currents ($\tilde{I}_{inv}$) and the input PWM voltages ($\tilde{V}_{pwm,0}$) are trivial and they do not appear in (5).
III. CONTROL SYSTEM DEVELOPMENT

To achieve fast current limiting capability for the inverter, the control strategy uses a two-loop control structure: an inner inverter currents loop and an outer load voltages loop as shown in Fig. 3. The outer loop regulates the load voltages ($\vec{V}_{load,qd}$) to follow 50/60 Hz balanced three-phase voltages references ($\vec{V}_{ref,qd}$) and generates the inverter currents commands ($\vec{I}_{cmd, qd}$), which are limited. The inner loop in turn generates the PWM voltage commands to regulate the inverter currents to follow the inverter current command. A standard voltage space vector algorithm is then used to realize the two control loops, the inner current loop using the discrete sliding mode controller and the voltage control loop using the robust servomechanism principles.

The next two subsections summarizes the development of the two control loops, the inner current loop using the discrete sliding mode controller and the voltage control loop using the robust servomechanism principles.

A. Discrete-Time Sliding Mode Current Controller

For designing the discrete time sliding mode current controller, consider the inverter and filter subsystem with no transformer and load dynamics:

$$\frac{d\vec{V}_{inv,qd}}{dt} = \frac{1}{3} C_{inv} \vec{I}_{inv,qd} - \frac{1}{3} C_{inv} \vec{V}_{pwm,qd} \cdot \vec{I}_{sd,qd0} \quad (7.a)$$

$$\frac{d\vec{I}_{inv,qd}}{dt} = \frac{1}{L_{inv}} \vec{I}_{pwm,qd} - \frac{1}{L_{inv}} \vec{V}_{inv,qd} \quad (7.b)$$

Assuming the secondary transformer currents $\vec{I}_{sd,qd0}$ as disturbances, this subsystem can be written in state space form as:

$$\dot{\vec{x}}_1 = A_1 \vec{x}_1 + B_1 \vec{u} + E_1 \vec{d}_1$$

$$A_1 = \begin{bmatrix} 0 \circ 2 \circ 2 & (3 \cdot C_{inv})^{-1} \cdot I_{2 \circ 2} \\ -(L_{inv})^{-1} \cdot I_{2 \circ 2} & 0 \circ 2 \circ 2 \end{bmatrix},$$

$$B_1 = \begin{bmatrix} 0 \circ 2 \circ 2 \\ (L_{inv})^{-1} \cdot I_{2 \circ 2} \end{bmatrix}, \quad E_1 = \begin{bmatrix} -(3 \cdot C_{inv})^{-1} \cdot T_{ri,qd0} \\ 0 \circ 2 \circ 2 \end{bmatrix},$$

where the states are $\vec{x}_1 = \vec{V}_{inv,qd}, \vec{I}_{inv,qd}$, the inputs $\vec{u} = \vec{V}_{pwm,qd}$ and disturbances $\vec{d}_1 = \vec{I}_{sd,qd0}$.

The discrete form of (8) can be calculated as:

$$\hat{\vec{x}}_1(k+1) = A_1^* \hat{\vec{x}}_1(k) + B_1^* \vec{u}(k) + E_1^* \vec{d}_1(k)$$

where

$$A_1^* = \exp(A \cdot T_S) \quad B_1^* = \int_0^{T_S} e^{A_1^*} \vec{B}_1 \ d\vec{\tau}$$

$$E_1^* = \int_0^{T_S} e^{A_1^*} \vec{E}_1 \ d\vec{\tau}$$

and $T_S$ is the A/D sampling time, which in this case is equal to the PWM period $T_{pwm}$.

To force the inverter currents to follow their commands, the sliding mode surface is chosen as:

$$\vec{s}(k) = C_1 \cdot \vec{x}_1(k) - \vec{I}_{cmd,k}$$

so that when discrete sliding mode occurs, we have $\vec{s}(k) = 0$ or $\vec{I}_{inv}(k) = \vec{I}_{cmd}(k)$. The existence of the discrete sliding mode can be guaranteed if the control is given [3]:

[Fig. 3 Overall control system]

[Fig. 4 Control timing diagram]
\[ u(k) = \begin{cases} 
\bar{u}_{eq}(k) & \text{for } \|\bar{u}_{eq}(k)\| \leq u_0 \\
u_0 & \text{for } \|\bar{u}_{eq}(k)\| > u_0 
\end{cases} \quad (9) \]

where the equivalent control input \( \bar{u}_{eq}(k) \) is calculated from:

\[ \bar{u}_{eq}(k) = \left( C_1 B_1^* \right)^{-1} \left( I_{cmd \_qd} - C_1 A_1^* \bar{x}_1(k) - C_1 E_1^* d_1^*(k) \right) \quad (10) \]

and \( u_0 \) denotes the maximum value of the PWM voltage command realizable by the space vector algorithm.

Note that the secondary transformer currents are needed for the control, but these currents are not measured in the system (see Fig. 1). A linear Luenberger observer can be easily designed to estimate these currents for control purposes. However, in most practical cases we can approximate these currents with the load currents (i.e. \( \bar{I}_{sd\_qd} = \bar{I}_{load\_qd} \)) since the currents through the output capacitor filters are small. According to the authors’ experience, the effect of using this approximation is unnoticeable in the control performance.

Due to the computation delay of the DSP, the control action given by (9) will result in undesirable overshoots during transients. This effect can be minimized, however, if the states \( \bar{x}_1(k) \) and disturbances \( \bar{d}_1^*(k) \) are replaced with their first order one-half step ahead predicted values given by:

\[ \bar{x}_1^p(k) = 1.5 \cdot \bar{x}_1(k) - 0.5 \cdot \bar{x}_1(k-1) \]

\[ \bar{d}_1^p(k) = 1.5 \cdot \bar{d}_1(k) - 0.5 \cdot \bar{d}_1(k-1) \quad (11) \]

The equivalent control input \( \bar{u}_{eq}(k) \) then becomes:

\[ \bar{u}_{eq}(k) = \left( C_1 B_1^* \right)^{-1} \left( I_{cmd \_qd} - C_1 A_1^* \bar{x}_1^p(k) - C_1 E_1^* \bar{d}_1^p(k) \right) \quad (12) \]

B. Voltage Controller Design using Discrete Perfect RSP

The voltage control loop designed in this paper is based on the discrete form of the technique developed in Davison [1]. To design the load voltages controller, let’s first consider the entire plant system with the 0-components of the voltages and currents omitted as given in (13). As explained in section III, these 0-components are completely decoupled and uncontrollable from the inputs, and therefore are not useful to be included in the design. In the system (13), an input delay of one-half the PWM period (0.5T\(_{\text{pwm}}\)) has been explicitly included to account for the computation delay of the DSP.

The states variables for the system (13) are chosen as:

\[ \bar{x}_p = [\bar{V}_{inv\_qd}, \bar{I}_{inv\_qd}, \bar{V}_{load\_qd}, \bar{I}_{sd\_qd}] \]

with the inputs as \( u = V_{\text{pwm\_qd}} \). System (13) can be transformed to a discrete-time system with sampling time \( T_s = T_{\text{pwm}} \) to yield:

\[ \bar{x}_p(k+1) = \Phi \cdot \bar{x}_p(k) + \Gamma_1 \cdot \bar{u}(k-1) + \Gamma_2 \cdot \bar{u}(k) \quad (14) \]

where

\[ \Phi = e^{A_{\text{d}} T_s}, \quad \Gamma_1 = \int_0^{T_s} e^{A_{\text{d}} \tau} B_{\text{d}} d\tau, \quad \Gamma_2 = \int_0^{0.5T_s} e^{A_{\text{d}} \tau} B_{\text{d}} d\tau \]

Discrete time system (14) can be written in a standard discrete time state space equations by adding the extra states:

\[ \bar{x}_a(k) = \bar{u}(k-1) = V_{\text{pwm\_qd}}(k-1) \]

so that the system can be written as:

\[ \bar{x}_p(k+1) = A_p^* \bar{x}_p(k) + B_p^* \bar{u}(k) \quad (15) \]

where:

\[ \bar{x}_p(k) = \begin{bmatrix} \bar{x}_p(k) \\ \bar{x}_a(k) \end{bmatrix}, \quad A_p^* = \begin{bmatrix} \Phi & \Gamma_1 \\ \bar{0}_{2\times2} & \bar{0}_{2\times2} \end{bmatrix}, \quad B_p^* = \begin{bmatrix} \Gamma_2 \\ \bar{I}_{2\times2} \end{bmatrix} \]

To design the voltage controller, we need to consider the true plant (16) and the discrete time sliding mode current controller as the equivalent ‘plant’ as seen by the outer voltage loop. Using equation (10) and (16) the augmented true plant and discrete sliding mode current controller can be found as in (17).

\[ \begin{align*}
\dot{x}(t) &= A_p \bar{x}(t) + B_p \bar{u}(t - 0.5T_{\text{pwm}}) \\
\dot{A}_p &= \begin{bmatrix} \bar{0}_{2\times2} & (3 \cdot C_{\text{inv}})^{-1} \cdot \bar{T}_{2\times2} & \bar{0}_{2\times2} & -(3 \cdot C_{\text{inv}})^{-1} \cdot \bar{T}_{3\times2} \\
-(L_{\text{inv}})^{-1} \cdot \bar{T}_{2\times2} & \bar{0}_{2\times2} & \bar{0}_{2\times2} & \bar{0}_{2\times2} \\
(L_{\text{inv}})^{-1} \cdot \bar{T}_{2\times2} & \bar{0}_{2\times2} & \bar{0}_{2\times2} & (C_{\text{load}})^{-1} \cdot \bar{T}_{2\times2} \\
(0) & \bar{0}_{2\times2} & \bar{0}_{2\times2} & \bar{0}_{2\times2} 
\end{bmatrix} \\
\dot{B}_p &= \begin{bmatrix} \bar{0}_{2\times2} \\
(L_{\text{inv}})^{-1} \cdot \bar{T}_{2\times2} & \bar{0}_{2\times2} & \bar{0}_{2\times2} \end{bmatrix} \\
\dot{T}_{2\times2} &= tr\cdot \frac{3}{2} \begin{bmatrix} 1 & \sqrt{3} \\ -\sqrt{3} & 1 \end{bmatrix} \\
\dot{T}_{3\times2} &= tr\cdot \frac{1}{2} \begin{bmatrix} 1 & -\sqrt{3} \\ \sqrt{3} & 1 \end{bmatrix} 
\end{align*} \quad (13) \]
\[
\dot{x}_p(k+1) = A_d x_p(k) + B_d \tilde{u}_i(k)
\] (17)
with \( \tilde{u}_i(k) = \tilde{I}_{cmd}^* qd(k)\), and
\[
A_d = A_p^* - B_p^* \left[ C_1 B_1 \right]^{-1} \left[ b_1^* C_{11} + e_1^* C_{12} \right]
\]
\[
B_d = B_p^* \left[ C_1 B_1 \right]^{-1}
\]
\[
C_{11} = \begin{bmatrix}
\hat{I}_{2x2} & \hat{0}_{2x2} & \hat{0}_{2x2} & \hat{0}_{2x2} \\
\hat{0}_{2x2} & \hat{I}_{2x2} & \hat{0}_{2x2} & \hat{0}_{2x2} \\
\hat{0}_{2x2} & \hat{0}_{2x2} & \hat{I}_{2x2} & \hat{0}_{2x2} \\
\hat{0}_{2x2} & \hat{0}_{2x2} & \hat{0}_{2x2} & \hat{I}_{2x2}
\end{bmatrix}
\]
\[
C_{12} = \begin{bmatrix}
\hat{0}_{2x2} & \hat{0}_{2x2} & \hat{0}_{2x2} & \hat{I}_{2x2}
\end{bmatrix}
\]
Note that the augmented system given in (17) was found assuming the approximation \( \tilde{I}_{sand} qd = \tilde{I}_{load} qd \) has been used.

Now, assume \( \omega_i = 2\pi f_i \), \( i = 1,\ldots,n \) are frequencies of the reference voltages and harmonics to be eliminated. For a 60-Hz DGS system with desire to eliminate 5th and 7th harmonics, for example, we use \( \omega_1 = 2\pi \cdot 60 \), \( \omega_2 = 2\pi \cdot 5 \cdot 60 \), and \( \omega_3 = 2\pi \cdot 7 \cdot 60 \). We can then choose the servo-compensator to be of the form (18):
\[
\dot{\eta} = A_c \eta + B_c e_{Vqd}
\]
\[
\dot{e}_{Vqd} = V_{ref} qd - V_{load} qd
\] (18)
where
\[
\eta = [\eta_1, \eta_2, \ldots, \eta_n]^T \quad \eta_i \in \mathbb{R}^4, \quad i = 1,\ldots,n
\]
\( A_c = \text{block diag} \left[ A_{c1}, A_{c2}, \ldots, A_{cn} \right] \)
\( B_c = [B_{c1}, B_{c2}, \ldots, B_{cn}]^T \)
with
\[
A_{ci} = \begin{bmatrix}
\hat{0}_{2x2} & \hat{I}_{2x2} \\
-\omega_i^2 \hat{I}_{2x2} & \hat{0}_{2x2}
\end{bmatrix}, \quad i = 1,\ldots,n
\]
\( B_{ci} = \hat{0}_{2x2} \hat{I}_{2x2} \) \( i = 1,\ldots,n \)
Note that each of the blocks \( \dot{\eta}_i = A_{ci} \eta_i + B_{ci} e_{Vqd} \) represents a state space implementation of the continuous transfer function: \( 1/(s^2 + \omega_i^2) \) for each of the qd-axis voltages errors.

The servo compensator (18) can be transformed to a discrete time system to yield:
\[
\tilde{\eta}(k+1) = A_c^* \tilde{\eta}(k) + B_c^* e_{Vqd}(k),
\]
\[
\dot{e}_{Vqd}(k) = V_{ref} qd(k) - V_{load} qd(k)
\] (19)
where:
\[
A_c^* = \exp(A_c \cdot T_S) \quad B_c^* = \int_0^{T_S} e^{A_c \cdot (\tau - T_S)} B_c \, d\tau
\]
Now that we have determined the 'plant' and the servo compensator, the control input for the perfect robust servomechanism controller is given by:
\[
\tilde{u}_i(k) = \tilde{I}_{cmd}^* qd(k) = K_0 \tilde{x}_p^* + K_1 \eta(k)
\] (20)
where the gains \( K = [K_0 \quad K_1] \) are found by minimizing the discrete performance index:
\[
J_\varepsilon = \sum_{k=0}^{\infty} \left( z(k) + \varepsilon \cdot u(k) \right) u(k),
\]
\[
z = \begin{bmatrix}
\tilde{x}_p^* \\
\eta
\end{bmatrix}
\] (21)
for the augmented ‘equivalent plant’ (17) and the servo compensator (19):
\[
\begin{bmatrix}
\tilde{x}_p^*(k+1) \\
\eta(k+1)
\end{bmatrix} =
\begin{bmatrix}
A_d & 0 \\
- B_c^* C & A_c^*
\end{bmatrix}
\begin{bmatrix}
\tilde{x}_p^*(k) \\
\eta(k)
\end{bmatrix} +
\begin{bmatrix}
B_d \\
- B_c^* D
\end{bmatrix} u_i(k)
\] (22)
where \( \varepsilon > 0 \) is an arbitrarily small scalar. Solutions of (21) and (22) can be found easily using Matlab command dlqr.

**Current Limit and Control Saturation Handling**

The current command \( \tilde{I}_{cmd} qd(k) \) generated by the robust servomechanism voltage controller above is limited in magnitude as in (23) to yield the current command \( \tilde{I}_{cmd} qd(k) \), which will be implemented by the inner loop current controller:
\[
\tilde{I}_{cmd} qd(k) = \begin{bmatrix}
\tilde{I}_{cmd}^* qd(k) \\ \tilde{I}_{cmd}^* qd(k)
\end{bmatrix} \begin{cases}
I_{max} & \text{if } |\tilde{I}_{cmd}^* qd(k)| \leq I_{max} \\
|\tilde{I}_{cmd}^* qd(k)| I_{max} & \text{if } |\tilde{I}_{cmd}^* qd(k)| > I_{max}
\end{cases}
\] (23)

\( I_{max} \) represents the maximum allowable magnitude of the inverter currents. Equation (23) limits the magnitude of the current commands but maintains their vector directions in the qd-space.

The states \( \tilde{\eta}_i \) of the servo-compensator can be seen as sine wave signal generators that get excited by the harmonic contents of the error signals at frequency \( \omega_i \). When the control inputs of the robust servomechanism voltage controller saturate i.e., \( |\tilde{I}_{cmd}^* qd(k)| > I_{max} \) the servo-compensator states will grow in magnitude due to the break in the control loop. This problem is similar to the integrator windup problem that occurs in an integral type controller. To prevent this, the servo-compensator in (19) can be modified as follows:
\[
\tilde{\eta}(k+1) = A_c^* \tilde{\eta}(k) + B_c^* \tilde{e}_i(k),
\]
\[
\tilde{e}_i(k) = \begin{cases}
\tilde{e}_{Vqd}(k) & \text{if } |\tilde{I}_{cmd}^* qd(k)| \leq I_{max} \\
0 & \text{if } |\tilde{I}_{cmd}^* qd(k)| > I_{max}
\end{cases}
\] (24)

Using (24), during the current limit saturation, the servo compensator states will continue to oscillate at the harmonic frequency with constant magnitude. The resulting robust servomechanism controller structure is shown in Fig. 5.
IV. V EXPERIMENTAL RESULTS

The effectiveness of the proposed control strategy has been verified on an 80kVA DGS unit with system parameters shown in Table 1. The DC bus voltage is obtained from a 6-pulse thyristor controlled rectifier in parallel with a 480V battery system. The DSP control system used is based on the TMS320F240 fixed point DSP with control timing diagram as given in Fig. 5. The PWM timing is calculated through a standard space vector PWM with switching frequency of 3.2 kHz ($T_{pwm} = T_s = 320 \ \mu \text{sec}$).

The experimental results presented in this paper have been obtained using the proposed control strategy with only the 5th and 7th harmonics being eliminated. Table 2 gives the steady state RMS output voltages regulation under different types of loads. It can be seen that the control strategy provides good output voltages regulation in all cases. Note that, the deviations in the output voltages for unbalanced load are due to the uncontrollable 0-component of the load currents. However, as can be seen the effect is minimal showing the effectiveness of the LC filter at the output side of the transformer.

Fig. 6 shows the waveforms of the load currents, load voltages, and inverter voltages under various linear loads: resistive, inductive, balanced, and unbalanced load. Fig. 7 shows the load voltages, load currents, inverter voltages, and inverter currents under. The THD of the load voltages in Fig. 7 was measured at 2.8% with the load currents of 3:1 crest factor. Table 3 summarizes the output voltages THD under different types of loads showing the superior THD performance of the proposed control strategy. Better results may be obtained by including more harmonics to be eliminated into the robust servomechanism controller.

---

**Table 1. System Parameters**

<table>
<thead>
<tr>
<th>DC Bus Voltages</th>
<th>$V_{dc}$</th>
<th>540 V (nom.) 390V (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Output voltage</td>
<td>$V_{load}$</td>
<td>208V (LL-RMS), 120V(LN)</td>
</tr>
<tr>
<td>$f$</td>
<td>60 Hz</td>
<td></td>
</tr>
<tr>
<td>Inverter filters</td>
<td>$C_{inv}$</td>
<td>540 $\mu$F</td>
</tr>
<tr>
<td></td>
<td>$L_{inv}$</td>
<td>300 $\mu$H</td>
</tr>
<tr>
<td>Delta-Wye Transformer</td>
<td>$L_{trans}$</td>
<td>48 $\mu$H ($= 0.03$ p.u)</td>
</tr>
<tr>
<td></td>
<td>$R_{trans}$</td>
<td>0.02 ohm</td>
</tr>
<tr>
<td>Output filter</td>
<td>$C_{grass}$</td>
<td>90 $\mu$F</td>
</tr>
</tbody>
</table>

**Table 2. Output voltages regulation**

<table>
<thead>
<tr>
<th>TYPES OF LOAD</th>
<th>OUTPUT V</th>
<th>AVG</th>
<th>FLD OUTPUT V</th>
<th>AVG</th>
</tr>
</thead>
<tbody>
<tr>
<td>No load</td>
<td>1.0%</td>
<td>129.67</td>
<td>129.85</td>
<td>129.45</td>
</tr>
<tr>
<td>100% balanced resistive load</td>
<td>1.35%</td>
<td>129.67</td>
<td>129.85</td>
<td>129.45</td>
</tr>
<tr>
<td>100% 0.8 pf load</td>
<td>1.32%</td>
<td>129.67</td>
<td>129.85</td>
<td>129.45</td>
</tr>
<tr>
<td>100% unbal. resistive (ph.A)</td>
<td>1.70%</td>
<td>129.67</td>
<td>129.85</td>
<td>129.45</td>
</tr>
<tr>
<td>100% unbal. resistive (ph.A&amp;B)</td>
<td>1.89%</td>
<td>129.67</td>
<td>129.85</td>
<td>129.45</td>
</tr>
<tr>
<td>Crest load (3:1)</td>
<td>2.7%</td>
<td>129.67</td>
<td>129.85</td>
<td>129.45</td>
</tr>
</tbody>
</table>

**Table 3. Output voltages THD**

<table>
<thead>
<tr>
<th>TYPES OF LOAD</th>
<th>Output voltages THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>No load</td>
<td>0.90%</td>
</tr>
<tr>
<td>100% balanced resistive load</td>
<td>1.30%</td>
</tr>
<tr>
<td>100% 0.8 pf load</td>
<td>1.32%</td>
</tr>
<tr>
<td>100% unbal. resistive (ph.A)</td>
<td>1.70%</td>
</tr>
<tr>
<td>100% unbal. resistive (ph.A&amp;B)</td>
<td>1.89%</td>
</tr>
<tr>
<td>Crest load (3:1)</td>
<td>2.7%</td>
</tr>
</tbody>
</table>
Fig. 6. Steady state linear load (a) 100% resistive balanced (b) 100% 0.8pf load (c) 100% resistive unbalanced (phase A unloaded) (d) 100% resistive unbalanced (phase A&B). Top: load currents; middle: load voltages; bottom: inverter voltages.

Fig. 7. Steady state non-linear load: 100% 3:1 crest load. Top: phase A of load voltages and load currents, Bottom: phase A of inverter voltages and inverter currents

Fig. 8. Resistive load transient: 0% to 100%. Top: three-phase load currents, bottom: three-phase load voltages resistive load transient

Fig. 9. Resistive load transient: 100% to 0%. Top: three-phase load currents, bottom: three-phase load voltages resistive load transient

Fig. 8 and 9 show the responses of the load voltages on resistive load transients, 0-100% and 100%-0 respectively. It can be seen that the load voltages recover within less than a cycle after the load is applied. In both cases, the output voltages magnitudes deviate less than 5% of the nominal. These results show that the perfect RSP controller provides fast transient recovery under load transients with minimal overshoot in the response.

Finally, the effectiveness of the current controller was verified by applying a sudden three-phase short circuit on the output load terminals. The current limit was set at 300% level, and the inverter was shut down deliberately after ten cycles of short circuit condition. The results are shown in Fig. 10. It can be seen that the discrete sliding mode controller provides a fast and minimal overshoot on the inverter currents.
applications. The control strategy combines the perfect RSP controller for low THD output voltages regulation and the discrete sliding mode current controller for fast over-current protection. The voltage controller was developed by including the dynamic of the current controller into the plant with the computation delay of the DSP accounted for. It was shown that by including the harmonic frequency mode to be eliminated into the perfect RSP controller, superior low THD performance could be achieved without sacrificing the transient recovery performance of the output voltages. The experimental results presented verified the effectiveness of the proposed control strategy both in providing low THD output voltages regulations and in providing protection under short circuit condition.

V. CONCLUSIONS

This paper has outlined the development of a digital control strategy for three-phase PWM inverters used in DGS applications. The control strategy combines the perfect RSP controller for low THD output voltages regulation and the discrete sliding mode current controller for fast over-current protection. The voltage controller was developed by including the dynamic of the current controller into the plant with the computation delay of the DSP accounted for. It was shown that by including the harmonic frequency mode to be eliminated into the perfect RSP controller, superior low THD performance could be achieved without sacrificing the transient recovery performance of the output voltages. The experimental results presented verified the effectiveness of the proposed control strategy both in providing low THD output voltages regulations and in providing protection under short circuit condition.

VI. REFERENCES


VII. BIOGRAPHIES

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Fig. 10 Three-phase short-circuit on output terminals. Top: inverter currents, middle: load voltages, and bottom: inverter voltages.