

CONTROL OF POWER CONVERTERS FOR
DISTRIBUTED GENERATION APPLICATIONS

Technical Report

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ABSTRACT

This technical report is generated on the basis of Min Dai's Ph.D. dissertation in combination of the technical details in the implementation of the analysis and experiments conducted for the dissertation.

The contributions of this Ph.D. research include the application of a modified space vector pulse width modulation (MSVPWM) scheme combined with robust servomechanism control in a three-phase four-wire split dc bus inverter and real-time implementation of Newton-Raphson Method on digital signal processors for on-line power system identification and power flow control of a distributed generation (DG) unit. This report addresses digital control strategies of solid-state electric power converters for distributed generation applications in both island and grid-connected modes. Three major issues of DG, island operation, grid-connected operation, and front-end converter control, are discussed with proposed solutions and related analysis. In island mode, a control approach is developed for a three-phase four-wire transformerless inverter system to achieve voltage regulation with low steady state error and low total harmonic distortion (THD) and fast transient response under various load disturbances. The control algorithm combines robust servomechanism and discrete-time sliding mode control techniques. An MSVPWM scheme is proposed to implement the control under Clarke's reference frame. The robust stability of the closed-loop system is analyzed. In grid-connected mode, a real and reactive power control solution is proposed based on the proposed voltage control strategy for island operation. The power control solution takes advantage of a system parameter identification method and a nonlinear feedforward algorithm, both of which

are based on Newton-Raphson iteration method. The proposed technique also performs gridline current conditioning and yields harmonic free grid-line current. A phase locked loop (PLL) based algorithm is developed as a part of the solution to handle possible harmonic distorted grid-line voltage. In a DG unit with three-phase three-wire ac-dc-ac double conversion topology including a controlled power factor correction (PFC) front-end rectifier, unbalanced inverter load could cause current and voltage fluctuation on the dc bus. Mathematical analysis is conducted to disclose the mechanism of the dc bus voltage ripple and a notch filter based rectifier control strategy is proposed to eliminate the impact of the ripple and yield balanced input current. The effectiveness of the techniques proposed in this report is demonstrated by both simulation and experimental results. The implementation related technical details are included in the specific chapters and attached electronic files.

Technical details are provided in descriptions, illustrations, schematics, and Matlab code about the frequency domain analysis and robust stability analysis for the four-wire inverter study, the experimental setup power stage configuration, the grid-connecting contactor design, and the dc bus overvoltage protection board design. Simulink models and DSP code are given as electronic files.

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CHAPTER 1

INTRODUCTION

1.1 The Background

The need for electric energy is never ending. Along with the growth in demand for electric power, sustainable development, environmental issues, and power quality and reliability have become concerns. Electric utilities are becoming more and more stressed since existing transmission and distribution systems are facing their operating constraints with growing load. Greenhouse gas emission has resulted in a call for cleaner and renewable power sources. Development in technology has been making the whole society more and more electricity dependent and creating more and more critical loads. Under such circumstance, distributed generation (DG) with alternative sources has caught people's attention as a promising solution to the above problems. According to L. Philipson [84], distributed generation entails using many small generators of 2-50MW output, situated at numerous strategic points throughout cities and towns, so that each provides power to a small number of consumers nearby and dispersed generation refers to use of even smaller generating units, of less than 500kW output and often sized to serve individual homes or businesses. Later publications tend to combine the two categories into one, i.e., distributed generation, to refer to power generation at customer sites to serve part or all of customer load or as backup power, or, at substations to reduce peak load demand and defer substation capacity reinforcements [76]. In this proposal, the combined concept is used.

Distributed generation is not a new concept since traditional diesel generator as

backup power source for critical load has been used for decades. However, due to its low efficiency, high cost, and noise and exhaust, diesel generator would be objectionable in any applications but emergency and fieldwork and it has never become a true distributed generation source on today's basis. What endows new meaning to this old concept is technology.

Environmental friendly renewable energy sources, such as photovoltaic devices and wind electric generators, clean and efficient fossil-fuel technologies, such as micro gas turbines, and hydrogen electric devices - fuel cells, have provided great opportunities for the development in distributed generation.

Gas fired micro-turbines in the 25-100kW range can be mass produced at low cost which use air bearing and recuperation to achieve reasonable efficiency at 40% with electricity output only and 90% for electricity and heat micro-cogeneration [51, 97]. Fuel cells have the virtue of zero emission, high efficiency, and reliability and therefore have the potential to truly revolutionize power generation. The hydrogen can be either directly supplied or reformed from natural gas or liquid fuels such as alcohols or gasoline. Individual units range in size from 3-250kW or even larger MW size [76].

The fastest growing renewable energy source is wind power. On a world-wide basis, available wind energy exceeds the presently installed capacity of conventional energy sources by a factor of four. Photovoltaic systems can be used in variety of

sizes and show better potentials in those areas with high intensity and reliability of sunlight.

Besides these power generators, storage technologies such as batteries, ultracapacitors, and flywheels have also been significantly improved. Flywheel systems can deliver 700kW for 5 seconds while 28-cell ultracapacitors can provide up to 12.5kW for a few seconds [51].

To apply above generation and storage technologies in an DG environment involves new technical problems. DG units require power electronics interfacing and different methods of control and dispatch. A DG unit should be able to operate under either island mode or grid-connected mode. In island mode, it should provide steady, low regulation error, low total harmonic distortion (THD), and fast response ac power under various load disturbances. In grid-connected mode, it should give steady state decoupled active power P and reactive power Q control and proper behavior under connecting, disconnecting, and reclosing operations. If multiple units are paralleled on the same terminal or bus, correct load sharing should be performed among the units.

A dc/ac voltage source inverter (VSI) is the most widely used interface for DG units, which involves many topology and control aspects under different operating conditions. Only with satisfactory control performance of each individual unit can paralleling two or more inverters or connecting one or more inverters to the power

system be conducted which involves P and Q control under various local load characteristics and operating conditions.

As stated above, the tremendous complexity in the power electronics interfaces for DG units creates many research problems as well as many possibilities to advance technologies. Many of the problems have been solved or partly solved while many are still left unsolved or even unfound. In general, a practically functioning DG system has to properly solve possible technical problems in the following three categories - control of a single inverter unit with quality voltage output in island mode, control of line real and reactive power flowing between a DG unit and the utility grid in grid-connected mode, and control of front-end power generation or conversion for high performance and low overhead. Due to the great potential of DG technologies, these research problems deserve special attentions and warrant careful further investigations.

In this report, problems and solutions in all three above technical categories will be addressed by presenting the following information - problem descriptions, proposed solutions, related analysis, simulation and experimental results, and conclusions and discussions. a literature review will be given within the scope of research as mentioned above about DG control technologies and the existing solutions will be evaluated. Specific research problems will be stated and described on basis of the literature review.

1.2 Literature Review

Published research about power electronics interface control in distributed gener-

ation environment, including both island mode and grid-connected mode, have been reviewed and categorized into a number of subtopics as listed below.

1. Voltage and current control of individual inverters in island mode.
2. The system topology.
3. Robust stability issues.
4. Pulse width modulation techniques.
5. Line-interactive operation of inverters and control of P and Q .
6. Front-end rectifier control in controlled ac-dc-ac systems.

The published researches will be reviewed based on the above guideline.

1.2.1 Voltage and current control of individual inverters in island mode

Before being operated in grid-connected mode, a DG unit needs to work in island mode at the first place as a voltage source supplying local load with quality power.

Many researches have been conducted in this area, which can be categorized based on the control techniques used - PID control, model based linear control, robust control, sliding mode control, internal model principle based control, and intelligent control.

Conventional PI controls

Borup et al. [8] have proposed a inverter control technique based on proportional-integral (PI) regulation under stationary reference frame where the PI regulators have to track sinusoidally varying inputs. Since PI controller only guarantees zero steady

state error under dc reference input, this control technique cannot be convincing in control performance. Noriega-Pineda et al. [81] have proposed a technique based on proportional control plus model based compensation. It does not utilize the information that the reference input is a 60 Hz sine wave, so that the control design has to be able to handle arbitrary input, which is unlikely to yield a good control performance for DG applications. Lu et al. [65] have developed an inverter control technique based on PI regulation only. Even though the system is required to handle strong harmonic current, no theoretical measure has been taken to address the issue. Abdel-Rahim et al. [4] have designed and analyzed a dual loop proportional control scheme for single-phase half-bridge inverters in island mode. The authors have conducted small signal frequency domain analysis to stabilize the closed-loop system. However, the simple proportional compensation can provide satisfactory performances in neither steady state nor transient.

State feedback based controls

Some researchers use standard linear control theory to develop their controllers.

Tsai et al. [105] have proposed an analog control algorithm using canonical lead-lag compensator based on a transfer function model. Chen et al. [15] have developed a state-space model based state feedback control technique. In [15], a 'sensorless' technique is presented trying to reduce the number of measurements, however the instantaneous active and reactive power are required which ends up with more complexity and the claimed reduction of measurements is not convincing. Botterfion et al. [9] have added a linear quadratic index on top of traditional linear state feedback

control to achieve optimized performance, where the performance under nonlinear load is not tested.

Robust control

Lee et al. [55] have applied H_∞ design procedure onto a single-phase inverter to improve robust stability under model uncertainty and load disturbance. However, the control performance under nonlinear load is not satisfactory.

Sliding mode controls

Sliding mode control has also been used in inverter control due to its robustness and overshoot-free fast tracking capability. Tai et al. [100] have developed a discrete-time implementation of sliding mode control for a full bridge single-phase inverter. This technique still use discontinuous control defined in continuous time system and implements it with a digital controller, which causes chattering problem inherently according to Utkin et al.'s result [108]. Buso et al. [12] and Mihalache [74] have developed similar techniques using discrete-time sliding mode control method for single-phase inverters in both voltage and current loops. In this technique, the control variable in each sampling period is calculated based on the plant model and feedback quantities. The control is continuous and the chattering problem does not exist. The presented results show good performances under both linear and nonlinear loads. Guo et al. [37] have proposed a single-phase inverter control technique using deadbeat current control and proportional voltage control. The deadbeat control concept is the same as the discrete-time sliding mode control when the plant model parameters

are known. The presented result is reasonably good. However, its dependence on knowledge of plant parameters limits its application as an outer loop controller in multi-loop feedback systems.

Internal model principle and reference frames

Internal model principle states that asymptotic tracking of controlled variables toward the corresponding references in the presence of disturbances (zero steady state tracking error) can be achieved if the models that generate these references and disturbances are included in the stable closed loop systems [33].

Actually a PI controller is an example of using the internal model principle in that the integral term models the mode of a step input and therefore results in zero steady state error tracking dc reference input. However, this is no longer true if the reference signal is an ac quantity. In three-phase systems, reference frame transformation from stationary ABC frame to synchronous rotating dq reference frame can transform ac quantities in synchronous frequency into dc quantities which can be handled by a PI controller. It has to be noticed that a synchronous reference frame can only transform components in the synchronous frequency into dc while all other frequency components are still ac. In three-phase DG systems, if the fundamental frequency components are transformed into a synchronous reference frame, all harmonic components are still ac quantities in the same synchronous reference frame. Abdel-Rahim et al. [5] have developed a proportional control scheme for a three-phase inverter based on small signal analysis in synchronous reference frame only for the fundamen-

tal frequency. Li et al. [57] have developed a PID control scheme with decoupling consideration between the d and q -axis quantities for a three-phase inverter in synchronous reference frame also only for fundamental frequency components. Neither of these researches provides theoretical solutions to the impacts of harmonic load disturbances. Mendalek et al. [73] have proposed a nonlinear prediction technique to handle harmonic components in a fundamental synchronous reference frame. Even though the simulation results show quite good harmonic current tracking, no experimental verification is given. Dong et al. [26] have proposed a harmonic current estimator to handle harmonic current components in a fundamental synchronous reference frame. However, the performance shown in the results is not satisfactory.

Due to the limitation of a single fundamental synchronous reference frame in handling harmonics, ideas have been raised for having multiple rotating reference frames corresponding to multiple frequency components including the fundamental and harmonics as well. Cheng et al. [16] have developed a three-phase inverter controller with multiple synchronous reference frames. This technique requires information of magnitudes and phase angles of each frequency components from phase-locked loops (PLL), which increases the complexity of the solution. Ponnaluri et al. [85] have proposed a control technique also based on multiple rotating reference frames trying to convert multiple frequency components into dc. This technique needs gain and phase correction in each reference frame, which also increases the overall complexity of the solution. In general, multi-rotating frame type of techniques provide a systematical solution to achieve zero steady-state error for multiple frequency components while

the trade-off is the high complexity.

The internal model principle can be better used in a different way where the modes of all frequencies of interest are modeled in the same reference frame so that the steady state tracking errors of all modeled frequencies can reach zero. Typically, a stationary reference frame for three-phase systems is used where all ac frequency components remain ac since there is no necessity to take advantage of dc quantities given the capability of handling ac directly using the internal models. Clarke's transformation [82] from ABC stationary reference frame to $\alpha\beta 0$ stationary reference frame provides decoupling between the axes and enables independent modeling and control in each dimension and hence it is widely used. There is no reference frame issue at all in single-phase systems since all original quantities are in stationary reference frame inherently.

Repetitive control is a specific implementation of internal model principle in a single reference frame, which eliminates periodical tracking error or disturbance whose frequency is less than half sampling frequency according to Haneyoshi et al. [38]. Detailed theory of repetitive control is seen in Hara et al.'s work [39]. Haneyoshi et al. have introduced repetitive control concept to inverter control even though despite the weakness in nonlinear load test. Rech et al. [91, 92] have proposed a repetitive control approach combined with a traditional PID controller serving as a predictive feedforward. However, the technique yields similar dip on output voltage waveform under nonlinear load as the one in [38]. Tzou et al. [106] and Montagner et al. [77]

have proposed a similar adaptive mechanism, i.e., a recursive least square based estimator, to tune the repetitive controller parameters to improve the performance under nonlinear load disturbance. Liang et al. [60] have used H_∞ design procedure to stabilize their repetitive controller and guarantee the robustness to load disturbances, which yields a good nonlinear load performance in simulation. Zhang et al. have performed consistent research on repetitive control of single-phase half-bridge inverters. In their work [116], a standard single loop repetitive controller has been designed and implemented in discrete-time, which yields acceptable steady state performance but slow transient response. The authors have continued their work in [117], where a state feedback plus integral controller has been added to provide better response to instantaneous disturbances and the idea has been proved effective by the presented results. However, no systematical stabilizing technique is given in [117].

Different from repetitive control, internal model principle can be used only to eliminate periodical tracking error and disturbance with specified frequency, which is generally enough for inverter control for DG applications since THD is nearly caused by low order harmonics. All works in this area take advantage of the concept of *generalized integrator* [63] which expands the functionality of the integral term of a PI controller in dc to multiple frequency components in the same reference frame.

Escobar et al. [30, 31, 109] and Mattavelli et al. [72] have developed a servo controller concept which includes modes of tracking error or disturbance to be eliminated. This type of servo controller applies gains only on specified frequency components to suppress them to zero. However, ripples still can be seen on their test waveforms under nonlinear load. Sato et al. [94] have proposed a similar approach but with a *resonant*

regulator concept and implemented it in discrete-time. Loh et al. [64] have introduced a resonant filter which applies infinite gain on specified frequency components and suppress other frequencies. This filter is used combined with a PID controller and yields acceptable results under nonlinear load. Fukuda et al. [34] have expanded the same idea in their inverter controller in that the integral term in a conventional PI control remains to cope with dc errors while the resonant terms in the controller are used to eliminate steady state errors of ac components. This solution can be called *expanded stationary frame PI control*. The contribution of Zmood et al. in [122] is establishing mapping PI controllers in synchronous reference frames to a stationary reference frame with multiple frequency components included. Zmood et al. [121] have expanded the *resonant regulator* concept by adding a damping term in the transfer function of the resonant filters allowing control of sensitivity and frequency response of the filters. Mattavelli [71] has proposed an approach combining PI controllers in both synchronous and stationary reference frames, using the synchronous reference frame to control the fundamental component and the stationary reference frame with resonant regulation to control the harmonics, which makes the solution very complex.

Marwali et al. [70] have combined the above servo controller and linear quadratic optimization in their control approach for a three-phase inverter. This approach is based on the robust servomechanism control theory proposed by Davison et al. [24]. The control in [70] yields a THD of 2.7% under nonlinear load with a crest factor of 3:1, which is satisfactory.

Intelligent control

Besides above conventional control, intelligent control has also been applied to inverter control. Guo et al. [36] have developed a fuzzy logic controller for voltage loop regulation which yields an acceptable performance. However, the control rules are based on empirical knowledge which cannot be obtained directly.

1.2.2 The system topology

All three-phase inverters involved in the above publications are all in a three-phase three-wire system where the inverter itself does not provide a neutral point. Typically a Δ/Y_g transformer is used with the secondary center grounded before the inverter powering the load or being connected to utility grid as shown in Figure 2.14. In this topology, the three-wire system on the Δ side only has two independent dimensions and 0-axis current cannot flow, which makes the system relatively easy to control. The drawback is the existence of the costly, heavy, and bulky transformer. Chu [19] has summarized multiple grounding topologies for inverter systems, where a three-phase four-wire inverter topology with the center of the dc bus grounded is mentioned as shown in Figure 1.2. The benefit of this topology is that the undesirable transformer can be removed. Dedicated research on control of this topology has not seen in literature, besides this three-phase four-wire system can also be considered

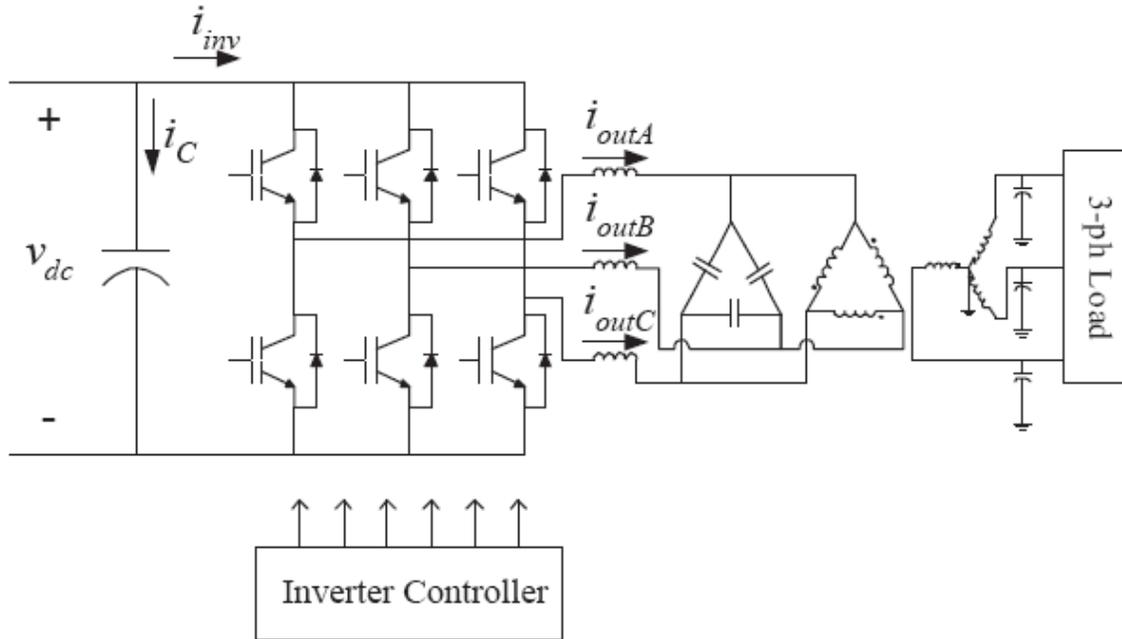


Figure 1.1: The three-phase three-wire inverter topology.

three independent single-phase half bridge inverters which have been addressed in many publications as shown in Figure 1.3. Therefore, control of such transformerless inverter topology on basis of three-phase systems warrants further investigation.

Another three-phase four-wire transformerless inverter topology also exists - the three-phase four-leg inverter shown in Figure 1.4. Unlike the split dc bus topology as mentioned above, the four-leg inverter uses a fourth leg whose mid-point is used as the neutral point of the inverter. This topology is equivalent to combining three full bridge single-phase inverters together as shown in Figure 1.5 with a shared neutral leg. Zhang et al. [118] have developed a three-dimensional space vector PWM technique for a four-leg inverter. El-Barbari et al. [28], Ma et al. [66], Hou et al. [40], and Li et al. [58] have proposed control techniques for this type of inverter topology. Compare to the split dc bus topology, a four-leg inverter has better dc bus voltage utilization,

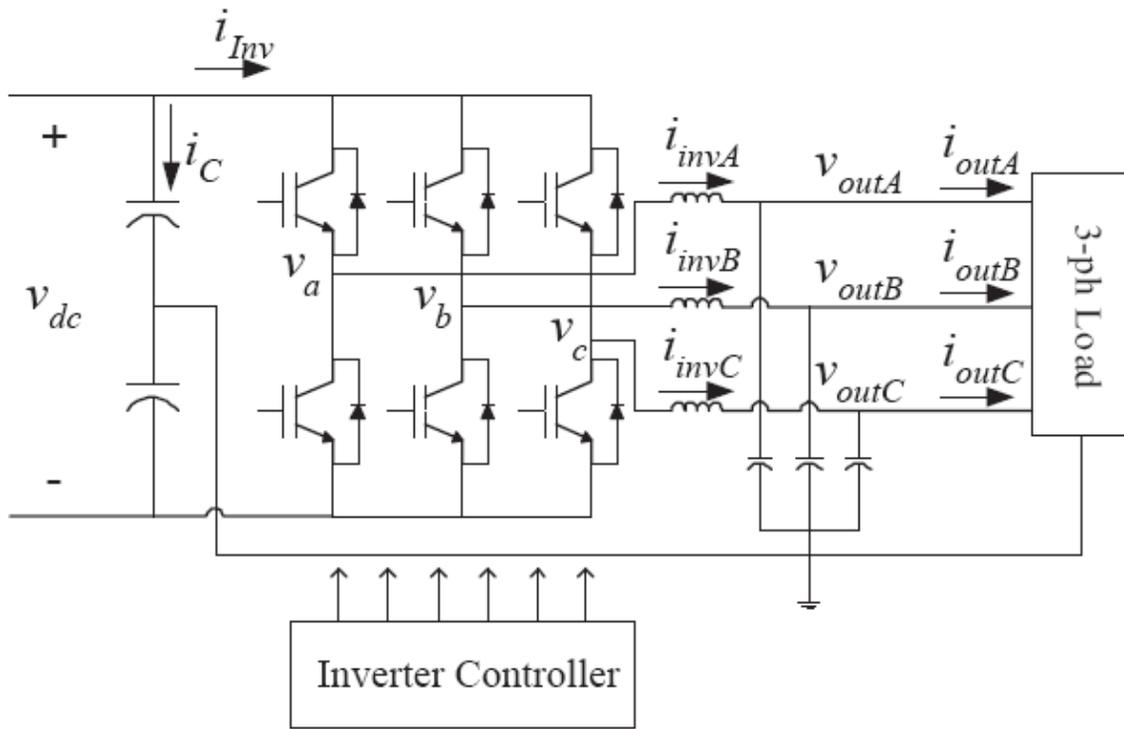


Figure 1.2: The three-phase four-wire split dc bus inverter topology.

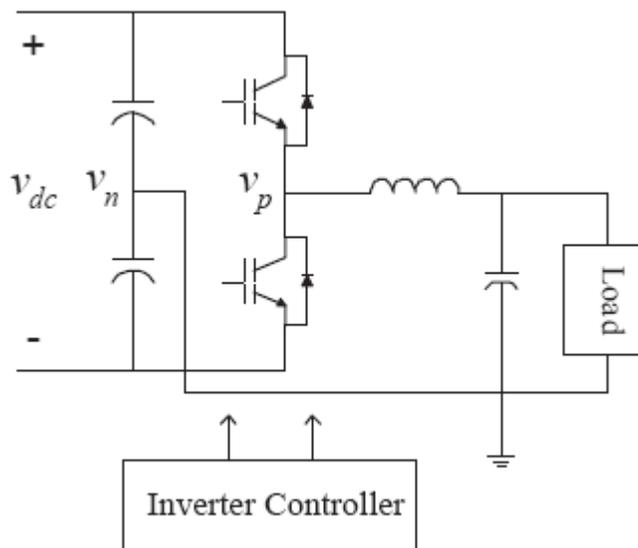


Figure 1.3: A single-phase half-bridge inverter.

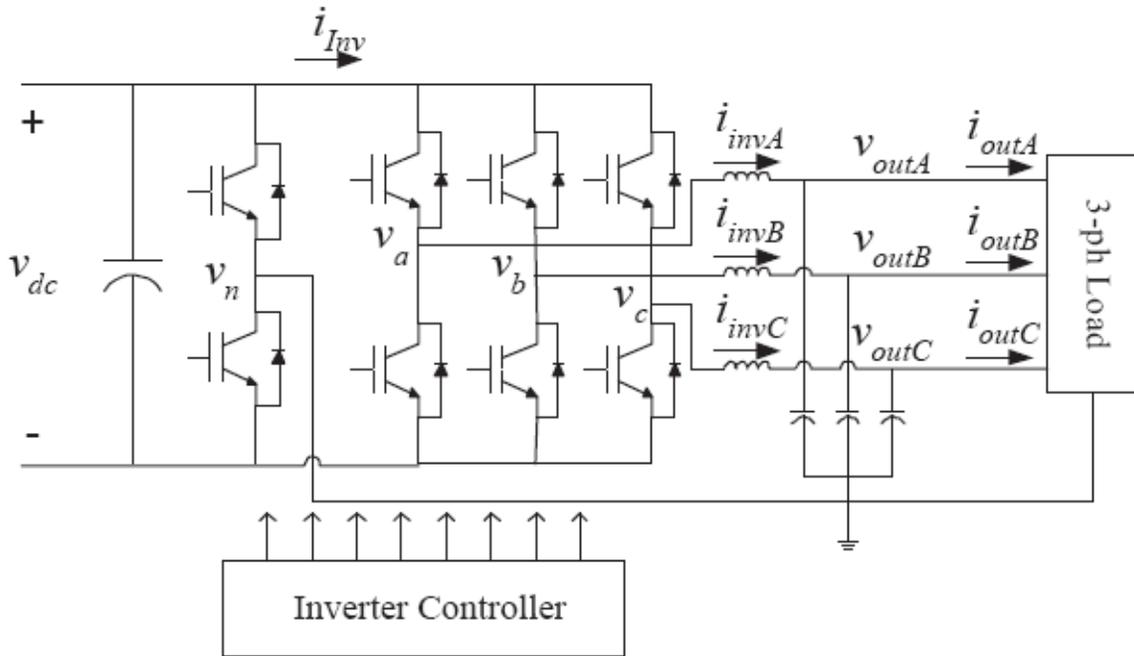


Figure 1.4: The three-phase four-leg inverter topology.

require less dc bus voltage regulation, and better common mode current control while it uses two more power switches and involves more complex control and modulation techniques.

1.2.3 Robust stability issues

A feedback control system is said to achieve robust stability if it remains stable for all considered perturbations in the plant. In feedback controlled PWM inverter systems, e.g., an inverter based three-phase distributed generation unit operated in island mode, load disturbance, noise, and parametric uncertainty of the electrical

components in the circuit are the major plant perturbations that have significant impacts on both system stability and performance and therefore warrant detailed investigation.

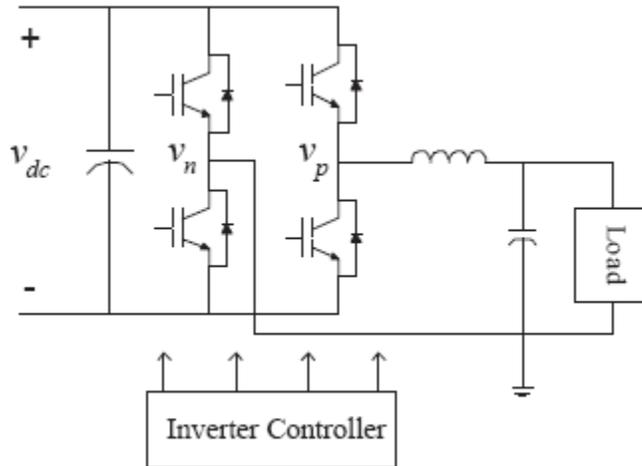


Figure 1.5: A single-phase full bridge inverter.

Robust stability related topics about power converter control systems have been addressed in literature. Czarkowski et al. [20] have studied a state feedback control method of a PWM dc-dc converter for its robust stability under parametric uncertainty. This study uses the Kharitonov's theorem [83] which checks whether the feedback system is stable by applying the Routh-Hurwitz stability tests but does not tell the stability margin or how stable the system is. GrÄundling et al. [35] have developed a robust model reference adaptive control technique for uninterruptible power supplies (UPS) which was expected to handle model inaccuracy but no robust stability property of the technique was presented. Lee et al. [56] have proposed an H_∞ loop-shaping robust controller design technique for UPS with robust stability

analysis. However, this technique does not perform well under nonlinear load, which significantly undermines its value for power supply applications. Lin et al. [62] have designed a dc-dc power converter controller using structured singular value (μ) concept which evaluates how stable the system is under the worst case of perturbation. This study uses admittance instead of resistance to model the dc load, which is proved convenient in the analysis. However, this design only considers load disturbances and no parametric uncertainties are included in the perturbation. Mohamed [75] has proposed a robust controller for a current source inverter (CSI) fed induction motor drive. Both H_∞ loop-shaping and μ -analysis techniques are applied in the research but no parametric uncertainty is considered which undermines the strength. Ye et al. [114] have proposed a robust controller design method for high frequency resonant inverters. This approach applies H_∞ robust controller synthesis method provided in Matlab Robust Control Toolbox but only includes load and external input voltage in the perturbation. Marwali et al. [69] have performed research on the robust stability of a voltage and current controller for a three-phase three-wire DG unit. This study takes advantage of μ -analysis and considers both the load disturbance and parametric uncertainty as perturbations. The analysis result shows the stability margin under perturbations and provides guideline in the controller gain tuning. No robust stability analysis has been reported for three-phase four-wire inverters.

1.2.4 Pulse width modulation techniques

Pulse width modulation (PWM) is an essential but not only technique to control

a switched-mode power converter using self-commutated devices, including the dc/ac inverter and ac/dc rectifier mentioned above. Alternative modulation techniques include hysteresis technique and delta modulation [1] where the switching frequency is not a constant, which tends to cause harmonic distortions in its output waveform and therefore limits the application of such techniques.

A number of PWM techniques have been developed and used in power converter controls to generate sinusoidal waveforms. However, only three of them have become standards and most often been applied into practice - naturally sampled sine PWM (NSPWM), uniformly or regularly sampled sine PWM (USPWM), and space vector PWM (SVPWM).

NSPWM uses a modulation signal, i.e., the sine wave, to be compared to a high frequency carrier, i.e., a triangle waveform, and the compare result which is a logic signal is used to determine the ON or OFF state of the power switches. NSPWM does not control the position of the pulses it generates in each cycle and the minimum pulse width is not controlled. USPWM still uses a triangle carrier signal at switching frequency but it only uses the comparison result to determine the ON or OFF duration of the switches but not the pulse position. The pulse position is uniformly controlled, e.g., put at the center of each switching cycle. SVPWM maps eight switching patterns of a three-phase full bridge converter into six 60 deg. apart space vectors on the same plane and two 0-axis vectors perpendicular to the plane and a reference vector on the plane is used as modulation signal and determines the time average of these switching patterns in each PWM cycle. If the reference vector rotates on the plane from sector

to sector, a sine wave is modulated in the pulses. This SVPWM technique was first proposed by van der Broeck [110] in 1988.

Since then, many researches have been conducted to analyze the performance of SVPWM. Boys et al. [11] and Moynihan et al. [79] have developed two different spectra formula for SVPWM which help to analyze the harmonics of the modulation technique. The spectra of NSPWM has been given by Wood [113]. Zhou et al. [120] have analyzed the relationship between SVPWM and USPWM in multiple aspects and provided a bidirectional bridge for the transformation between the two. Bowes et al. [10] and Kwasinski et al. [49] have compared the performances between SVPWM and USPWM and concluded that USPWM can be as good as SVPWM if an additional 0-sequence signal is injected into the modulation signal. Injection of 0-sequence component can extend the linear modulation range and reduce THD.

Blasko [7] have proposed an idea and measures to utilized the third degree of freedom in SVPWM by changing the magnitudes of two 0-axis vectors. This change allows control of 0-axis quantities. Lee et al. [52] have proposed a practical application of Blasko's theory in a rectifier-inverter system for motor drive where the 0-axis leakage current can be minimized. No practice of this theory in a three-phase four-wire system has been reported.

All inverter control techniques listed in Section 1.2.1 are based on an assumption that the dc bus voltage is fixed, well regulated, or its change does not affect the control

on the load side. However, this assumption is not always true in DG environment where fuel cells, wind generators, or photovoltaic modules could be the source with an unregulated or poorly regulated dc voltage. Even though in most case, a properly developed PWM scheme can compensate for the dc bus voltage change inherently so that the load side cannot see any effect of the dc voltage change, this change may still undermine the performance of PWM inverter under some situations. Shireen et al. [96] have addressed this problem and developed a modulation correction technique to overcome it.

1.2.5 Line-interactive operation of inverters and control of P and Q

Line-interactive inverters for harmonic current compensation

Control issues of line-interactive inverter systems with a local load have been addressed by a number of researchers focusing on the active filtering capability of the inverter which compensates for the effect of harmonic corrupted load current by pumping compensating current into the power system through real-time control. In this type of applications, the goal is to make the current dragged from power system, i.e., the line current, as sinusoidal as possible.

Takeshita et al. [101] have developed a PI based inverter controller which compensates both the line current and the terminal voltage, but the current compensation performance shown in their experimental results is poor. Dehbonei et al. [25] have proposed a inverter control technique for photovoltaic systems connected with utility

grid, which uses standard space vector PWM with only a linear local load. Qin et al. [88] have presented a notch filter harmonic elimination technique with a diode rectifier load. Neither experimental result in [25] and [88] is satisfactory from THD point of view. Cheung et al. [17] have developed an instantaneous harmonic current compensation technique which yields relatively good line current compensation result. A special topology, so called series-parallel topology, which utilizes power dragged from utility grid through a rectifier to condition the utility line current through an inverter. The rectifier is connected to the utility grid through a transformer in series with the power line and the inverter is paralleled with the power line and this is how the topology is named. This concept was first introduced by Rathmann et al. [90] in 1996 without a well addressed control technique. Since then, a few other researchers have put efforts on this topic and produced some meaningful results. Kwon et al. [50] have proposed a single-phase system based on this topology with a proportional control and Lee et al. [54] have presented a PI controller based technique for a 3-ph system, both of which yield good active filtering results. Da Silva et al. [21 {23] have put quite much effort in analyzing this topology and presented a series results based on PI control technique, which show the effectiveness for both linear and nonlinear local load.

Current quality of line-interactive inverters

When an inverter is connected to power system, the terminal voltage is governed by the power system but the current waveform is still controllable.

Naik et al. [80] have developed a 3-ph thyristor full bridge interface for connecting

DG units to utility grid. The current waveform shows 6 spikes per cycle at commutation of the thyristors. Qiao et al. [86] have presented a current control technique which incorporates a special designed inverter firing logic different from typical PWM techniques. Even though the authors claim the inverter can control the current at unity power factor but the current waveforms in the experimental results are unsatisfactory. Abdel-Rahim et al. [2] have proposed a model based control technique for a grid connected inverter. In this research, a coupling inductor is applied between the inverter output and the power system. With knowledge of the inductance and the utility voltage, a state space model is constructed which leads to a model based current control. The simulation result shows clean sinusoidal waveforms.

Power control of line-interactive inverters

Although current waveform control is one of the goals of the line-interactive inverter control, power control, including P and Q controls, is the eventual objective to be achieved by a power electronics interface in DG environment.

As early as 1984, Key [44] pointed out that future grid-connected switched-mode inverters can provide a compatible utility interface. Since that time, Wall [111] has addressed a number of differences between an inverter interfaced DG unit and a synchronous generator in power system operation under normal, island, and fault conditions. Thomas et al. [104] have concluded that DG may have significant impact on power system stability if not properly compensated in reactive power, and Donnelly et al.'s [27] research has shown that DG could have significant impacts on transmission system stability at heavy penetration levels, where penetration is defined as the

percentage of DG power in total load power in the system. A DG unit affects the system stability by generating or consuming active and reactive power. Therefore, power control performance of the DG unit determines its impact on the utility grid it connects to. If the power control performs well, the DG unit can be used as means to enhance the system stability and improve power quality; otherwise it could undermine the system stability.

Line-interactive uninterruptible power supply (UPS) is able to pick up the load at power system failure and reverse power flow direction to battery charging when the power line is restored as addressed in the work of Chandorkar et al. [14]. However, the power flow control in line-interactive UPS does not match the requirement of DG systems by far.

Abdel-Rahim et al. [3] have developed a line-interactive inverter control technique which allows a certain output power factor setting. Similarly, Rajagopalan et al. [89] have presented an inverter control allows some P and Q setting when it is connected to power system. However, neither of them has closed loop power control for arbitrary P and Q tracking. Teodorescu et al. [103] have proposed a three-phase ac-dc-ac power conversion system interfacing small wind turbines to utility grid. This system has been developed for both island and grid-connected operations. However, major endeavor has been used in island mode control. Although a current control approach under grid-connected mode has been presented, no power control behavior has been addressed and evaluated.

In 1987, Kalaitzakis et al. [42] first introduced the power control concept for synchronous generator paralleled with power system into the application of grid connected inverters, that active power P can be controlled by adjusting phase angle of output voltage and reactive power Q can be controlled by adjusting magnitude of output voltage. Since then, Chandorkar et al. [13] have developed an inverter control technique for line-interactive operation where P and Q can be separately controlled through closed-loop control, and Sedghisigarchi et al. [95] have performed a simulation research on P and Q dynamic control under reclosing operating condition although its control strategy is poorly addressed and the transient response is slow.

Yu et al. [115] have studied four different line current control techniques for three-phase line-interactive inverters with a series-parallel topology in a unified power flow controller (UPFC), in which a PI plus dq -axis decoupling method yields a good real and reactive power response. Experimental results on a 1 kW level have been presented to show the power flow control performance. However, due to the topology issue, this technique is difficult to be implanted into a typical DG unit where high performances in both island mode and grid-connected mode are required.

Liang et al. [59] have presented a power control method for a grid-connected voltage source inverter which achieves good P and Q decoupling and fast power response. However, this approach requires an interface inductor to be connected between the DG output terminal and power system, whose inductance value is assumed known. The existence of the interface inductor force greater voltage magnitude change at the DG terminal to perform certain regulations of the utility P and Q . If this inductor

is taken out, since knowledge of the value of power system equivalent impedance is not available in practical applications, this approach would not work anymore. Even though the possible error in the power factor angle of the impedance has been considered, it is the magnitude of the impedance that truly causes the sensitivity of P and Q responses, which is however not addressed. Therefore, the effectiveness of the control approach claimed in [59] is seriously undermined.

Illindala et al. [41] have presented a different power control strategy based on frequency and voltage droop characteristics of power transmission, which allows decoupling of P and Q at steady state. In this method, power regulation errors ΔP and ΔQ are used to generate output voltage phase angle and magnitude changes respectively, which decouples P and Q controls in steady state. Unfortunately, the presented simulation result does not show a satisfactory performance in response time and control magnitude which could be caused by low feedback gain and implies that higher gain may cause problems.

About Newton-Raphson Method

Newton-Raphson Method, is a iterative root-finding algorithm that uses the first few terms of the Taylor series of a function $f(x)$ in the vicinity of a suspected root. Newton-Raphson Method is widely used in solving power flow problems due to its fast convergence property, such as in El-Khattam et al.'s work [29]. This technique has also been used in line-interactive power converter systems. Fan et al. [32] have performed power flow analysis in a power system involving ac-dc-ac switch mode power converters where a modified Newton-Raphson Method is used as the power

flow solver. Lee et al. [53] and Wei et al. [112] have used Newton-Raphson Method to solve for voltage magnitude and phase angle of a unified power flow controller (UPFC). Sundareswaran et al. [99] have used Newton-Raphson Method to solve for optimized switching pattern of a PWM ac chopper. In the above applications, Newton-Raphson Method is only used as an off-line solver for the specific mathematical problems. No on-line application of the method for real-time control purpose has been reported.

1.2.6 Front-end rectifier control in controlled ac-dc-ac systems

If we look one step back toward the feeder of the inverter dc bus, we can find that a significant portion of the feeders are controlled ac/dc rectifiers. In DG environment, the input ac source can be any gas or wind turbine driven generators or other ac systems. No matter what source is used, balanced 3-ph input current with low THD is desired, which is so called power factor correction (PFC).

There are many existing PFC rectifier topologies. For high power applications, especially when high performance is required, continuous conducting mode (CCM) boost rectifier is usually used [68] due to its high efficiency, good current quality, and low EMI emissions. A standard CCM boost rectifier has a full bridge topology, exactly identical to a three-phase full bridge inverter. This type of rectifier is controlled by an outer dc voltage control loop and an inner input current control loop, where the voltage regulation error is used to generate the input current command for the inner loop. When the dc voltage is boosted, i.e., greater than the input line voltage

amplitude, this rectifier yields excellent control performance. The CCM boost rectifier is also called PWM rectifier, boost rectifier, or controlled rectifier in literature.

In three-phase four-wire systems, a split dc bus inverter topology can maximize its performance with a three-level controlled rectifier regulating both the top and bottom half voltages of the dc bus. A full-bridge CCM boost rectifier as discussed above can serve the purpose with a modified voltage regulation scheme based on the standard approach described above. Besides the full bridge topology, VIENNA rectifier topologies can also be used. A VIENNA rectifier is a three-phase three-level rectifier based on a traditional uncontrolled diode rectifier with additional input inductors and six active power switches to achieve the neutral point voltage control. Detailed operation and control of VIENNA rectifiers have been reported by Kolar et al. [48] and Qiao et al. [87]. A drawback of the VIENNA rectifiers compared to the full bridge topology is that it does not allow bi-directional power flow.

In three-phase three-wire systems, if a full bridge controlled rectifier is used together with an inverter, the impact from the inverter side needs to be taken care of for better control of the rectifier. One typical impact frequently seen is unbalanced load on the inverter side.

Although this particular problem has not been addressed in literature, related research has been conducted on rectifier control under unbalanced input voltage conditions [18, 78, 93, 98]. Kamran et al. [43] have mentioned dc voltage ripple problem caused by either unbalanced inverter load current or unbalanced input voltage supply. However, their control goal was to minimize the dc link voltage ripple instead of

improving the input power quality.

Some other researches have focused on improving instantaneous power balance between the input and output of a rectifier-inverter system and minimizing the dc coupling capacitance to reduce the cost [46, 61, 67, 102, 107]. The less the dc coupling capacitance is, the better instantaneous power balance the system could yield. However, this is only desirable under balanced load. Once the inverter load is unbalanced, it is apparent that the steady state inverter output power is no longer a constant, and neither is the inverter input dc power.

A switching function concept for power converters has been used in [18, 78, 98] to show the existence of harmonics in dc bus voltage. However, none of these works quantified the harmonic components analytically and used the result to analyze the ripple problem mentioned above.

1.2.7 Summary

The above literature review has covered control related issues in major aspects of single-unit operation of switching mode utility interface for DG systems.

Single unit voltage and current control is the the basis for DG unit operations in either island mode or grid-connected mode. Many control theories have been applied in this area and it has turned out that sliding mode control and internal model principle based controls yield better performance under nonlinear load disturbances. Although multiple rotating reference frame techniques can handle the harmonic load disturbances, the stationary reference frame based techniques yield the same perfor-

mance while cost less overhead.

Although the four-leg inverter topology in a three-phase four-wire system performs better than a split dc bus topology in some aspects, the latter requires easier control and uses less power switches and therefore remains an option and warrants further investigations.

The robust stability of an inverter control technique is an important issue in practice given parametric uncertainties and load disturbances. Structured singular value μ -based analysis provides evaluation of closed-loop robust stability and the stability margin information and hence can be used as a guideline for control gain tuning.

Uniformly sampled PWM can be made identical to space vector PWM with 0-axis signal injection. Space vector PWM can perform 0-axis control if magnitudes of the two 0-axis vectors are made different. This allows SVPWM to be used in three-phase four-wire systems but such application has not been seen in literature.

Power control of a DG unit is necessary under grid-connected running mode.

Experimental results about line-interactive inverters are only seen for active filtering purpose or united power flow controller (UPFC) topologies in the literature while those for power control of DG with local load have not been seen in publications.

Newton-Raphson Method is known as a good nonlinear equation solving tool and widely used in power flow problems, including switching mode power converter involved problems, all of which are performed off-line.

As far as the front-end source of a DG unit is concerned, a controlled rectifier should not only provide well regulated dc voltage but also perform PFC and take balanced input current. In a three-phase three-wire system, unbalanced inverter load may introduce ripple on the dc bus and cause unbalanced input current problem for the rectifier but no further solution has been reported.

1.3 Problem Statement

The above literature review shows that given the existing research results, the following problems about switch-mode inverter based DG interface warrant further investigation - in island mode, the voltage control problem of a DG inverter with three-phase four-wire transformerless topology for quality power supply to the local load; in grid-connected mode, the real and reactive power flow control problem in existence of local load; and in a three-phase three-wire ac-dc-ac system, the front-end PFC rectifier control problem with unbalanced inverter load. In this report research, all of the above problems will be addressed by proposing a series of new solutions with detailed analysis, simulations, and experimental results.

1.3.1 Voltage and current control of a three-phase four-wire

DG unit in island mode

A three-phase three-leg inverter with split dc bus is one topology to implement

three-phase four-wire system with a neutral point seen by the load. Compared to a three-phase three-wire system, it does not have the isolation transformer and provides three-dimensional control. Compared to a three-phase four-leg topology, it saves two power switches and reduces control complexity. Therefore the control problem of the three-phase three-leg inverter with split dc bus deserves detailed research for its best possible performance.

Although a three-phase three-leg inverter with split dc bus topology is a combination of three half bridge single-phase inverters and control techniques designed for single-phase inverters still work in the three-phase systems, new control problems emerge after the three phases are combined together in that the reference frame issue and the PWM issue become problems. In this report, control to be performed in synchronous $\alpha\beta 0$ reference frame is suggested together with a new modified space vector PWM scheme.

Besides, in this report, the common control problems shared by both the three-phase system and the single-phase half bridge topology will also be addressed by presenting a new control solution with detailed analysis of its performances and robust stability.

1.3.2 Power control of DG in grid-connected mode

Power control, including real power P and reactive power Q controls, of a DG inverter in grid-connected mode with existence of local load is of interest. The chal-

lenges come from the fact that the system should also be able to supply quality power to the local load in island mode. Based on this fact, control solutions yielding stability, fast transient response, and less coupling between P and Q are desired. Previous research has shown that knowledge about the utility grid helps the control of DG unit in transients. There has not been any published work addressing the methodology of obtaining the knowledge of the grid and apply the knowledge in DG control in real-time. In this report, a power system parameter identification technique and a feedforward control technique applying the system identification results for real-time implementation will be presented.

If the local load of the DG unit is nonlinear, e.g., diode rectifier sort of load, it tends to draw harmonic current for the feeder. In island mode, the DG unit is the only feeder. However, in grid-connected mode, how the harmonic current is shared by the DG unit and grid becomes a concern. Harmonic free line current is always desired and how to let the DG unit take all the harmonic current is an important problem. In this report, the power control technique proposed will address this problem.

In practice, the voltage of utility grid is often somewhat harmonic distorted.

Whether the DG unit can identify the harmonic components in the grid voltage and compensate for them to maintain clean sinusoidal line current becomes a challenge.

In this report, a mechanism coping with this situation will be proposed.

In most cases, from the power control point of view, the inverter topology does not matter. In this report research, a three-phase three-wire inverter with an output

isolation transformer will be used as the DG unit interfacing with the utility grid since it allows two-dimensional control which is simpler than three-dimensional control in a four-wire system. The limitation of the two-dimensional topology is that it does not provide zero sequence control and hence cannot maintain balanced three-phase line currents given unbalanced grid voltages.

1.3.3 Front-end rectifier control in three-phase three-wire ac-dc-ac systems

If a front-end PFC rectifier exists in a three-phase three-wire ac-dc-ac double conversion system, once the inverter load is not balanced, the output power is no longer a constant, which leads to fluctuation of the dc link voltage. On the rectifier side, the ripple corrupted dc link voltage is fed back to the voltage regulator which generates a fluctuating d -axis current command under a constant dc voltage reference. If the current regulator of d -axis has high bandwidth, it yields fast current tracking and consequently a fluctuating rectifier output current which causes unbalanced front-end input current in the input current. This situation is undesirable no matter the front-end is fed by a power system or a single generator.

In this report, the effects of unbalanced inverter load on the dc bus will be analyzed and evaluated. A rectifier control philosophy with a method solving this problem will be proposed accordingly.

1.4 Organization of the Report

After this introduction chapter, the report is organized in the following structure:

Chapter 2 will address the voltage and current control of a three-phase four-wire DG unit with a split dc bus topology. The control technique is a combination of robust servomechanism control and discrete-time sliding mode control in stationary $\alpha\beta 0$ reference frame. A modified space vector pulse width modulation (MSVPWM) technique will be presented. The control performance will be evaluated in both time-domain simulation and experiments plus frequency domain analysis. The robust stability of the proposed approach will be analyzed using structured singular value μ -analysis technique.

Chapter 3 will cover the grid-connected operation problems. A Newton-Raphson Method based on-line power system parameter identification technique will be proposed to obtain the Thevenin parameters of the utility grid in real-time. A Newton-Raphson Method based feedforward controller will be proposed on top of a conventional integral power controller to achieve better power control performance in transients. A phase-locked loop based harmonic identifying algorithm will also be presented to handle the harmonic corrupted grid voltages and maintain harmonic free line currents. Both simulation and experimental results will be presented.

Chapter 4 will discuss the front-end rectifier control problem in a three-phase

three-wire system with unbalanced inverter load. A switching function concept will be used under standard space vector PWM to quantify the harmonic components in the dc link. According to the analysis result, a notch filter will be designed and applied to eliminate the undesired harmonic component from the feedback signal. The proposed controller with the notch filter will yield constant rectifier power under steady state and balanced three-phase input currents while still exhibit fast response to load transients. Both simulation and experimental results will be presented.

Chapter 5-7 gives technical details associated to the analytical and experimental implementations of the techniques proposed by the above chapters, including schematics and source code listings and some are available only in electronic version.

Chapter 8 concludes the report.

CHAPTER 2

VOLTAGE AND CURRENT CONTROL OF A THREE-PHASE FOUR-WIRE DG INVERTER IN ISLAND MODE

2.1 The Control Plant Modeling

The three-phase four-wire DG unit studied in this report has a topology shown in Figure 2.1. In this circuit, the dc bus voltage is assumed to be ideal dc voltage source, which can be implemented by a dc-voltage-regulated front end supplied by any distributed sources, including fuel cells, photovoltaic devices, wind turbines, gas turbines, etc. The control issues of the inverter will be discussed in this chapter. The inverter has a three-phase three-leg plus split dc bus topology. A full bridge front-end PFC boost rectifier is assumed to provide regulated dc bus voltage evenly split on the top and bottom halves. The inverter outputs are connected to a three-phase second order $L-C$ filter and the filter output voltage is supplied to the load. The control goal of a DG unit in island mode is low steady state voltage tracking error, low total harmonic distortion (THD) in the output voltage waveforms, and fast transient response to load disturbances under various types of load. A new control technique achieving this goal for the DG unit topology will be presented.

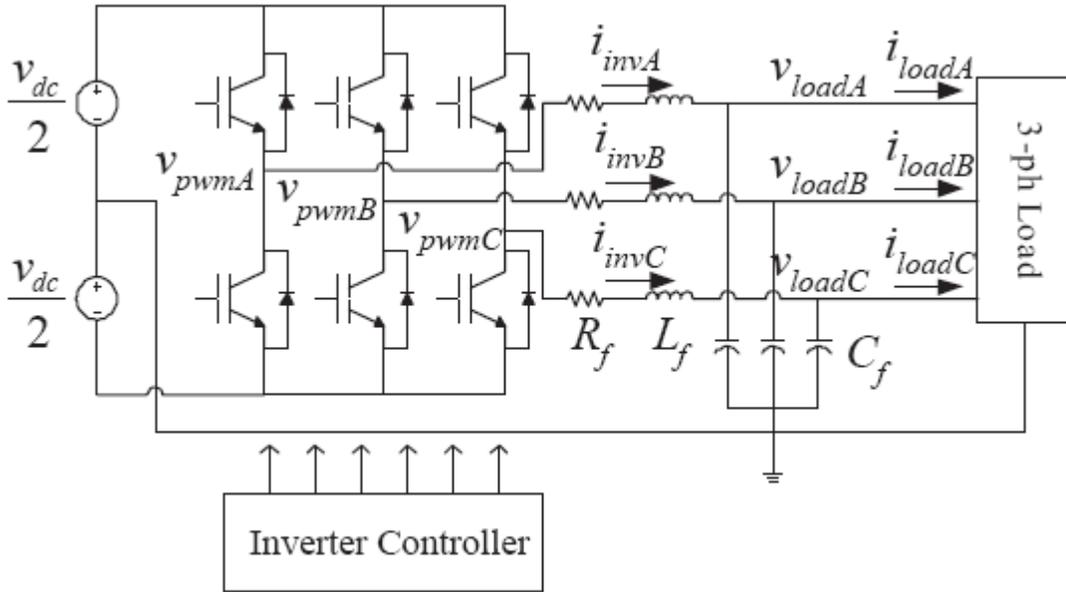


Figure 2.1: The three-phase four-wire inverter with a split dc bus.

2.1.1 The basic circuit equations

The circuit defined in Figure 2.1 uses the following quantities to describe its behavior. The three-phase inverter output line-to-neutral PWM voltages are v_{pwmA} , v_{pwmB} , and v_{pwmC} and can be represented by vector

$$V_{pwm} = [v_{pwmA} \quad v_{pwmB} \quad v_{pwmC}]^T .$$

The three-phase inverter output currents, which also flow through the filter inductor, are i_{invA} , i_{invB} , and i_{invC} and can be represented by vector

$$I_{inv} = [i_{invA} \quad i_{invB} \quad i_{invC}]^T .$$

The three-phase load voltages, v_{loadA} , v_{loadB} , and v_{loadC} , are the same as the filter capacitor voltages and can be represented by vector

$$V_{load} = [v_{loadA} \quad v_{loadB} \quad v_{loadC}]^T .$$

Figure 2.2: Clarke's stationary $\alpha\beta 0$ stationary reference frame.

The three-phase load currents, i_{loadA} , i_{loadB} , and i_{loadC} , can be represented by vector

$$I_{load} = [i_{loadA} \quad i_{loadB} \quad i_{loadC}]^T .$$

Given the filter series resistance R_f , inductance L_f and capacitance C_f , the system is governed by the following equations

$$\dot{V}_{load} = \frac{1}{C_f} I_{inv} - \frac{1}{C_f} I_{load}, \quad (2.1)$$

$$\dot{I}_{inv} = \frac{1}{L_f} V_{pwm} - \frac{R_f}{L_f} I_{inv} - \frac{1}{L_f} V_{load}. \quad (2.2)$$

2.1.2 Transform the model into stationary reference frame

In this research, the control will be performed in Clarke's stationary $\alpha\beta 0$ reference frame defined in Figure 2.2, where the 0-axis is orthogonal to the paper plane, and

$$f_{\alpha\beta 0} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} f_{ABC} \triangleq T_{\alpha\beta 0} f_{ABC}, \quad (2.3)$$

where f_{ABC} is any vector defined in ABC reference frame, $f_{\alpha\beta 0}$ is its counterpart in $\alpha\beta 0$ reference frame, and the matrix $T_{\alpha\beta 0}$ is defined as the transformation matrix from ABC to $\alpha\beta 0$.

Apply this reference frame transformation to Equations 2.1 and 2.2, it can be obtained that

$$\dot{V}_{load,\alpha\beta 0} = \frac{1}{C_f} I_{inv,\alpha\beta 0} - \frac{1}{C_f} I_{load,\alpha\beta 0}, \quad (2.4)$$

and

$$\dot{I}_{inv,\alpha\beta 0} = \frac{1}{L_f} V_{pwm,\alpha\beta 0} - \frac{R_f}{L_f} I_{inv,\alpha\beta 0} - \frac{1}{L_f} V_{load,\alpha\beta 0}. \quad (2.5)$$

It can be observed from Equations 2.4 and 2.5 that all dimensions, i.e., α , β and 0, share the identical dynamics and there is no coupling between any two of the three dimensions. Therefore, without losing generality, the three dimensional system can be reduced into an equivalent one dimensional system for convenience in further analysis and control strategy development. In the reduced one dimensional equivalent system as shown in Figure 2.3, the load voltage is denoted by $v_{load;eq}$, the inverter current is denoted by $i_{inv;eq}$, the load current is denoted by $i_{load;eq}$, and the inverter PWM voltage can be denoted by $v_{pwm;eq}$. The system equations become

$$\dot{v}_{load,eq} = \frac{1}{C_f} i_{inv,eq} - \frac{1}{C_f} i_{load,eq}, \quad (2.6)$$

and

$$\dot{i}_{inv,eq} = \frac{1}{L_f} v_{pwm,eq} - \frac{R_f}{L_f} i_{inv,eq} - \frac{1}{L_f} v_{load,eq}. \quad (2.7)$$

It can be observed from Figure 2.3 that this one dimensional equivalent circuit is exactly the same as one phase of the original three-phase model. Here comes a question, about why it is necessary to do the stationary reference frame transformation.

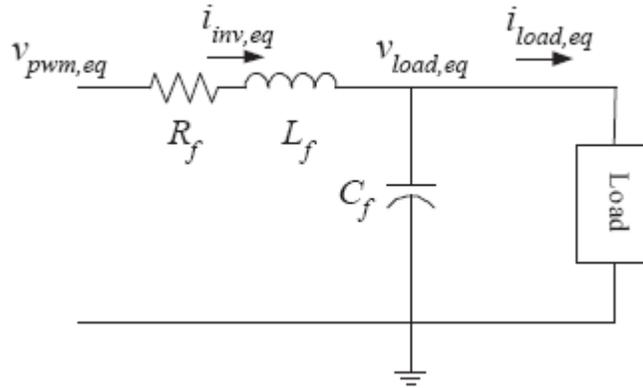


Figure 2.3: The one dimensional equivalent model of the inverter system.

This question can be answered as follows. The stationary reference frame transformation is used to transform three-phase quantities from original ABC reference frame into Clarke's $\alpha\beta 0$ reference frame and all following control strategy will be developed in this reference frame. It is true that there is no difference in the circuit parameters between the one dimensional equivalent model and one phase of the three-phase orig-

inal circuit. However, the system dynamics is described using $\alpha\beta 0$ quantities rather than ABC quantities in the one dimensional equivalent model compared to the case of one phase in the three-phase original circuit. More detailed discussion about the differences of conducting control in these two reference frames and the advantage of the stationary $\alpha\beta 0$ reference frame will be presented in later sections.

2.1.3 Convert to per-unit system

For the conveniences of implementation of control algorithms in fix-point micro-processors and analyzing the control performance, it is beneficial to convert the system model into a per-unit system where all variables and parameters are normalized.

Given system rated apparent power S_{rated} and rated output line-to-neutral RMS voltage V_{rated} , the base values can be derived as follows:

$S_b =$

$$S_b = \frac{1}{3} S_{rated},$$

$$V_b = \sqrt{2} V_{rated},$$

$$I_b = \sqrt{2} \frac{S_b}{V_{rated}},$$

and

$$Z_b = \frac{V_b}{I_b}.$$

Based on the base values and with v_{load} representing the per-unit load voltage, i_{inv} representing the per-unit inverter current, i_{load} representing the per-unit load current, and v_{pwm} representing the per-unit inverter PWM voltage, the per-unit variables can be obtained as follows:

$$v_{load} = \frac{v_{load,eq}}{V_b},$$

$$i_{inv} = \frac{i_{inv,eq}}{I_b},$$

$$i_{load} = \frac{i_{load,eq}}{I_b},$$

and

$$v_{pwm} = \frac{v_{pwm,eq}}{V_b}.$$

The circuit parameters should also be converted into the per-unit system. Let R represent the per-unit filter resistance, L represent the per-unit filter inductance, and C represent the per-unit filter capacitance. The per-unit parameters can be derived as follows:

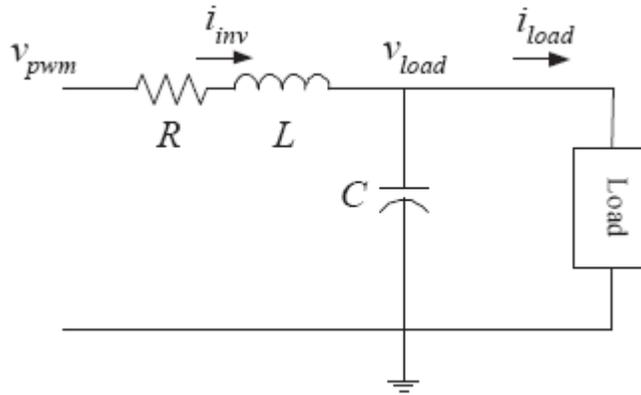


Figure 2.4: The per-unit one dimensional equivalent model of the inverter system.

$$R = \frac{R_f}{Z_b},$$

$$L = \frac{\omega_1 L_f}{Z_b} \cdot \frac{1}{\omega_1} = \frac{L_f}{Z_b},$$

and

$$C = \frac{1}{\omega_1} \cdot \frac{1}{\frac{1}{\omega_1 C_f} \frac{1}{Z_b}} = C_f Z_b,$$

where $\omega_1 = 2\pi f_1 = 2\pi \times 60 = 120\pi$ (rad/s) is the fundamental angular frequency.

The per-unit one dimensional equivalent model is depicted in Figure 2.4 and the system equations become

$$\dot{v}_{load} = \frac{1}{C} i_{inv} - \frac{1}{C} i_{load}, \quad (2.8)$$

and

$$\dot{i}_{inv} = \frac{1}{L} v_{pwm} - \frac{R}{L} i_{inv} - \frac{1}{L} v_{load}. \quad (2.9)$$

The above equations can be rewritten in state space format as follows:

$$\dot{X} = AX + Bu + Ed, \quad (2.10)$$

where the state variable $X = [v_{load} \ i_{inv}]^T$, the control input $u = v_{pwm}$, the disturbance input $d = i_{load}$, and the coefficients

$$A = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{R}{L} \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix},$$

and

$$E = \begin{bmatrix} -\frac{1}{C} \\ 0 \end{bmatrix}.$$

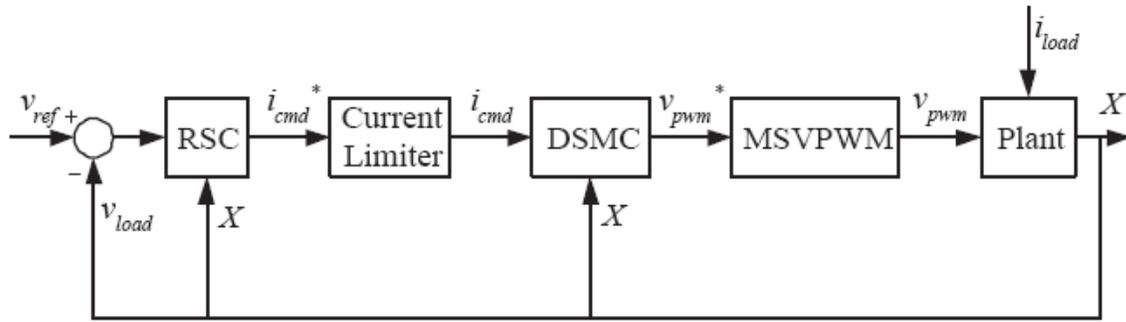


Figure 2.5: The proposed control system block diagram.

2.2 Control System Development

Given the above per-unit plant model, a dual loop control structure is proposed in this research. The inner loop is for inverter current control. A discrete-time sliding mode controller is applied. The outer loop is for the load voltage control. A discrete-time robust servomechanism controller is used as the voltage controller. The entire closed-loop system can be illustrated by Figure 2.5.

In Figure 2.5, RSC is the robust servomechanism controller, DSMC is the discrete-time sliding mode controller, MSVPWM is a modified space vector pulse width modulation inverter, v_{ref} is the reference load voltage, i^*_{cmd} is the desired inverter current command, i_{cmd} is the true inverter current command, v^*_{pwm} is the PWM voltage command, and v_{pwm} is the true modulated inverter output voltage. A current limiter is added between the two loops for over-current protection. The detailed development of each module will be described in the following subsections.

2.2.1 Design of the discrete-time sliding mode current controller

Discrete-time sliding mode control (DSMC) is the implementation of the sliding mode control theory in discrete-time. Unlike its continuous-time counterpart, which is known for having an discontinuous control law caused by the sign function, the discrete-time sliding mode is achieved with a continuous control law. Direct implant of continuous-time sliding mode control law into discrete-time causes chattering problem due to the sampling effects. However, the discrete-time sliding mode control law does not have the problem and achieves one-step tracking for any reference input with a bandwidth lower than half of the sampling frequency given unlimited control force. If the control force is limited, the sliding mode manifold can be reached in finite number of steps [108]. Since the control law of the discrete-time sliding mode control is continuous from discrete-time point of view, it can be implemented in practice with pulse width modulation with a fixed switching frequency. Continuous-time sliding mode control on an inverter typically results in varying switching frequency which

may introduce more harmonics. With known plant parameters and enough control force, the discrete-time control law is equivalent to deadbeat control in formula. The most attractive property of the discrete sliding mode control is its overshoot free fast response.

For the control plant given in Equation 2.10, the discrete-time sliding mode control law can be derived as follows.

Given a sampling period of T_s and assuming zero order hold, the plant for inverter current control can be discretized as

$$\begin{cases} X(k+1) = A_d X(k) + B_d u(k) + E_d d(k), \\ y(k) = C_i X(k) \end{cases} \quad (2.11)$$

where

$$A_d = e^{AT_s}, B_d = \int_0^{T_s} e^{A(T_s-\tau)} B d\tau, E_d = \int_0^{T_s} e^{A(T_s-\tau)} E d\tau, \text{ and } C_i = [0 \ 1]$$

To let the current output of next step $y(k+1)$ track the reference input $i_{cmd}(k)$, a discrete-time sliding mode manifold can be chosen in the form of

$$s(k) = C_i X(k) - i_{cmd}(k),$$

i.e., the tracking error, such that when the discrete-time sliding mode exists, the

output $y(k)$ tends to the reference $i_{cmd}(k)$. Discrete-time sliding mode can be reached if the control input $u(k)$ is designed to be the solution of

$$s(k+1) = C_i A_d X(k) + C B_d u(k) + C E_d d(k) - i_{cmd}(k) = 0, \quad (2.12)$$

The control law satisfies Equation 2.12 is called *equivalent control* [108] and is given by

$$u_{eq}(k) = (C_i B_d)^{-1} [i_{cmd}(k) - C_i A_d X(k) - C_i E_d d(k)], \quad (2.13)$$

and $v^*_{pwm}(k) = u(k)$.

The actual control voltage applied to the $L_j C$ filter stage is the inverter output PWM voltage $v_{pwm}(k)$, which is limited by the available top and bottom half dc bus voltages. The control force limitation caused by the dc bus voltage will be discussed in Sections 2.2.4 and 2.3.4.

In practical implementation of the proposed discrete-time control strategy using a microprocessor, there exists a half sampling cycle time delay as illustrated in Figure 2.6. Figure 2.6 shows that the discrete-time control operation of a digital signal

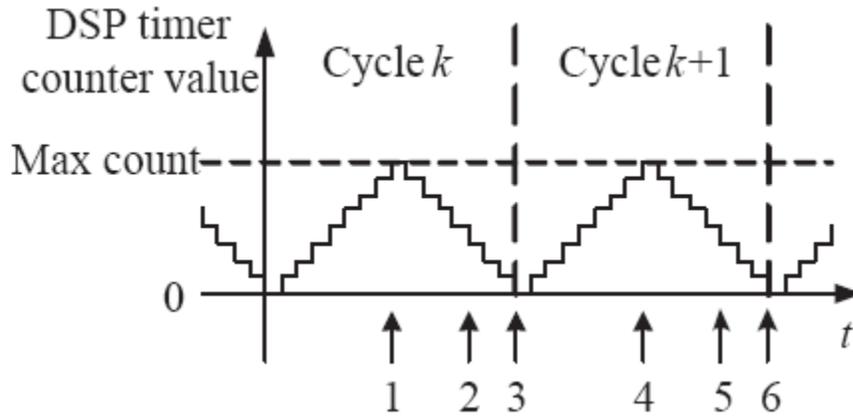


Figure 2.6: DSP operation causes half sampling cycle time delay: 1 - ADC of Cycle k , 2 - calculation done of Cycle k , 3 - PWM updated of Cycle k , 4 - ADC of Cycle $k + 1$, 5 - calculation done of Cycle $k + 1$, 6 - PWM updated of Cycle $k + 1$.

processor (DSP) is synchronized by the system timer counting in a continuous up and down mode. When the timer count reaches its maximum, e.g., time instants 1 and 4 in Figure 2.6, which is preset determining the sampling period, the analog to digital conversion (ADC) of the measured signals is triggered and the control algorithm of this cycle is launched. Based on the complexity of the control algorithm and the DSP clock frequency, the control algorithm is supposed to complete sometime before the timer counts back to zero, e.g., time instants 2 and 5 in Figure 2.6. The time duration between points 1 and 2 or 4 and 5 is the time consumed by the control calculation. However, the updated three-phase PWM values resulting from the control calculation do not take effect until the timer counts to zero, e.g., time instants 3 and 6 in Figure 2.6. Therefore, there is a half cycle time delay between the time instant when the feedback variables are measured and the one when the updated PWM control command takes effect.

In order to compensate for the time delay and improve the control performance, a first-order half step predictor is introduced as follows:

$$x(kT_s + \frac{1}{2}T_s) = x(k) + \frac{x(k) - x(k-1)}{T_s} \cdot \frac{T_s}{2} = 1.5x(k) - 0.5x(k-1), \quad (2.14)$$

where x can be replaced by any discrete-time variable in the system. Therefore, the control law can be rewritten in

$$u_{eq}(k) = (C_i B_d)^{-1} \{ i_{cmd}(k) - C_i A_d [1.5X(k) - 0.5X(k-1)] - C_i E_d [1.5d(k) - 0.5d(k-1)] \}, \quad (2.15)$$

If a new vector X_{DSMC} is defined as

$$X_{DSMC} = [i_{cmd}(k) \ v_{load}(k) \ v_{load}(k-1) \ i_{inv}(k) \ i_{inv}(k-1) \ i_{load}(k) \ i_{load}(k-1)]^T$$

the DSMC control gain can be represented by

$$k_{DSMC} = (C_i B_d)^{-1} [1 \ 1.5A_{d,21} \ -0.5A_{d,21} \ 1.5A_{d,22} \ -0.5A_{d,22} \ 1.5E_{d,21} \ -0.5E_{d,21}], \quad (2.16)$$

where $A_{d:21}$ denotes the 2nd row and 1st column element in matrix A_d , and the control law becomes

$$u_{eq}(k) = k_{DSMC} X_{DSMC}. \quad (2.17)$$

2.2.2 Design of the robust servomechanism voltage controller

The goal of designing a realistic multivariable controller to solve the robust servomechanism problem [24] is to achieve closed-loop stability and asymptotic regulation, as well as other desirable properties - fast response, robustness, etc. The solution, so called the robustness servomechanism controller, combines both the internal model principle and the optimal control. The internal model principle says that a regulator synthesis is structurally stable only if the controller utilizes feedback of the regulated variable, and incorporates in the feedback path a suitably reduplicated model of the dynamic structure of the exogenous signals which the regulator is required to process [33]. Using the internal modeling principle to a linear time-invariant (LTI) plant, asymptotic tracking of controlled variables toward the corresponding references in the presence of disturbances (zero steady state tracking error) can be achieved if the models that generate these references and disturbances are included in the stable closed loop systems. A simple form of optimal control technique - linear quadratic controller is used to obtain the feedback gain satisfying a certainly defined optimization criterion. By minimizing this criterion, the eigenvalues of the state space model will be automatically placed and the feedback gains will be uniquely selected. The

optimization criterion chosen is a functional of quadratic forms in the space of the state vector and the input of the system [6].

A discrete-time robust servomechanism controller (RSC) is used for outer loop regulation. In this control system, the reference input is the desired DG unit output voltage which is a 60 Hz sinusoidal signal, the disturbance is the load current, which may contain harmonic frequency components besides the fundamental. In practice, all high frequency harmonics have already been suppressed by the L/C filter and the major components that may affect the system control performance are low harmonics, typically 3rd, 5th, and 7th order harmonics, etc. The higher the order of the harmonic, the less effect it can cause to the performance. Therefore, the dynamics of the tracking or rejecting signals are known, which are governed by poles at $\pm j\omega_1$, $\pm j\omega_3$, $\pm j\omega_5$, and $\pm j\omega_7$, etc., where $\omega_1 = 2\pi \times 60$ rad/s, $\omega_3 = 3\omega_1$, $\omega_5 = 5\omega_1$, and $\omega_7 = 7\omega_1$, etc.

The RSC is a model based controller. Given a plant, reference signals, and disturbances, the existence of the control solution is conditional. The solution of RSC exists if the following four conditions are satisfied [24]:

1. The control plant is stabilizable and detectable.
2. The dimension of control is greater or equal to that of the outputs.
3. The transmission zeros of the plant exclude the poles of the reference input and disturbance signals.
4. The outputs of the system is measurable.

If the above conditions are satisfied, the RSC can be designed analytically.

Since the DSMC serves as the controller for in the inner loop, its dynamics has to be included together with the original plant to form the control plant for the RSC. Given the plant as shown in Equation 2.10 and a sampling period of T_s , assuming zero order hold and half sampling period input delay, the discretized plant is

$$\begin{cases} X(k+1) = A_d X(k) + B_{d0} u(k) + B_{d1} u(k-1) + E_d d(k), \\ y(k) = C_v X(k) \end{cases} \quad (2.18)$$

where

$$A_d = e^{AT_s}, B_{d0} = \int_{\frac{T_s}{2}}^{T_s} e^{A(T_s-\tau)} B d\tau, B_{d1} = \int_0^{\frac{T_s}{2}} e^{A(T_s-\tau)} B d\tau, E_d = \int_0^{T_s} e^{A(T_s-\tau)} E d\tau,$$

and $C_v = \begin{bmatrix} 1 & 0 \end{bmatrix}$. Due to the existence of $u(k-1)$, it is reasonable to convert the plant model in Equation 2.18 into standard state space format as

$$\begin{cases} X_p(k+1) = A_p X_p(k) + B_p u(k) + E_p d(k), \\ y(k) = C_p X_p(k) \end{cases} \quad (2.19)$$

where $X_p(k) = \begin{bmatrix} X(k)^T & u(k-1) \end{bmatrix}^T = \begin{bmatrix} v_{load}(k) & i_{inv}(k) & u(k-1) \end{bmatrix}^T,$

$$A_p = \begin{bmatrix} A_d & B_{d1} \\ 0_{1 \times 2} & 0 \end{bmatrix},$$

$$B_p = \begin{bmatrix} B_{d0} \\ 1 \end{bmatrix},$$

$$E_p = \begin{bmatrix} E_d \\ 0 \end{bmatrix},$$

and $C_p = [C_v 0]$.

After the dynamics of the DSMC shown in Equation 2.13 is included, the overall plant for the RSC is:

$$\begin{cases} X_p(k+1) = A_p^* X_p(k) + B_p^* u(k) + E_p d(k), \\ y(k) = C_p X_p(k) \end{cases} \quad (2.20)$$

where

$$A_p^* = A_p - B_p (C_i B_d)^{-1} C_i A_d C_1,$$

and

$$B_p^* = B_p (C_i B_d)^{-1},$$

where

$$C_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}.$$

The plant for RSC described by Equation 2.20 can be observed and proved controllable and observable using the controllability and observability criteria in linear systems theory with practically chosen circuit parameters R , L , and C . Since the tracking and rejecting dynamics have poles only at $\pm j\omega_1$, $\pm j\omega_3$, $\pm j\omega_5$, and $\pm j\omega_7$, etc., the transmission zeros of the plant can easily avoid coinciding them. In practice,

this is not a concern. The input control signal to the plant, i.e., the output of the RSC, is the inverter current command. The output of the plant, for the load voltage control purpose, is the load voltage itself. Therefore, the input and output have the same dimension. In practical systems, the load voltages, inverter currents, and the load currents are all measured. Hence, it can be declared that all of the four existence conditions of the RSC are satisfied.

The RSC design includes two parts - a servo compensator and a stabilizing compensator.

The servo compensator can be designed as follows. If the tracking/disturbance poles to be considered are $\pm j\omega_1$, $\pm j\omega_3$, $\pm j\omega_5$, and $\pm j\omega_7$, the servo-compensator is

$$\dot{\eta} = A_s \eta + B_s e, \quad (2.21)$$

where

$$\eta = \begin{bmatrix} \eta_1 \\ \eta_3 \\ \eta_5 \\ \eta_7 \end{bmatrix},$$

$$A_s = \begin{bmatrix} A_{s1} & & & \\ & A_{s3} & & \\ & & A_{s5} & \\ & & & A_{s7} \end{bmatrix},$$

and

$$B_s = \begin{bmatrix} B_{s1} \\ B_{s3} \\ B_{s5} \\ B_{s7} \end{bmatrix},$$

and voltage regulation error $e = v_{ref} - v_{load}$, where

$$\eta_i = \begin{bmatrix} \eta_{i1} \\ \eta_{i2} \end{bmatrix}$$

$$A_{si} = \begin{bmatrix} 0 & 1 \\ -\omega_i^2 & 0 \end{bmatrix},$$

(2.22)

and

$$B_{si} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

for $i=1, 3, 5, 7$.

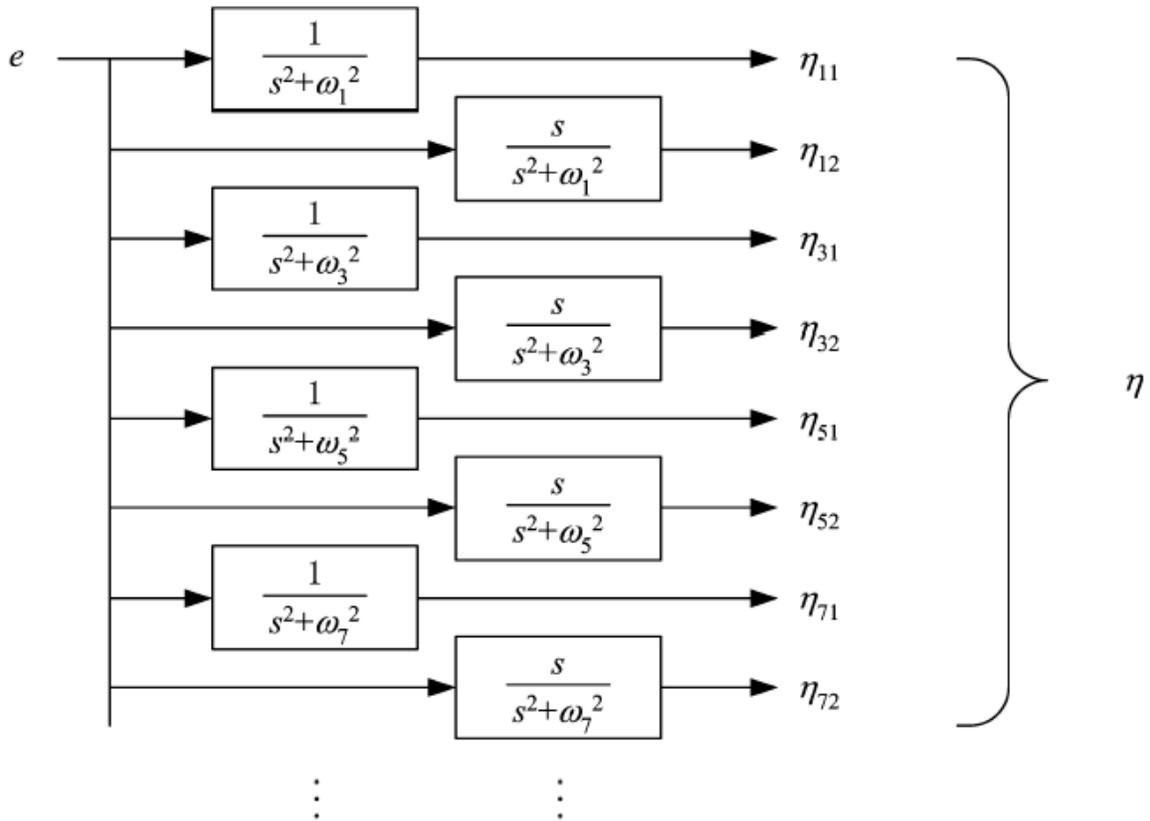


Figure 2.7: Block diagram of the servo compensator.

The transfer function representation of the servo compensator is illustrated in Figure 2.7, which shows that the servo compensator consists of a series of resonant filters with their resonant frequencies equal to the specified tracking or rejecting frequencies. The frequency domain characteristics of the four included resonant filter are shown in Figures 2.8 to 2.11. The resonance characteristic only allows the signals with specified frequencies to pass, i.e., since the input to the servo compensator is the voltage regulation error, the voltage regulation tends to be sensitive to only those regulation error signals with specified frequencies. This idea is the same as the *resonant regulator* concept reviewed in Section 1.2.1.

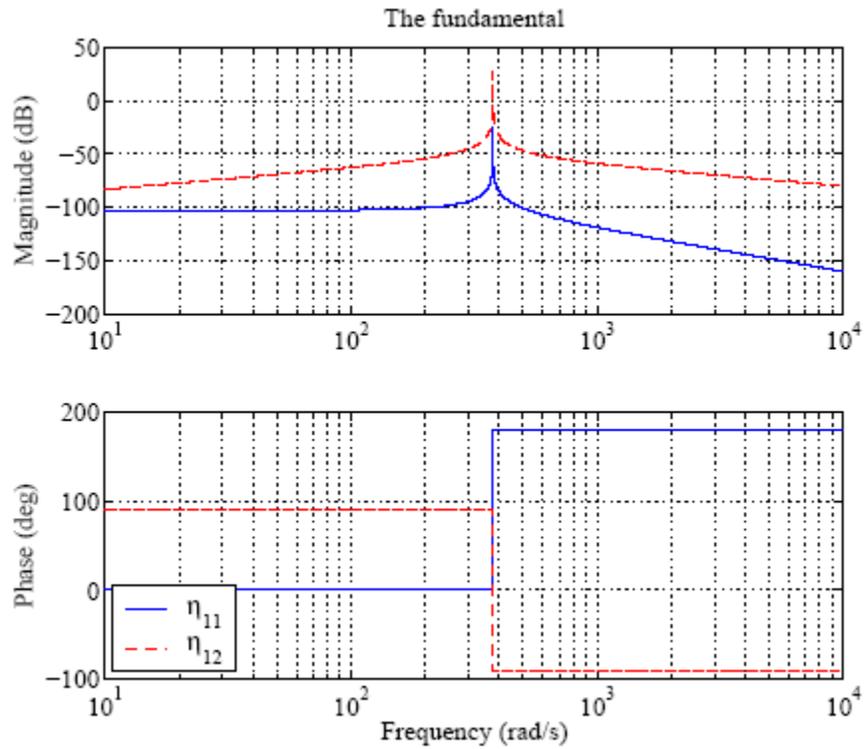


Figure 2.8: Bode plot of servo compensator for the fundamental component.

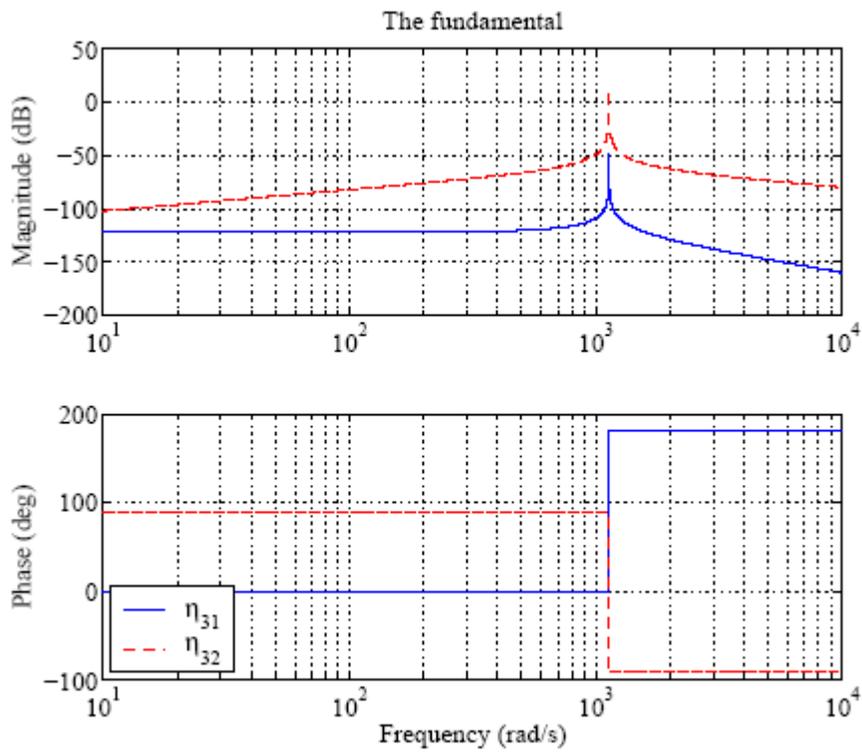


Figure 2.9: Bode plot of servo compensator for the 3rd harmonic.

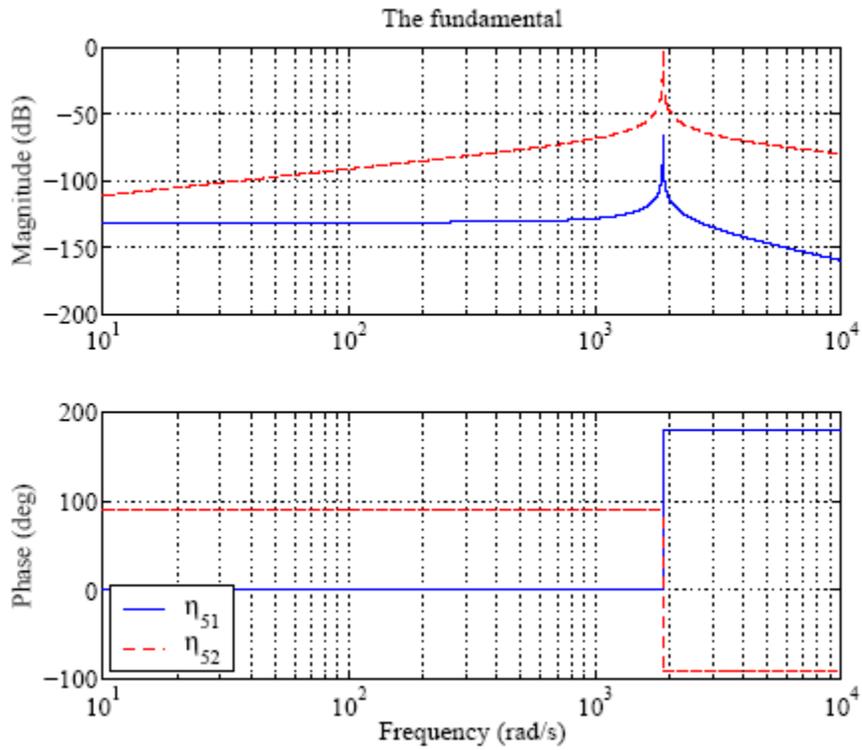


Figure 2.10: Bode plot of servo compensator for the 5th harmonic.

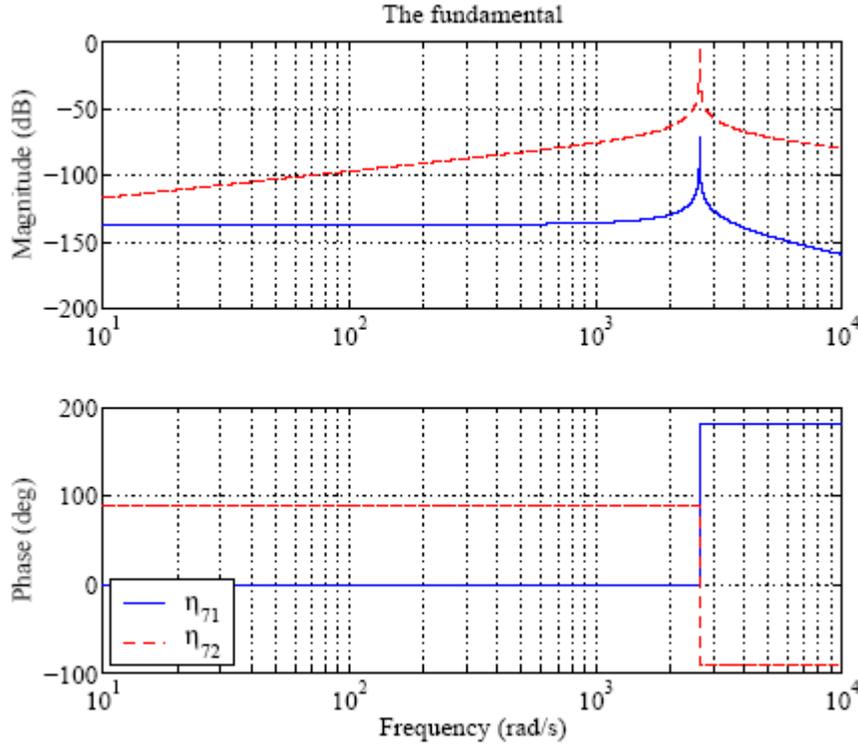


Figure 2.11: Bode plot of servo compensator for the 7th harmonic.

Equation 2.22 is the most straight forward state space implementation of a resonant filter with a specified frequency. However, in practice, the values of the elements in matrix A_{si} may significantly differ from each other, which may cause poor condition number of the matrix and numerical instability in microprocessor implementation, especially fixed point microprocessors. To overcome this problem, an orthogonal transformation can be applied to the matrices A_{si} and B_{si} to balance up the elements in A_{si} while keep the transfer function unchanged. This transformation can be described as $A_{si,bal} = T^{-1}A_{si}T$ and $B_{si,bal} = T^{-1}B_{si}$, where the orthogonal matrix T can be obtained using Matlab function `ssbal()`.

The servo compensator needs to be discretized in practice. Given the same sam-

pling period T_s as above, the discrete-time servo compensator is

$$\eta(k+1) = A_{sd}\eta(k) + B_{sd}e(k), \quad (2.23)$$

where $A_{sd} = e^{A_s T_s}$ and $B_{sd} = \int_0^{T_s} e^{A_s(T_s-\tau)} B_s d\tau$.

In existence of the servo compensator, the stabilizing compensator can be generated.

An augmented system combining both the plant (Equation 2.20) and the servo-compensator (Equation 2.23) can be written as:

$$\hat{X}(k+1) = \hat{A}\hat{X}(k) + \hat{B}u_1(k) + \hat{E}_1 d(k) + \hat{E}_2 y_{ref}(k), \quad (2.24)$$

where the control input is $u_1(k) = i_{cmd}(k)$, the load disturbance is $d(k) = i_{load}(k)$,

the reference input is $y_{ref}(k) = v_{ref}(k)$, the state vector is $\hat{X} = [X_p^T \quad \eta^T]^T$, and

the coefficient matrices are

$$\hat{A} = \begin{bmatrix} A_p^* & 0 \\ -B_{sd}C_p & A_{sd} \end{bmatrix},$$

$$\hat{B} = \begin{bmatrix} B_p^* \\ 0 \end{bmatrix},$$

$$\hat{E}_1 = \begin{bmatrix} E_p \\ 0 \end{bmatrix},$$

and

$$\hat{E}_2 = \begin{bmatrix} 0 \\ B_{sd} \end{bmatrix}$$

The task of the stabilizing compensator is to stabilize the augmented system in Equation 2.24. To achieve this goal, the discrete-time LQ optimal control technique can be used, which guarantees stability of the system while yields optimized performance by minimizing a discrete-time linear quadratic performance index

$$J_\epsilon = \sum_{k=0}^{\infty} \hat{X}(k)^T Q \hat{X}(k) + \epsilon u_1(k)^T u_1(k), \quad (2.25)$$

where Q is a symmetrical positive-definite matrix to be chosen and $\epsilon > 0$ is a small number to reduce the weight of the control force in the optimization.

Obtaining the state feedback gain K minimizing J_ϵ requires solving the algebraic Riccati equation

$$\hat{A}^T P + P \hat{A} + Q - \frac{1}{\epsilon} P \hat{B} \hat{B}^T P = 0 \quad (2.26)$$

for the unique positive semidefinite solution P , so that

$$K = -\frac{1}{\epsilon} \hat{B}^T P. \quad (2.27)$$

Then the control input can be obtained as

$$u_1(k) = K^T \hat{X} = [K_0 \quad K_1] \begin{bmatrix} X_p \\ \eta \end{bmatrix}. \quad (2.28)$$

The block diagram of the RSC is shown in Figure 2.12.

In practice, the discrete-time algebraic Riccati equation can be solved using the Matlab function `dlqr()`. Since the system is linear time-invariant, the feedback

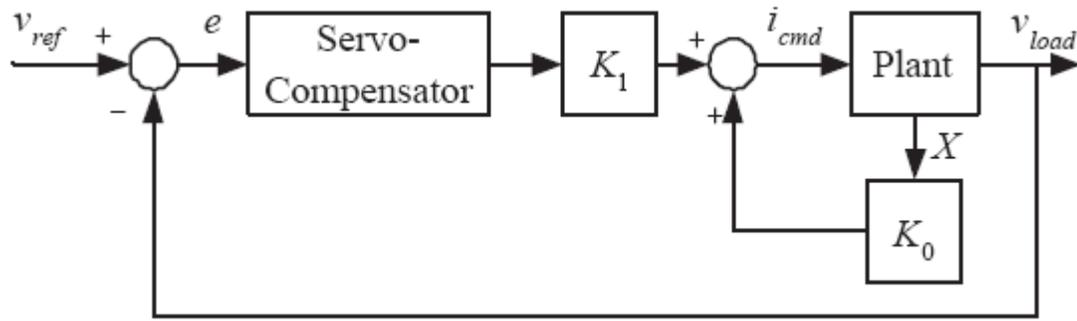


Figure 2.12: Block diagram of the RSC.

gain K is a constant value calculated in advance and does not change in operation.

Therefore, online updating of K is unnecessary.

In practice, the selection of Q has significant impacts on the control performance.

In the proposed technique, three different gains, w_p , w_1 , and w_h , are used as weights

for the plant states, i.e., X_p , fundamental servo compensator states, i.e., η_{11} and

η_{12} , and harmonic servo compensator states, i.e., η_{31} , η_{32} , η_{51} , η_{52} , η_{71} , and η_{72} ,

respectively. Therefore the weight matrix can be obtained as

$$Q = \begin{bmatrix} Q_1 & 0 \\ 0 & Q_2 \end{bmatrix}, \quad (2.29)$$

where $Q_1 = w_p I_3$, and

$$Q_2 = \begin{bmatrix} w_1 I_2 & 0 \\ 0 & w_h I_6 \end{bmatrix},$$

where I_n denotes an n dimensional identity matrix. To make good use of the servo compensator, w_p should be significantly less than w_1 and w_h . To emphasize good fundamental tracking, w_1 can be set significantly greater than w_h .

2.2.3 Limit the current command

The current command signal $i^*_{cmd}(k) = u_1(k)$ generated by the RSC needs to be limited to perform overload protection. In the discussed DG inverter system topology, current limit I_{max} is given as the maximum peak current allowed for a phase. However, the voltage and current controls are conducted in the stationary $\alpha\beta 0$ reference frame.

To solve this problem, a new current limiting algorithm has been developed as follows:

$$i_{cmd,i} = \begin{cases} i^*_{cmd,i}, & \text{for } \sqrt{i_{cmd,\alpha}^{*2} + i_{cmd,\beta}^{*2}} + |i^*_{cmd,0}| \leq I_{max}, \\ \frac{I_{max}}{\sqrt{i_{cmd,\alpha}^{*2} + i_{cmd,\beta}^{*2}} + |i^*_{cmd,0}|} i^*_{cmd,i}, & \text{for } \sqrt{i_{cmd,\alpha}^{*2} + i_{cmd,\beta}^{*2}} + |i^*_{cmd,0}| > I_{max}, \end{cases} \quad (2.30)$$

where the subscript $i \in \{\alpha, \beta, 0\}$, $i_{cmd,\alpha}^*$, $i_{cmd,\beta}^*$, and $i_{cmd,0}^*$ are the current commands generated by the RSCs for each axis.

To prevent servo-compensator states, which are related to the current command, from growing while the current command is saturated, the following strategy can be applied. Rewrite the servo-compensator equation as

$$\eta(k+1) = A_{sd}\eta(k) + B_{sd}e_1(k), \quad (2.31)$$

where

$$e_1(k) = \begin{cases} e(k), & \text{for } \sqrt{i_{cmd,\alpha}^{*2} + i_{cmd,\beta}^{*2}} + |i_{cmd,0}^*| \leq I_{max}, \\ 0, & \text{for } \sqrt{i_{cmd,\alpha}^{*2} + i_{cmd,\beta}^{*2}} + |i_{cmd,0}^*| > I_{max}. \end{cases}$$

When the current command is limited, the voltage control loop is open and the system is running under current controlled mode.

2.2.4 A modified space vector PWM

The conventional space vector PWM technique

Pulse width modulation (PWM) is a process that varies the time duration of a sequence of pulses according to a reference signal to get a reference-signal-modulated pulse sequence. In power electronics, PWM techniques are typical tools to control high-power voltage or current waveforms using low-power signals. The so called space

vector PWM (SVPWM) is a known and widely used three-phase pulse width modulation technique, which is originally developed for three-phase three-wire topologies where the inverter does not provide a neutral point. The basic operating principle of the conventional SVPWM for three-phase voltage source inverters is briefly reviewed as follows.

The SVPWM is a specially designed switching sequence for the power switches in a three-phase inverter using base space vectors to generate three-phase 120° apart sinusoidal line-to-line output voltages. This technique treats the sinusoidal reference voltage as a constant amplitude vector rotating at a certain frequency. There are eight base space vectors in total, corresponding to eight possible switching patterns of the inverter. The switching patterns of the inverter and associated base space vectors are shown in Figure 2.13. Each of the three elements reflects the on/off state of one of the three legs in the inverter. If the inverter has a Y connected load as shown in Figure 2.14, the output line-to-neutral and line-to-line voltages are shown in Table 2.1 assuming normalized dc bus voltage.

Among the eight base vectors, Vectors 1 to 6 generate non-zero output voltages and the three-phase voltage waveforms generated by repeated sequences of Vector 1 to 6 are illustrated in Figure 2.15, where the line-to-neutral voltages are known as the six-step waveform. Vectors 7 and 8 generate zero output voltage in the topology of Figure 2.14 by connecting all three outputs to the upper or bottom rail of the dc bus.

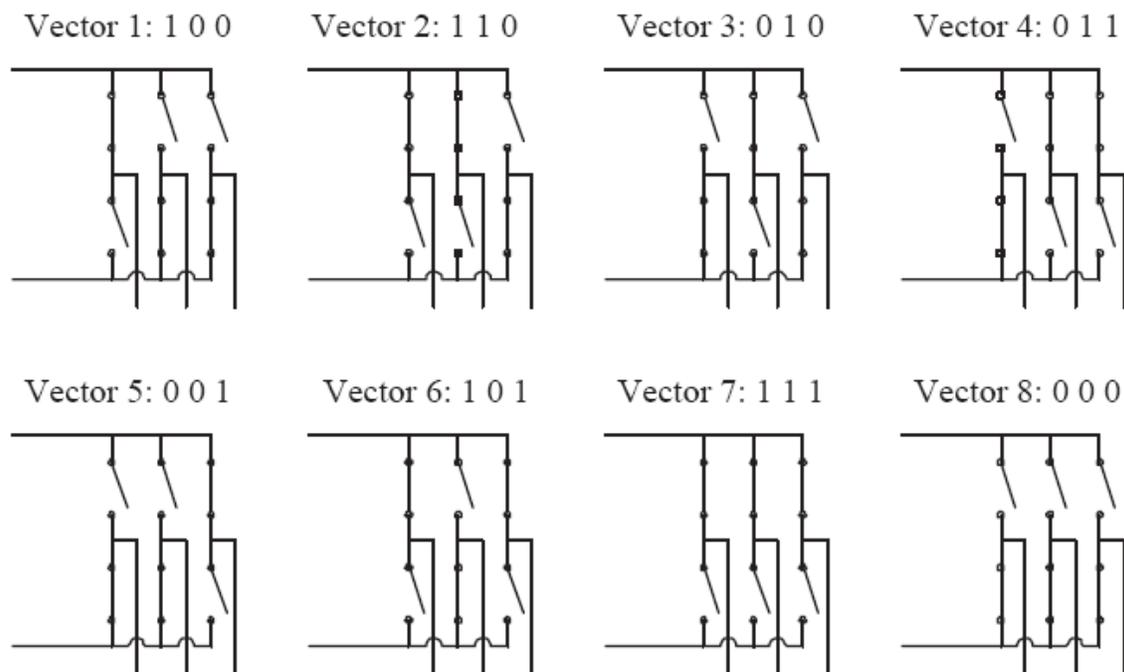


Figure 2.13: Switching patterns of space vector PWM.

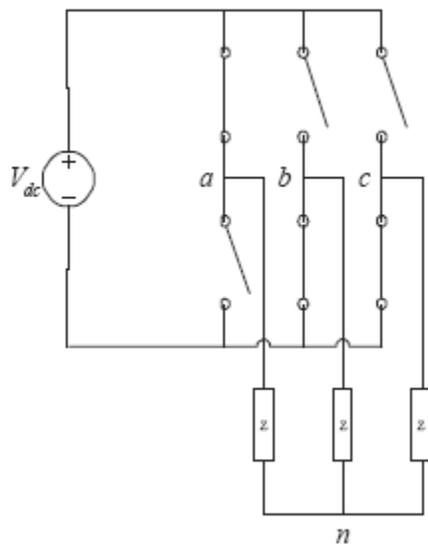


Figure 2.14: Three-phase three-wire inverter topology with Y connected load.

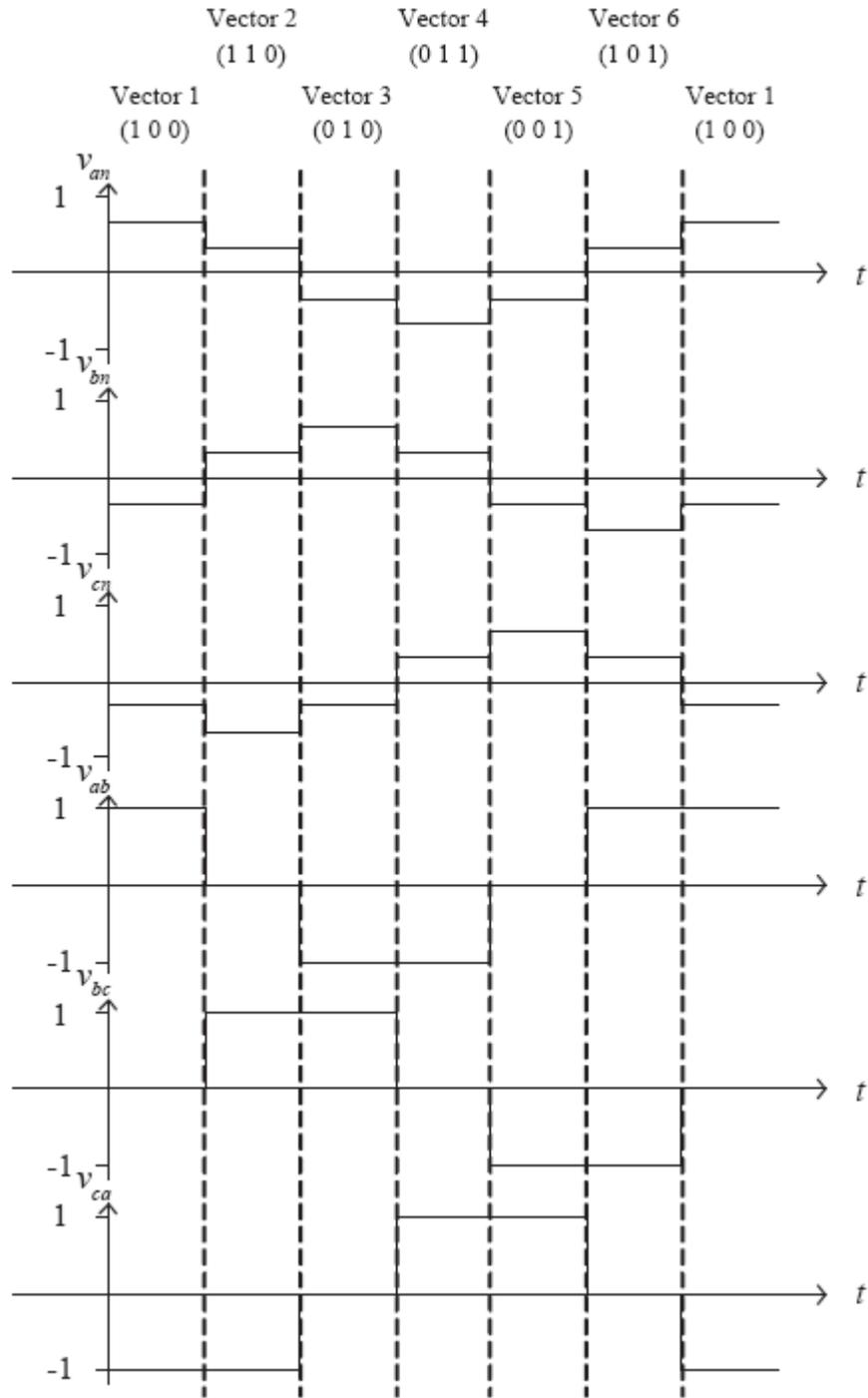


Figure 2.15: Output voltage waveforms of space vector PWM base vectors.

	a	b	c	v_{an}	v_{bn}	v_{cn}	v_{ab}	v_{bc}	v_{ca}
Vector 1	1	0	0	$\frac{2}{3}$	$-\frac{1}{3}$	$-\frac{1}{3}$	1	0	-1
Vector 2	1	1	0	$\frac{1}{3}$	$\frac{1}{3}$	$-\frac{2}{3}$	0	1	-1
Vector 3	0	1	0	$-\frac{1}{3}$	$\frac{2}{3}$	$-\frac{1}{3}$	-1	1	0
Vector 4	0	1	1	$-\frac{2}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	-1	0	1
Vector 5	0	0	1	$-\frac{1}{3}$	$-\frac{1}{3}$	$\frac{2}{3}$	0	-1	1
Vector 6	1	0	1	$\frac{1}{3}$	$-\frac{2}{3}$	$\frac{1}{3}$	1	-1	0
Vector 7	1	1	1	0	0	0	0	0	0
Vector 8	0	0	0	0	0	0	0	0	0

Table 2.1: Output voltage patterns of base vectors under normalized dc bus voltage.

The fundamental components of the waveforms shown in Figure 2.15 are three-phase 120° apart sine waves. However, there are significant amount of harmonics due to the step waveforms caused by the base vectors which do not provide intermediate values in between the steps. Weighting of these discrete base vector values in time duration allows intermediate values to be obtained. Weighting the duration of the base vectors according to a reference vector is the main idea of SVPWM. The base vectors can be depicted geometrically as shown in Figure 2.16, where the consecutive non-zero vectors on a plane form six 60° sectors representing a full sinusoidal period matching the result in Figure 2.15. A sinusoidal reference signal can be represented by a vector on the same plane rotating from one sector to another with a constant speed. In each sector, the reference vector can be achieved by time-averaging the two boundary base vectors and two zero vectors with proper weights, as illustrated in Figure 2.17 showing the case of Sector I.

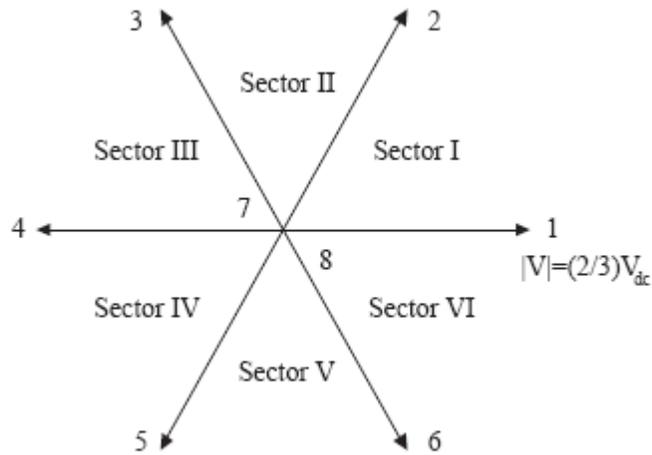


Figure 2.16: Base vectors of space vector PWM in two dimensional space.

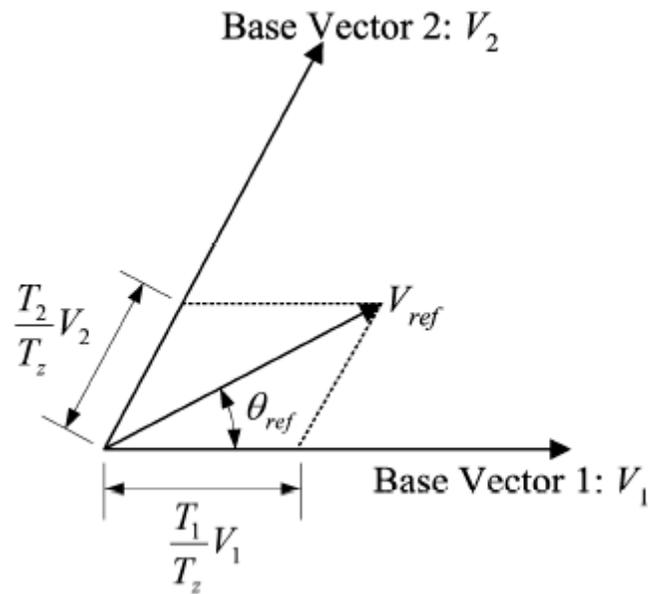


Figure 2.17: Modulation of a reference voltage using space vector PWM in two dimensional space.

Similar to the well known sine wave PWM, SVPWM is also a carrier based fixed switching frequency modulation technique, where each power switch is turned on and

off fixed number of times in a period of time. In any one PWM period, a switch is turned on and off once. The PWM switching frequency should be significantly greater than the reference frequency to generate enough number of pulses and reduce harmonics. In Figure 2.17, T_z is half of the PWM period, T_1 is the duration of Vector 1 and T_2 is the duration of Vector 2 in a half PWM period. The remaining time $T_z - T_1 - T_2$ is the duration for the zero vectors. The values of T_1 and T_2 are calculated based on the values of V_{ref} and μ_{ref} .

The advantages of conventional SVPWM for a three-phase three-wire system include less harmonic distortion in output voltages and/or currents applied to the phases and more efficient use of the supply voltage in comparison with direct sinusoidal modulation technique, i.e., higher dc bus utilization.

A modified space vector PWM technique

In three-phase three-wire systems, the three phases are not independent, i.e., there exist only two independent degrees of freedom. The conventional SVPWM only provides two dimensional control and that is why the base vectors are on the same plane. However, in a three-phase four-wire system with split dc bus topology discussed in this report, the neutral of the load is grounded, which yields three independent phases and calls for three dimensional control. In this topology, Vectors 7 and 8 are no longer zero vectors in terms of line-to-neutral voltages. The output voltages of the split dc bus inverter are shown in Table 2.2 and the corresponding waveforms are shown in Figure 2.18.

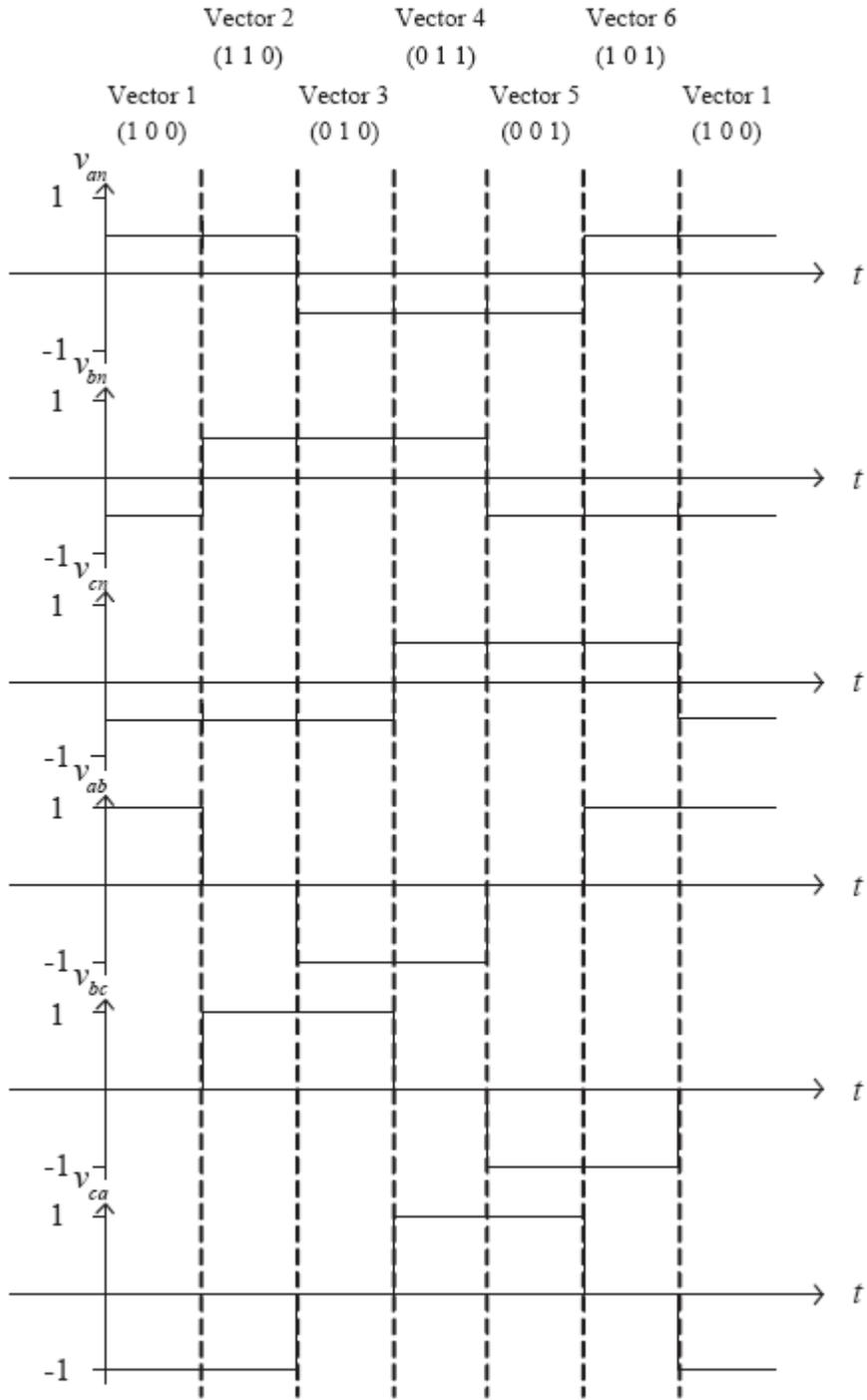


Figure 2.18: Output voltage waveforms of the base vectors in a four-wire split dc bus topology.

	a	b	c	v_{an}	v_{bn}	v_{cn}	v_{ab}	v_{bc}	v_{ca}
Vector 1	1	0	0	$\frac{1}{2}$	$-\frac{1}{2}$	$-\frac{1}{2}$	1	0	-1
Vector 2	1	1	0	$\frac{1}{2}$	$\frac{1}{2}$	$-\frac{1}{2}$	0	1	-1
Vector 3	0	1	0	$-\frac{1}{2}$	$\frac{1}{2}$	$-\frac{1}{2}$	-1	1	0
Vector 4	0	1	1	$-\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	-1	0	1
Vector 5	0	0	1	$-\frac{1}{2}$	$-\frac{1}{2}$	$\frac{1}{2}$	0	-1	1
Vector 6	1	0	1	$\frac{1}{2}$	$-\frac{1}{2}$	$\frac{1}{2}$	1	-1	0
Vector 7	1	1	1	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	0	0	0
Vector 8	0	0	0	$-\frac{1}{2}$	$-\frac{1}{2}$	$-\frac{1}{2}$	0	0	0

Table 2.2: Output voltage patterns of base vectors in the four-wire split dc bus topology.

From Table 2.2, it can be observed that Vectors 7 and 8 provide non-zero line-to-neutral voltages which is the third dimension, the 0-axis quantity, not existing in the three-wire topology. The 0-axis voltages or currents in the three-phase circuit caused by Vector 7 or 8 are called common mode voltages or currents because they are in phase to each other.

A modified space vector PWM technique (MSVPWM) has been developed to take advantage of the Vectors 7 and 8 to achieve three dimensional control in an $\alpha\beta 0$ system.

In conventional SVPWM, the durations of Vectors 7 (000) and 8 (111) are equal in a half PWM period, as shown in Figure 2.19, and there is no 0-axis control capability. However, in MSVPWM, unequal duration of Vectors 7 and 8 causes uneven 0-axis

average voltage in a PWM period and allows 0-axis current to flow, which enables the inverter to perform control in all α , β , and 0 axes. A Sector I illustration is shown in Figure 2.20.

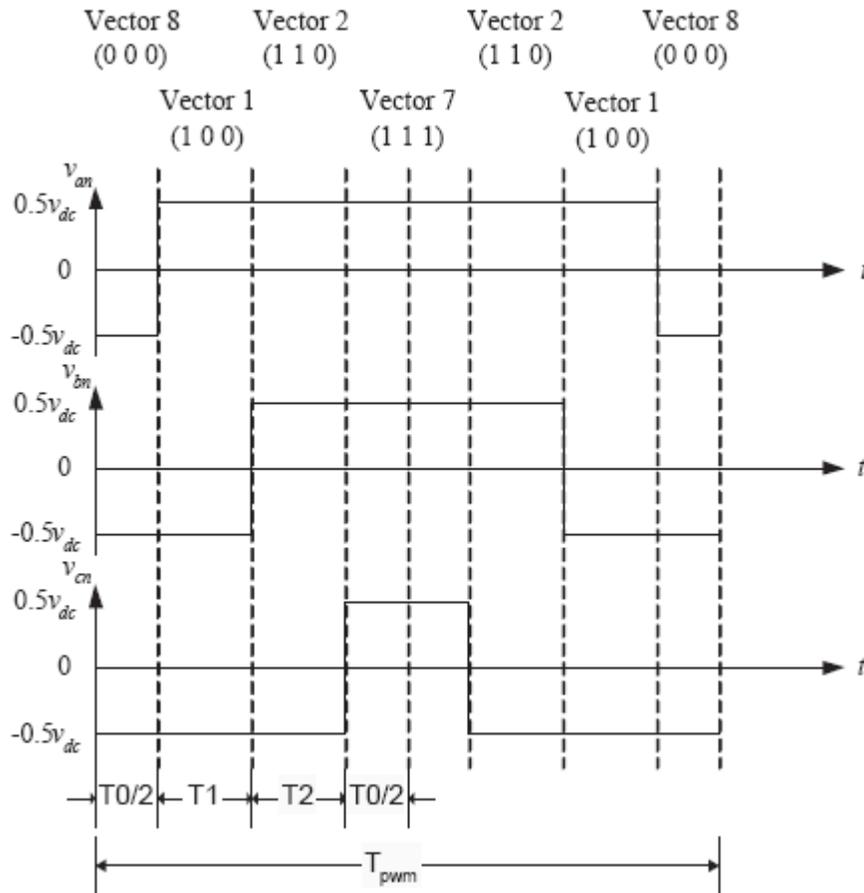


Figure 2.19: Sector I on-off sequence of conventional space vector PWM.

Calculation of the vector durations in MSVPWM is shown below, using Sector I as an example. Given three dimensional reference voltage inputs, v_α , v_β , v_0 , and the PWM period T_{pwm} , the α - β plane reference voltage is

$$V_{ref} = \sqrt{v_{\alpha}^2 + v_{\beta}^2}, \quad (2.32)$$

its phase angle is

$$\theta_{ref} = \arctan \frac{v_{\beta}}{v_{\alpha}}, \quad (2.33)$$

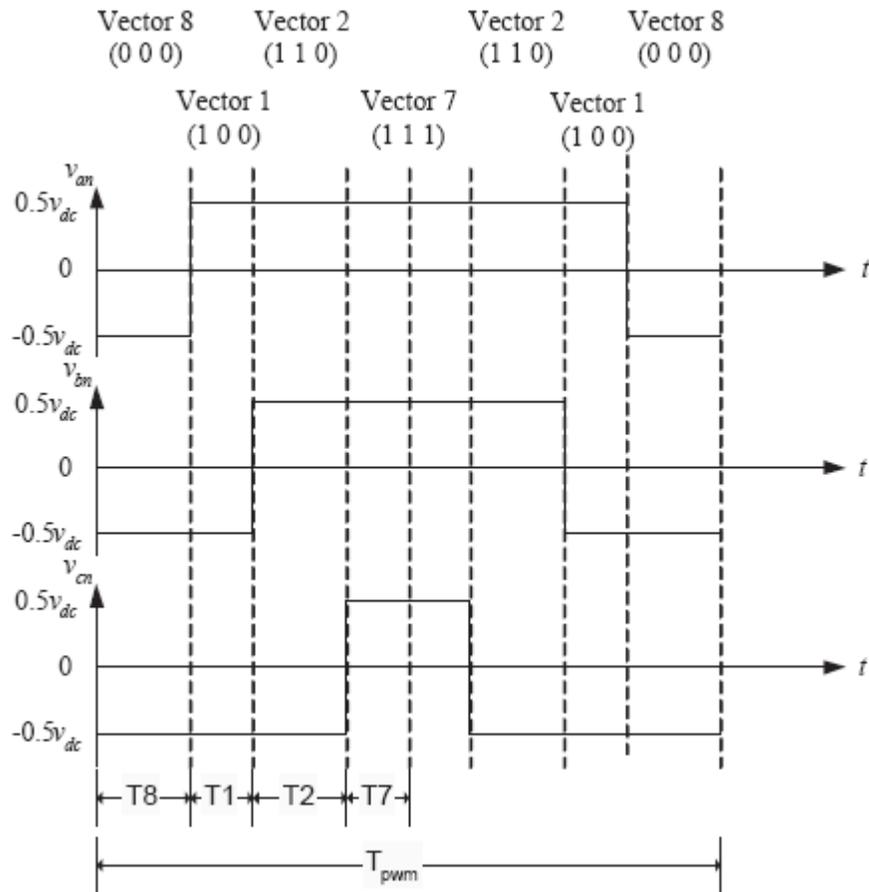


Figure 2.20: Sector I on- α sequence of modified space vector PWM.

and the modulation index is

$$a = \frac{V_{ref}}{\frac{1}{2}V_{dc}}. \quad (2.34)$$

As mentioned above, $T_z = (1/2)T_{pwm}$ is the half PWM period. The Vector 1 duration is

$$T_1 = \frac{\sin(\frac{\pi}{3} - \theta_{ref})}{\sin \frac{\pi}{3}} T_z a \quad (2.35)$$

and the Vector 2 duration is

$$T_2 = \frac{\sin \theta_{ref}}{\sin \frac{\pi}{3}} T_z a. \quad (2.36)$$

The sum of the Vector 7 and 8 durations is $T_0 = T_z - T_1 - T_2$. After defining

$$\Delta T = \frac{v_0}{\frac{1}{2}V_{dc}} T_z,$$

the durations of Vectors 7 and 8 are

$$T_7 = \begin{cases} \frac{1}{2}(T_0 + \Delta T) & \text{for } |\Delta T| \leq T_0, \\ T_0 & \text{for } |\Delta T| > T_0, \\ 0 & \text{for } |\Delta T| < -T_0, \end{cases} \quad (2.37)$$

and

$$T_8 = \begin{cases} \frac{1}{2}(T_0 - \Delta T) & \text{for } |\Delta T| \leq T_0, \\ 0 & \text{for } |\Delta T| > T_0, \\ T_0 & \text{for } |\Delta T| < -T_0. \end{cases} \quad (2.38)$$

The one PWM period time average voltage waveforms comparing the conventional SVPWM and the new MSVPWM have been shown in Figure 2.21, where the dashed curve is the line-to-neutral voltage generated by conventional SVPWM while the solid curve is that by MSVPWM with a 0-axis compensation injection shown by the dotted line. In a feedback control system, this compensation signal v_0 can be automatically generated by the controller in the feedback loop.

The benefit of this MSVPWM is that it provides three dimensional control for three-phase four-wire split dc bus topology inherently in the stationary $\alpha\beta 0$ reference

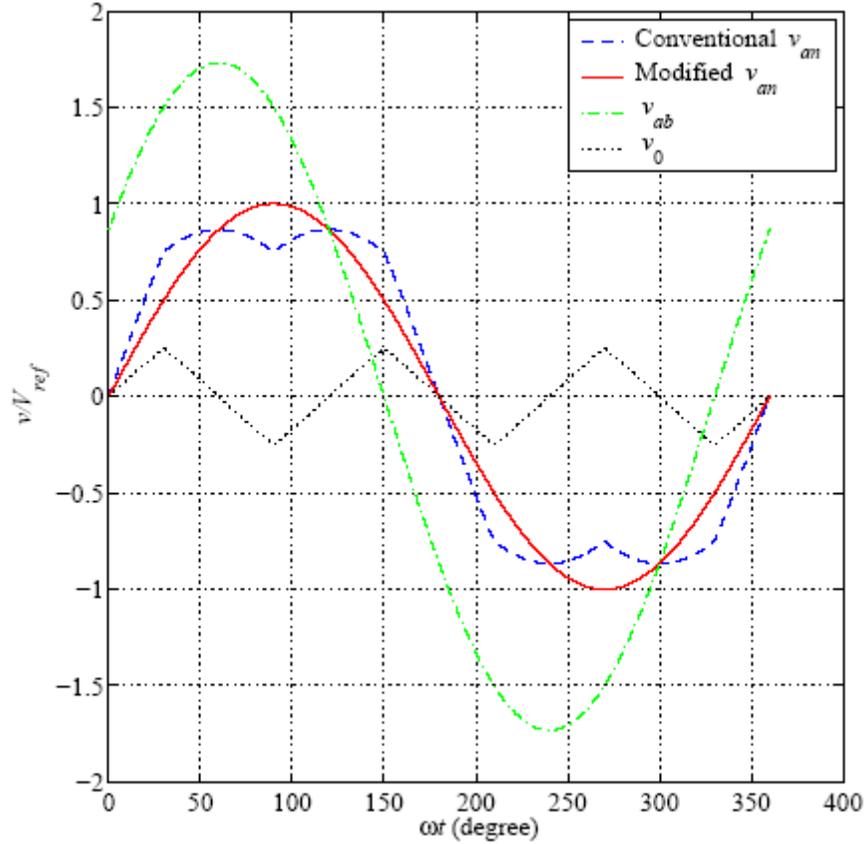


Figure 2.21: Output waveforms of the space vector PWM techniques.

frame, which performs better than direct ABC reference frame control when the dc bus voltage is limited. Further analysis results verifying this statement will be presented in Section 2.3.4. The trade-off of this technique is that it has less dc bus voltage utilization in that the maximum reference voltage in the conventional

SVPWM is $V_{ref,max} = \frac{\sqrt{3}}{3}V_{dc}$ and that in the MSVPWM is $V_{ref,max}=(1/2)V_{dc}$.

2.3 Performances and Analysis

In this section, both frequency domain analysis and time domain simulation and

experiments will be presented.

2.3.1 Frequency domain analysis

A 5-KVA DG unit with three-phase four-wire split dc bus topology as shown in Figure 2.1 is analyzed. The rectifier is assumed to supply dc voltages regulated at ± 270 V. The rated RMS line-to-neutral three-phase ac output voltage is 120 V. The discrete-time control frequency, as well as the PWM switching frequency, $f_s = 1/T_s$ is set to be 5.4 kHz.

A three-phase L - C filter is selected with $L_f = 10.2$ mH and $C_f = 55$ μ F. This filter has a natural frequency of 1335.1 rad/s and damping ratio of 0.0367, where a line/coil resistance of 1 Ω is assumed. The bode plot of this filter is shown in Figure 2.22. Greater values of L and C yield better filter performance but large L leads to high weight and volume and large C leads to high capacitor current at no load. Therefore the selection of L and C is usually a trade-off and the values can be selected to yield a natural frequency or cut-off frequency lower than 10th harmonic frequency, which filters out high frequency components, leaves lower frequency components for the control to handle, and keep the weight and volume within a reasonable range. In

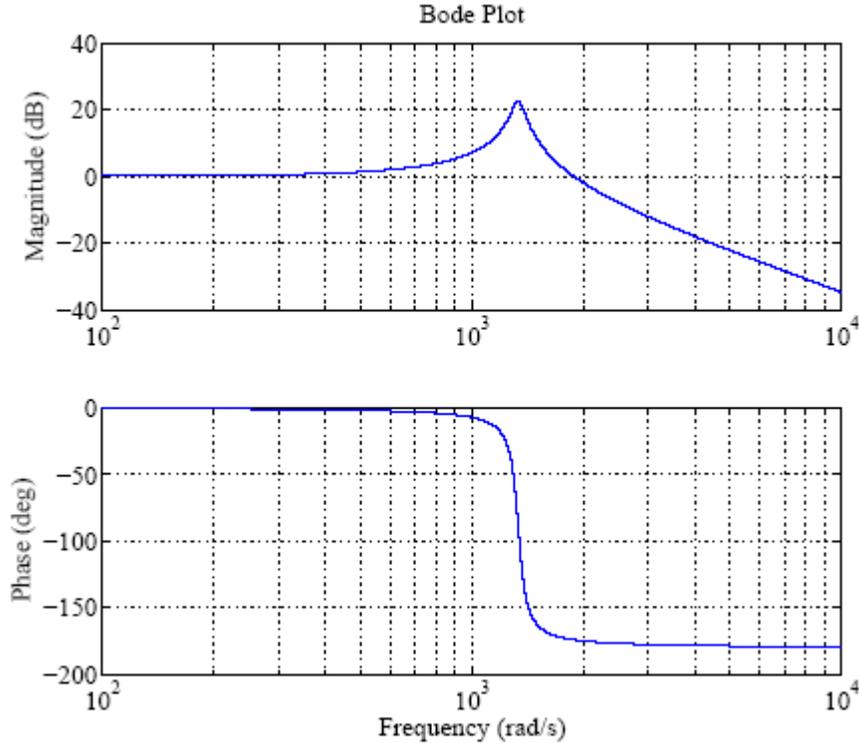


Figure 2.22: Bode plot of the L - C filter.

the split bus topology, the filter input voltage, i.e., v_{pwm} could never be zero, which tends to cause high switching frequency current. In order to suppress this current, a higher L is necessary especially when the switching frequency is not high.

When the current control loop is closed while the voltage loop remains open, the frequency response of the current controlled system is shown in Figure 2.23 and the corresponding discrete-time pole-zero map on Z -plane is shown in Figure 2.24. The responsiveness of the closed-loop control can be measured by bandwidth which is the frequency where the gain falls to -3 dB. In Figure 2.23, it can be observed that the closed-loop system has a bandwidth greater than 10,000 rad/s, which explains the fast response of the current control. Ideally, without the input time delay caused by the microprocessor, the bandwidth of DSMC reaches half of the sampling frequency.

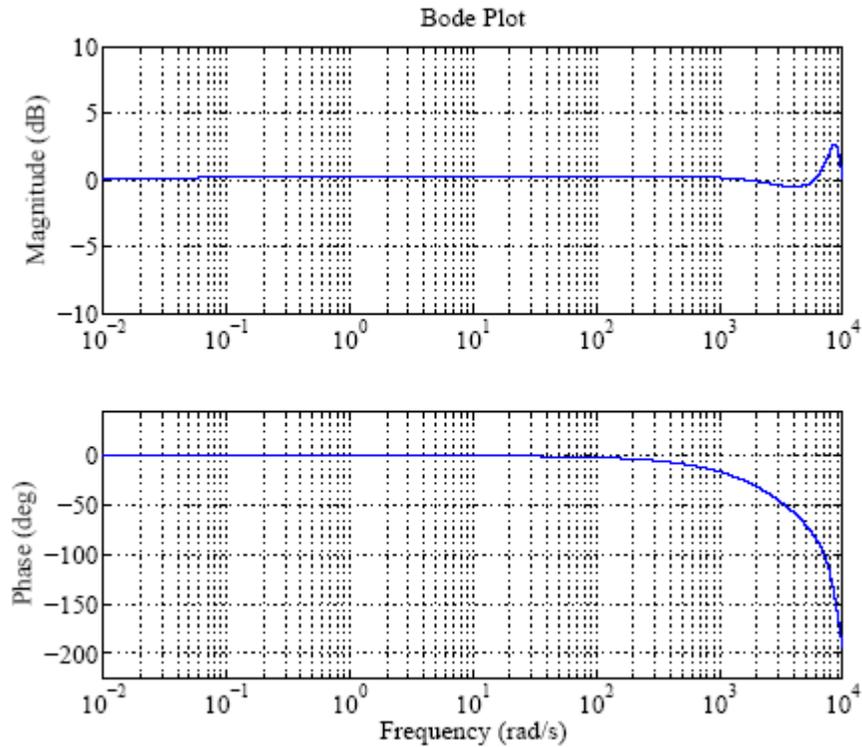


Figure 2.23: Bode plot of the closed loop current controlled system.

In 2.24, all closed-loop poles are in the unit circle, so that the current control loop is stable.

The closed-loop voltage control has a frequency response shown in Figure 2.25. It can be observed that, with the existence of the RSC, all tracking/rejecting frequencies have a unity gain which is desired.

The discrete-time pole-zero map on Z-plane is shown in Figure 2.26 where all closed-loop poles are in the unit circle, which indicates that the voltage control loop is stable.

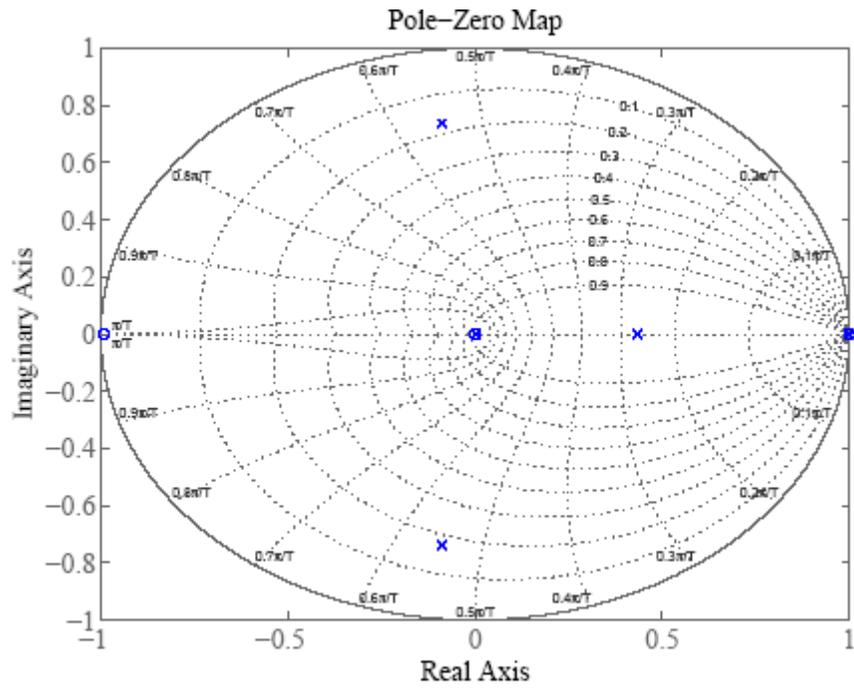


Figure 2.24: Poles and zeros of the closed loop current controlled system.

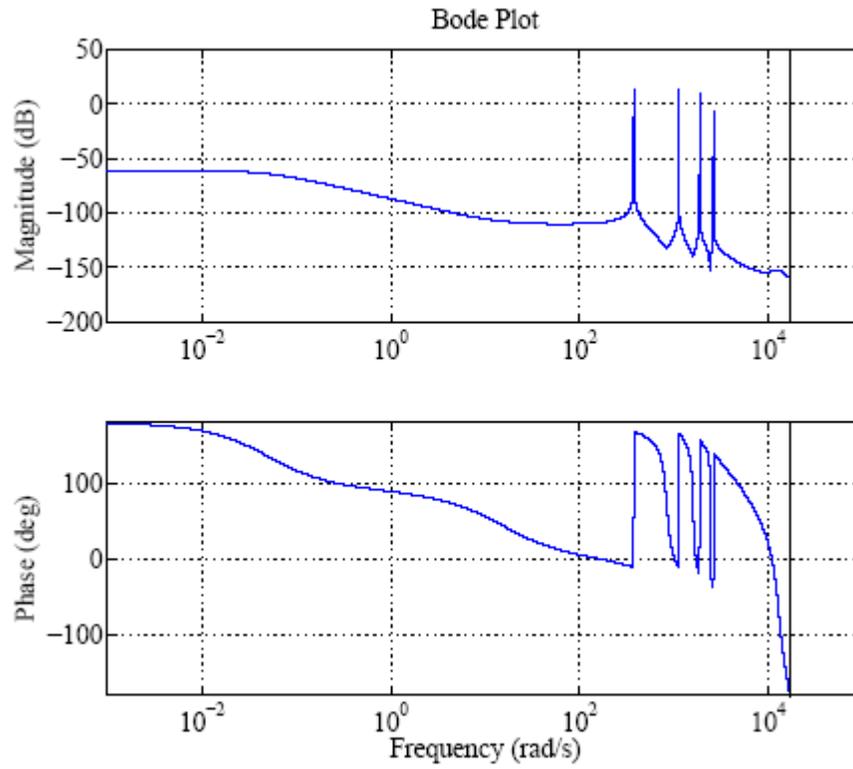


Figure 2.25: Bode plot of the closed loop voltage controlled system.

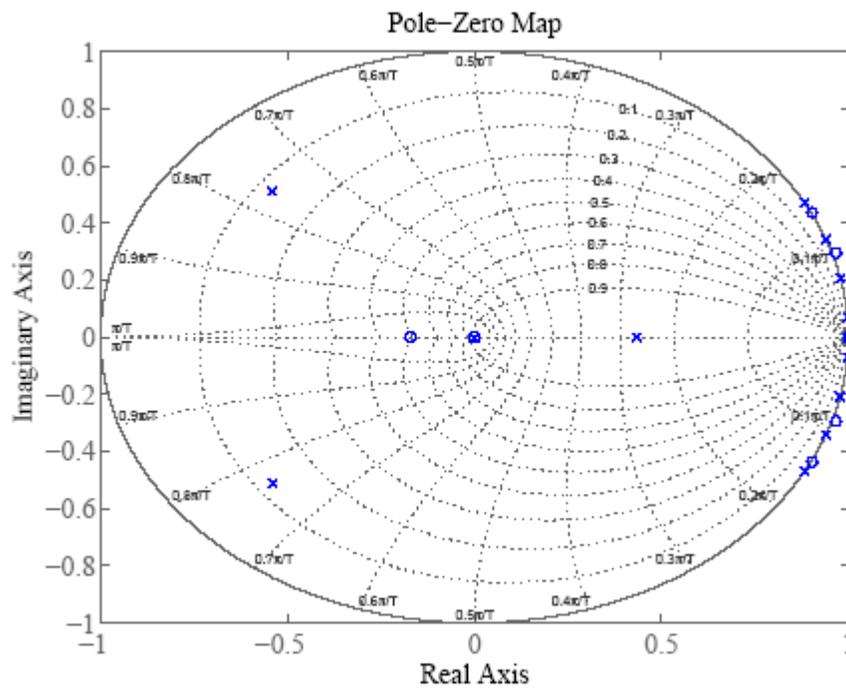


Figure 2.26: Poles and zeros of the closed loop voltage controlled system.

2.3.2 Time domain simulations

Time domain simulations of the closed system have been performed under various load scenarios, including both steady state and transient. A computer simulation software Matlab[®] with Simulink SimPowerSystems Blockset is used.

Steady state RMS output voltages and THDs under different types of load have been presented in Table 2.3. The load types include 5 kVA balanced resistive load, unbalanced resistive loads applied on phase *A* only and on both phases *A* and *B*, 5 kVA inductive load with 0.8 power factor, no load, and nonlinear load with crest factor 2:1, where the crest factor is equal to the peak amplitude of a waveform divided by the RMS value. It can be observed from the table that the proposed control technique results nearly zero steady state error and THD lower than 1% for all tested load types.

Load Type	RMS Load voltages (V)			THD
	$V_{load,A}$	$V_{load,B}$	$V_{load,B}$	
Resistive load	120.0	120.0	120.0	0.80%
Unbalanced <i>A</i>	120.0	120.0	120.0	0.47%
Unbalanced <i>A&B</i>	120.0	120.0	120.0	0.52%
Inductive load 4	120.0	120.0	120.0	0.50%
No load	120.0	120.0	120.0	0.70%
Nonlinear load	120.3	120.3	120.5	0.98%

Table 2.3: Simulation results of steady state performances of the proposed control

technique.

The output waveforms of load voltages, load currents, inverter currents, RMS load voltages, and ground current in the above scenarios are shown in Figures 2.27 to 2.31. In the balanced load scenarios, the 0-axis ground current, including the capacitor current, does not have low frequency components besides switching frequency. However, in the unbalanced load cases, the ground current has a fundamental component and in the nonlinear load case, it has a 3rd harmonic dominant ac component.

The transient response of the control has been demonstrated in Figures 2.32 and 2.33, where a full resistive load is instantaneously applied to or removed from the output terminal. The figures show that the voltage waveforms are only slightly affected by the load transients and restored to steady state in very short period of time, i.e., the waveform dents last for only 2 ms, the RMS values show about 2 V deviations on each transient, which last for about 20 ms.

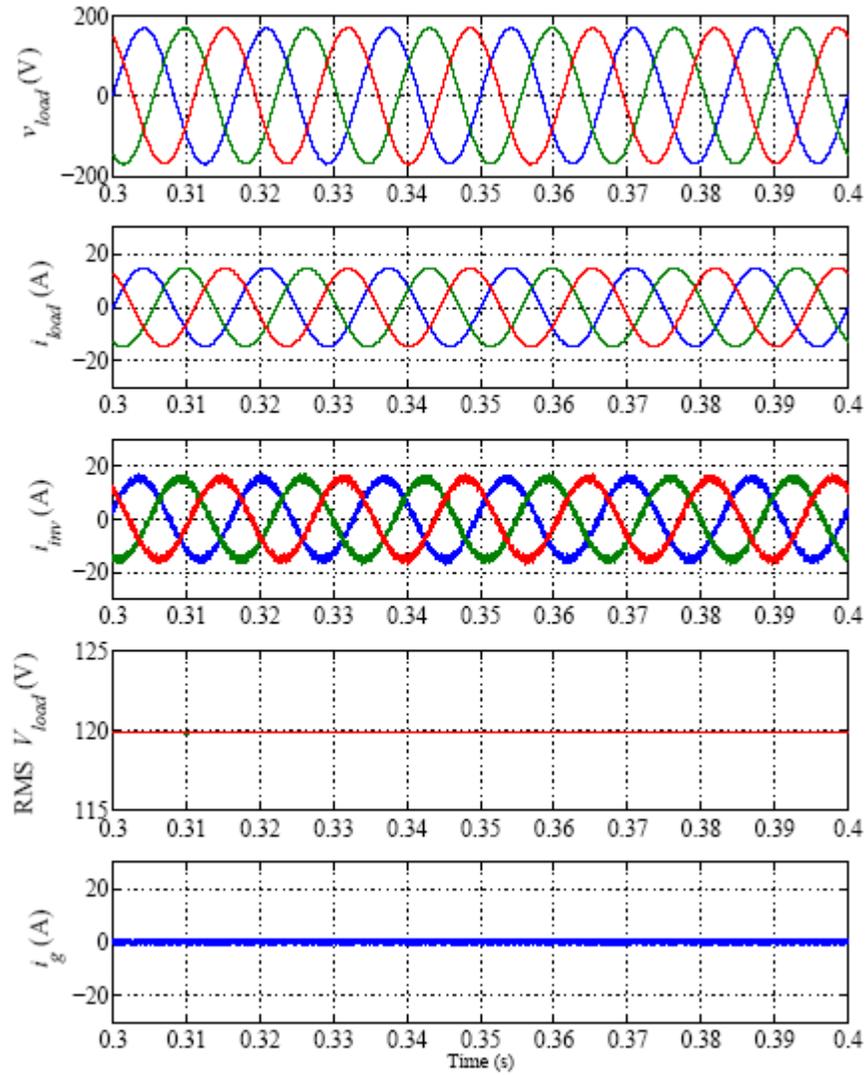


Figure 2.27: Simulation under full resistive load.

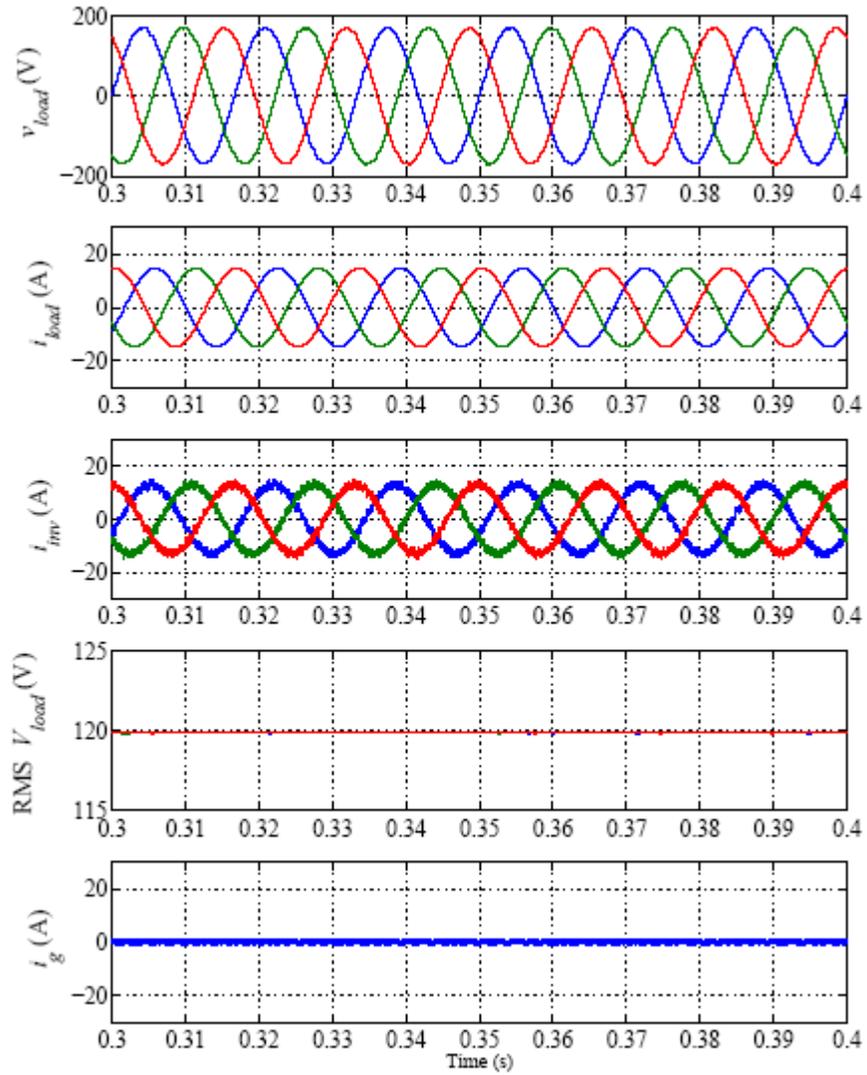


Figure 2.28: Simulation under full inductive load with power factor 0.8.

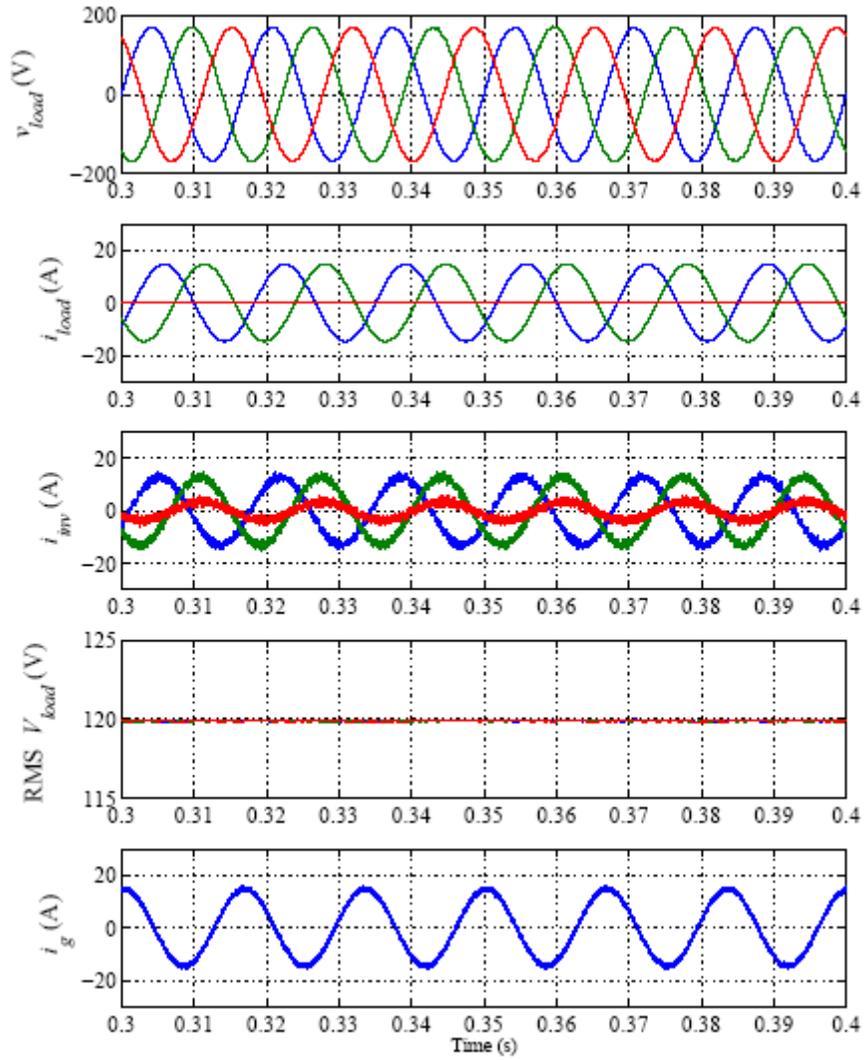


Figure 2.29: Simulation under unbalanced resistive load - phases A and B are fully loaded.

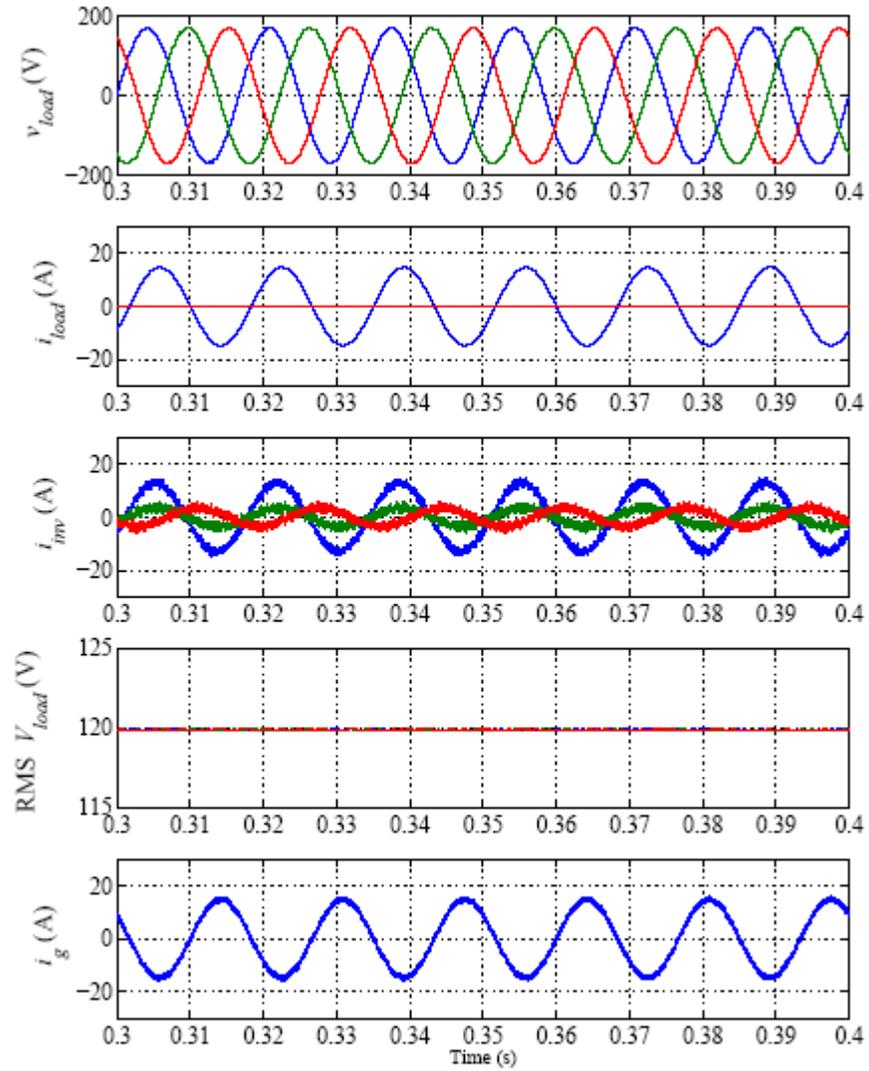


Figure 2.30: Simulation under unbalanced resistive load - phase A is fully loaded.

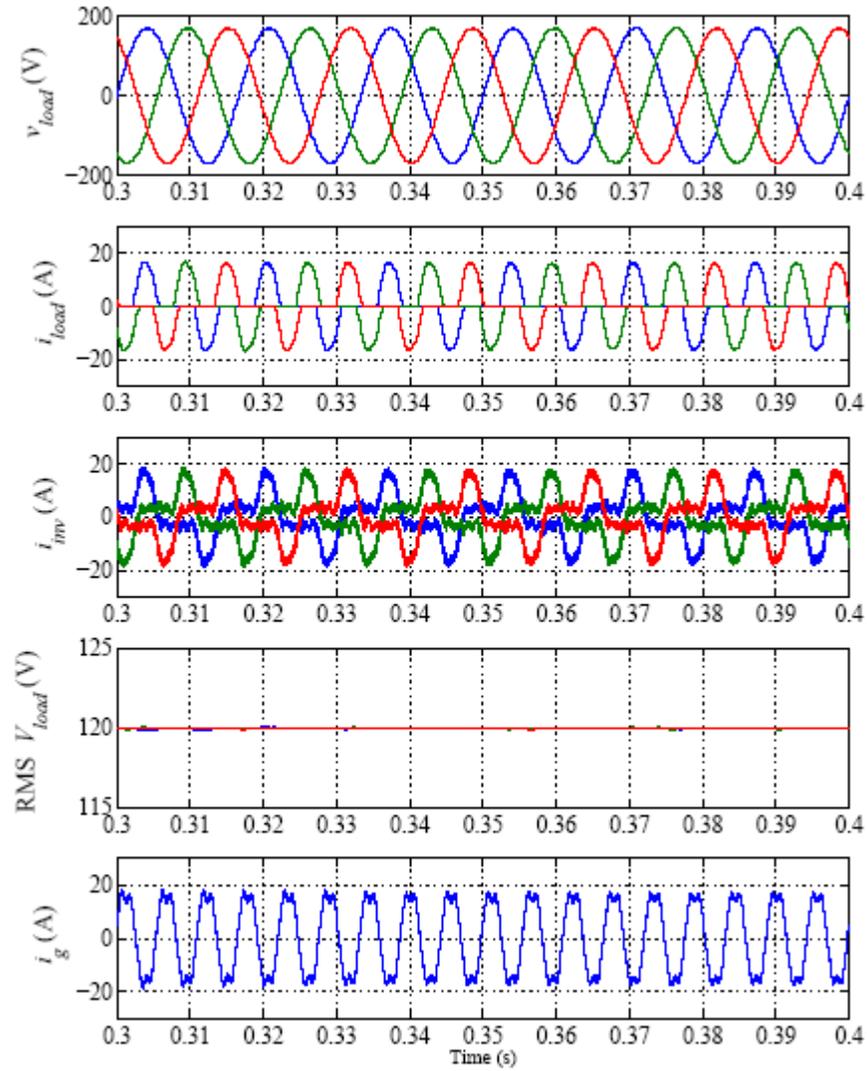


Figure 2.31: Simulation under nonlinear load with crest factor 2:1.

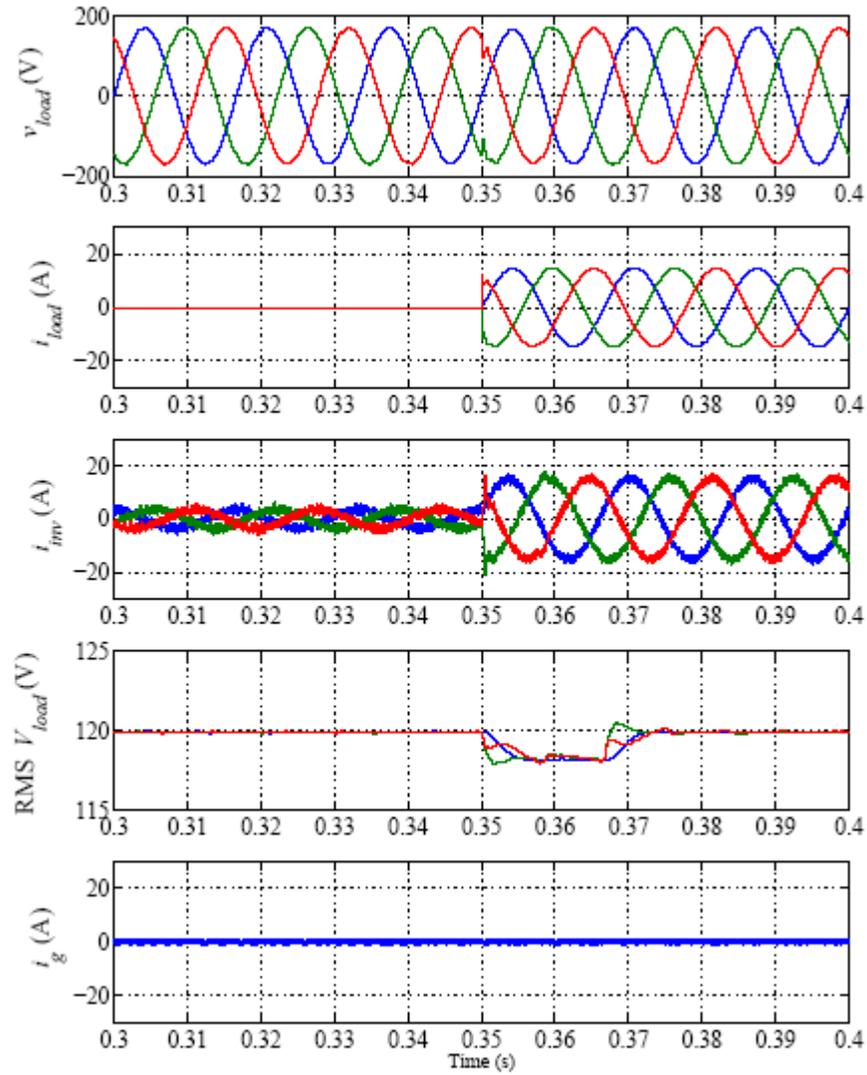


Figure 2.32: Simulation of transient response at load change from 0 to 100%.

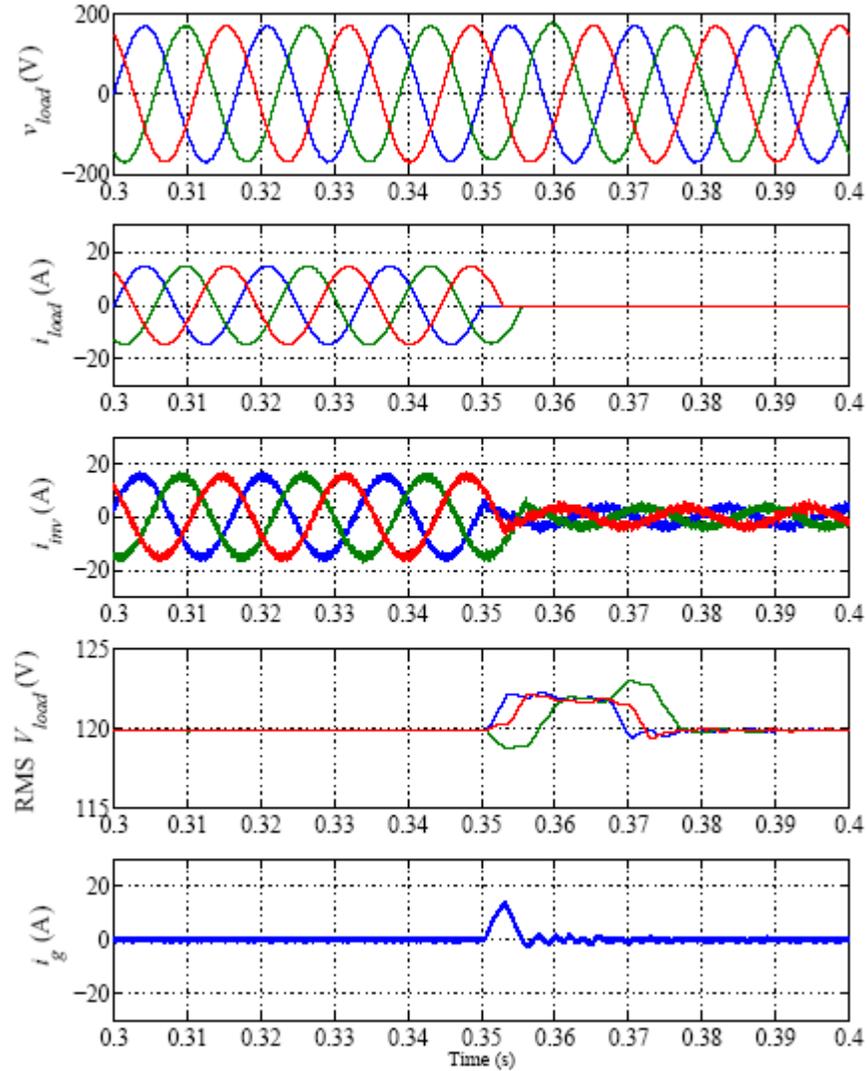


Figure 2.33: Simulation of transient response at load change from 100% to 0.

2.3.3 Experimental results

The experimental setup

Experimental tests of the proposed control technique have been performed on a 1 kVA prototype system with ± 200 V dc bus and a greater inductance $L_f = 60.2$ mH is used to provide strong suppression of the 0-axis switching frequency current which

affects control performance significantly in practical systems. The filter capacitance $C_f = 55 \mu\text{F}$ remains the same as above. The power converter uses SEMIKRON[®] SKM 50GB 123D IGBT modules with SKHI 22 gate drives. A Texas Instruments[®] TMS320LF2407A digital signal processor (DSP) with a Spectrum Digital[®] evaluation module (EVM) have been used as the digital controller. The block diagram of the setup is shown in Figure 2.34.

In Figure 2.34, the voltage divider is used to sense high voltages by lowering it down within $\pm 12 \text{ V}$ range which is operable by operational amplifiers. LEM[®] LA55-P current output Hall effect current transducers are used to measure currents with a $75 - 0.1\%$ burden resistor for each channel.

The signal conditioning stage adjusts the input measurement signals into 0-3.3 V range with 1.65 V dc offset matching the requirement of the analog to digital conversion of the DSP. Texas Instruments[®] TL074BCN four channel operational amplifiers are used in the signal conditioning.

The optical isolation interfaces the DSP pulse-width modulation output pins with the IGBT gate drives. The isolation prevents the DSP from possible damages caused by fault in the power stage. Dual-channel Hewlett Packard[®] HCPL-2232 optocouplers are used.

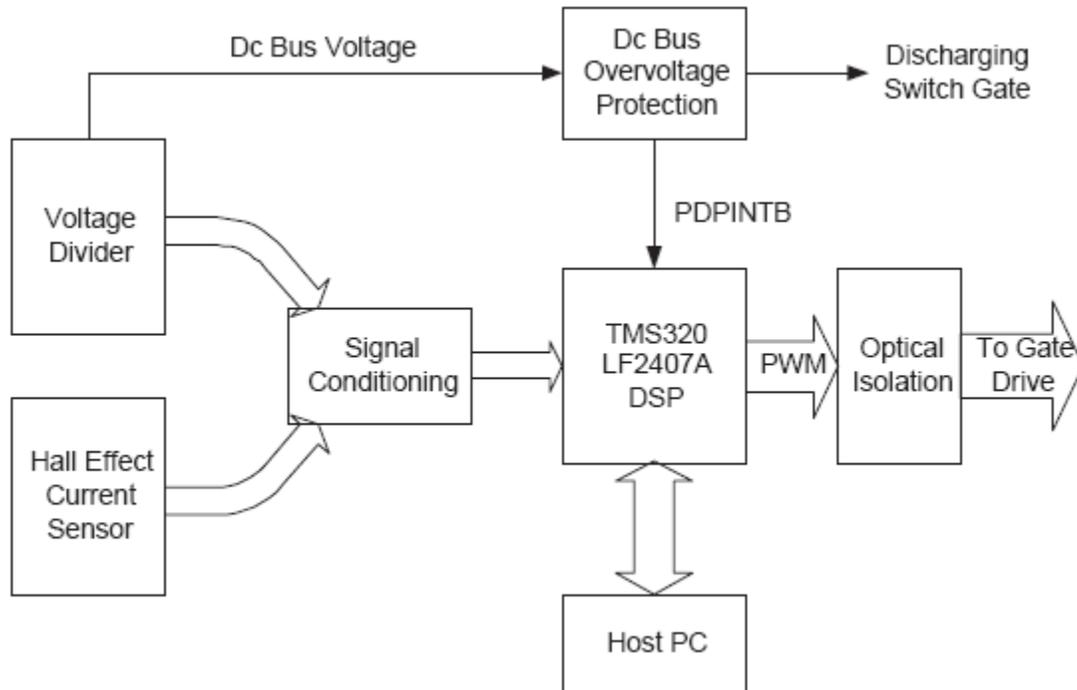


Figure 2.34: Block diagram of the experimental setup.

The dc bus overvoltage protection circuit protects the dc electrolytic capacitors and the IGBT modules from possible overvoltage fault caused by the front end. Once overvoltage is detected, the front-end power supply will be shut down and a dc bus discharging circuit will be switched on to lower the dc bus voltage.

A photo of the setup is shown in Figure 2.35.

The test results

The test waveforms have been presented in Figures 2.36 to 2.45. Although the experimental results are less perfect compared to the simulation ones, they are reasonably good to demonstrate the effectiveness of the proposed control technique.

The experimental results can be improved by using faster PWM switching frequency,

which reduces switching frequency current and allows higher control gain leading to better control performance.

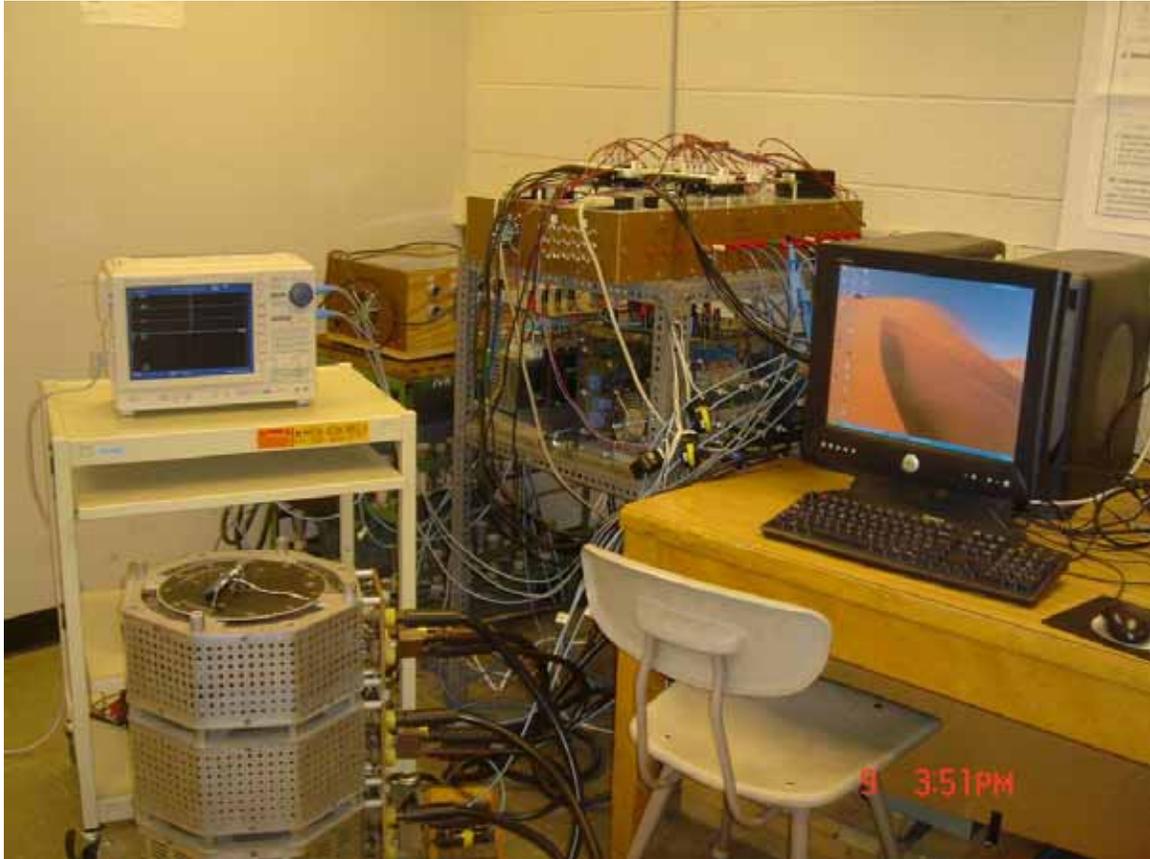


Figure 2.35: A picture of the experimental setup.

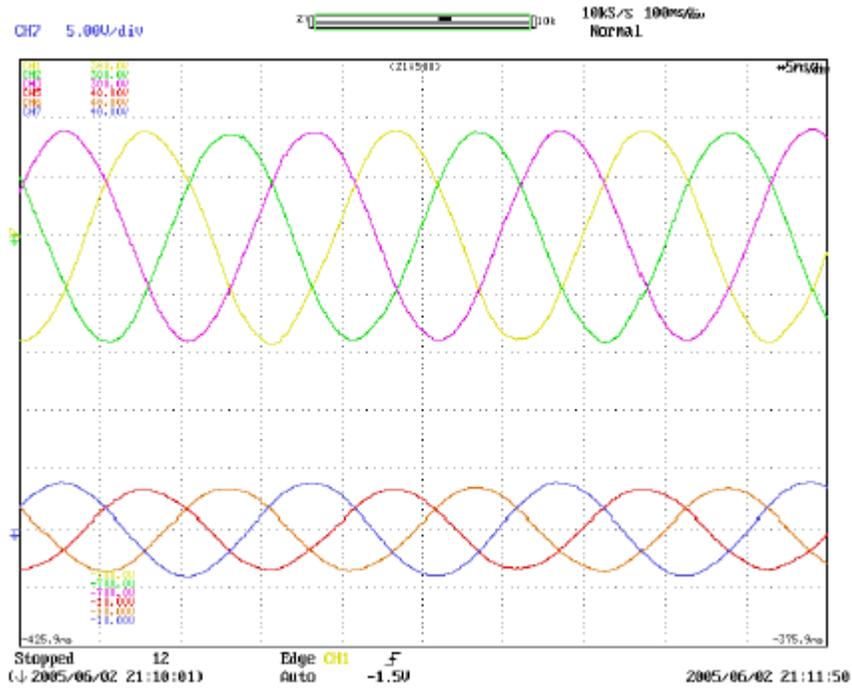


Figure 2.36: Experimental result of load voltages and currents under resistive load - upper: 100V/div and lower: 1A/div.

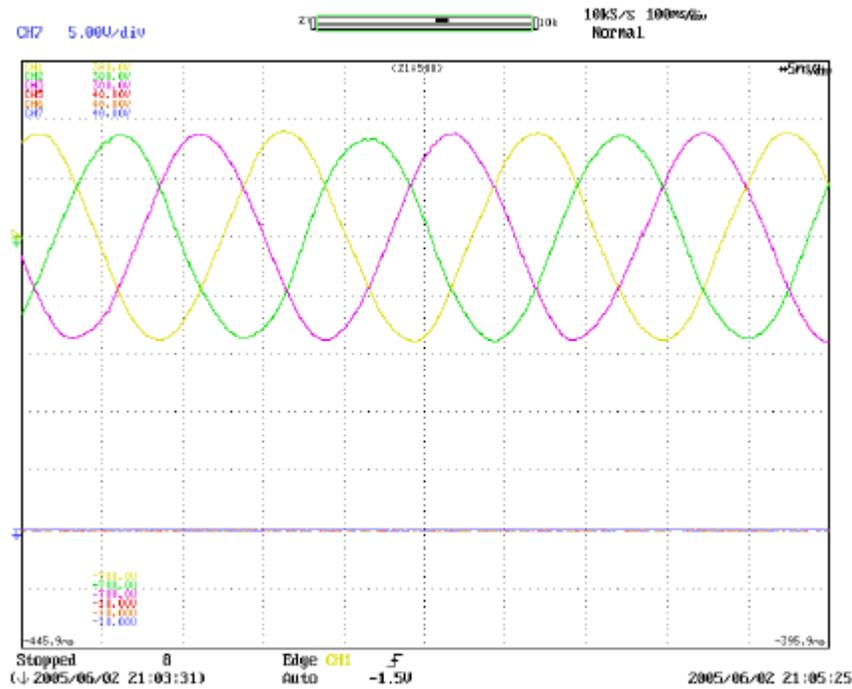


Figure 2.37: Experimental result of load voltages and currents under no load - upper: 100V/div and lower: 1A/div.

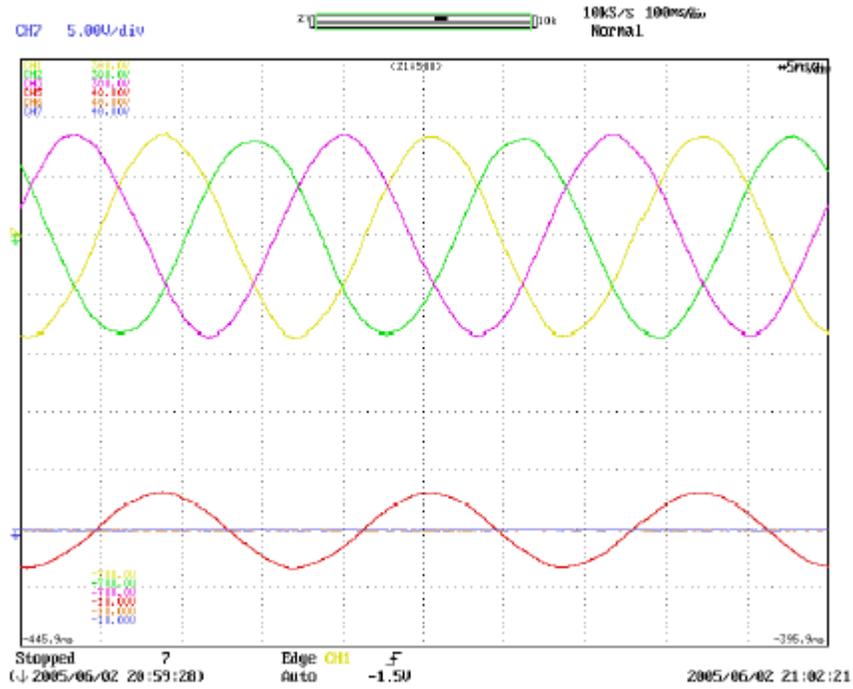


Figure 2.38: Experimental result of load voltages and currents under unbalanced load, phase A is loaded - upper: 100V/div and lower: 1A/div.

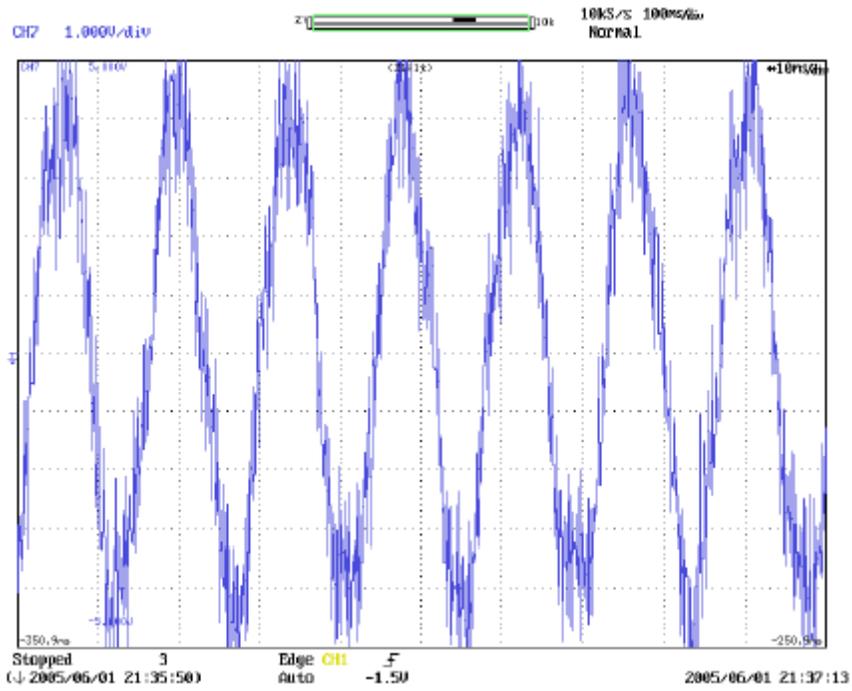


Figure 2.39: Experimental result of ground current under unbalanced load, phase A is loaded, 1A/div.

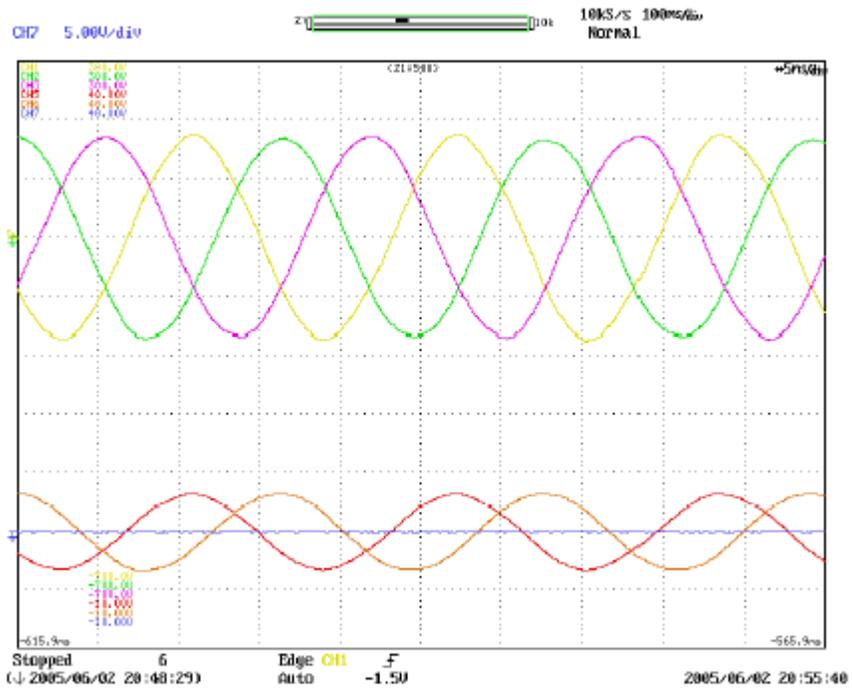


Figure 2.40: Experimental result of load voltages and currents under unbalanced load,

phases A and B are loaded - upper: 100V/div and lower: 1A/div.

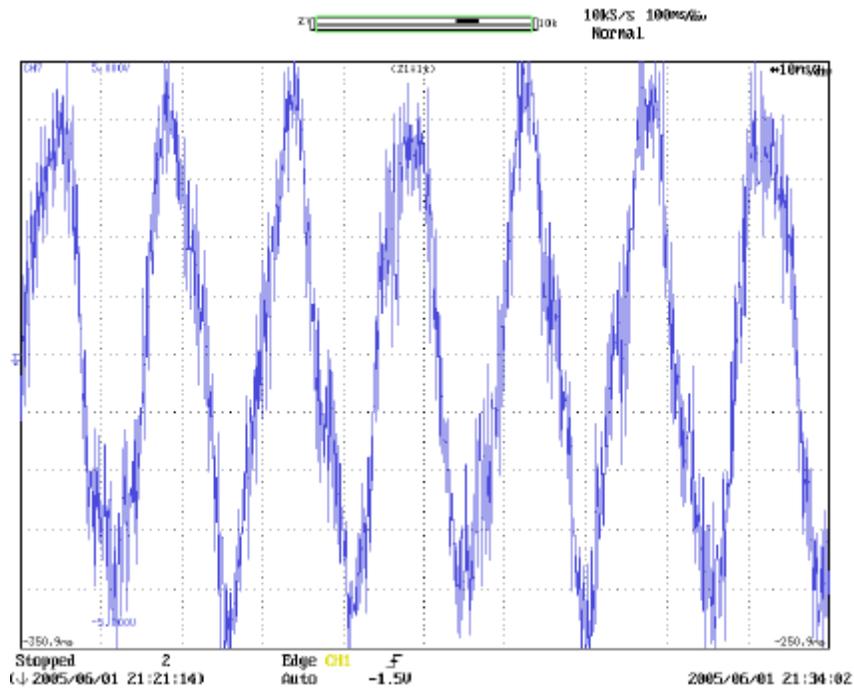


Figure 2.41: Experimental result of ground current under unbalanced load, phases A and B are loaded, 1A/div.

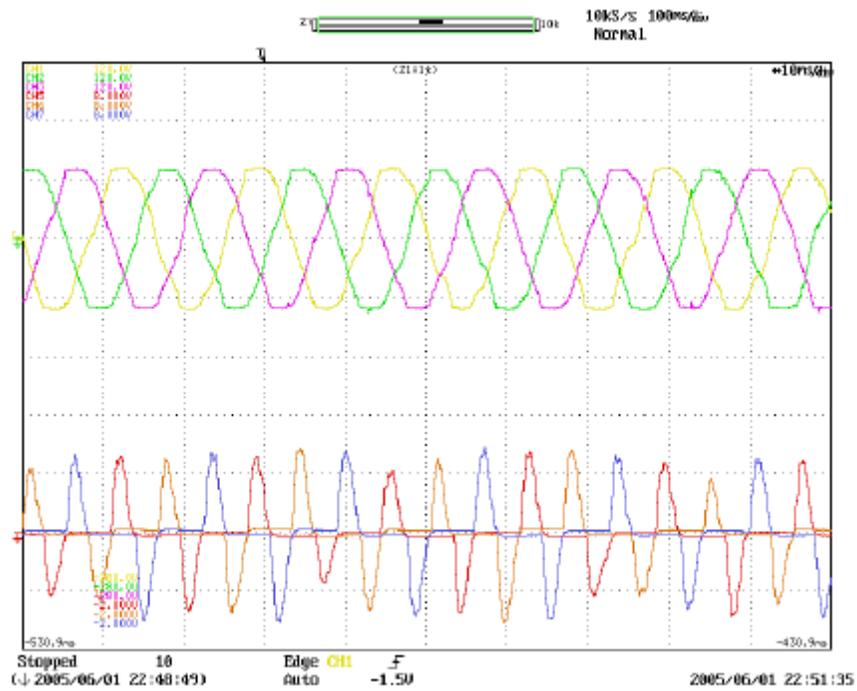


Figure 2.42: Experimental result of load voltages and currents under nonlinear load

- upper: 40V/div and lower: 1A/div.

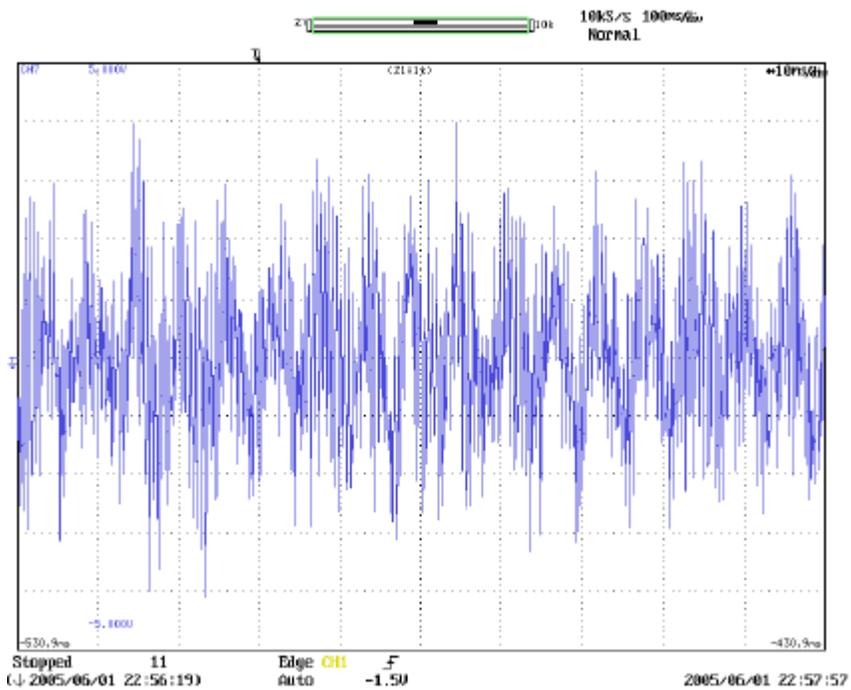


Figure 2.43: Experimental result of ground current under nonlinear load, 1A/div.

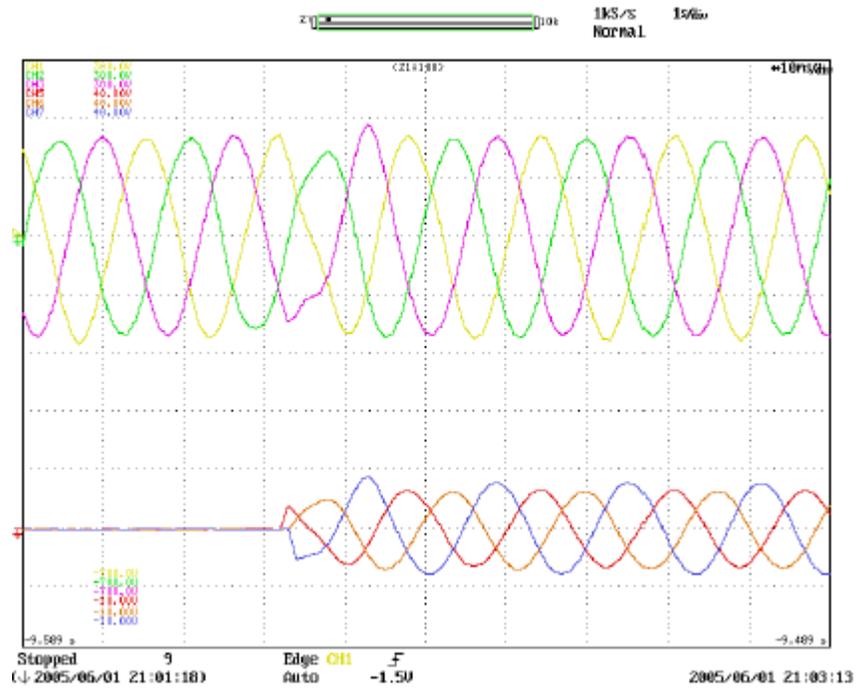


Figure 2.44: Experimental result of load voltages and currents in stepping up load transient - upper: 100V/div and lower: 1A/div.

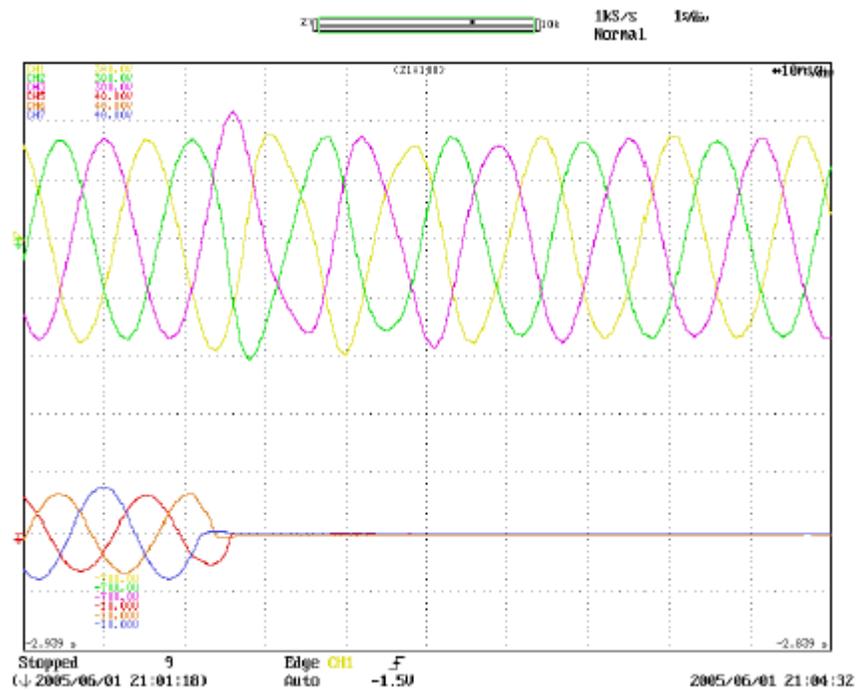


Figure 2.45: Experimental result of load voltages and currents in stepping down load transient - upper: 100V/div and lower: 1A/div.

2.3.4 Stationary $\alpha\beta 0$ reference frame vs. ABC reference frame

One simulation research has been performed comparing the performances of conducting the controls in stationary $\alpha\beta 0$ reference frame vs. ABC reference frame.

It is natural to use the MSVPWM if the $\alpha\beta 0$ reference frame is used and to use conventional sine wave PWM if the ABC reference is used.

As reviewed in Section 1.2.4, mutual-transformable relationship can be constructed between the conventional SVPWM and USPWM which is a sine wave PWM technique in a three-phase three-wire system. It is imaginable that there exists a similar relationship between the MSVPWM and sine wave PWM while the detailed proof deserves further investigation. If this is true and the harmonic issues in the switching frequency and vicinity are ignored, conditional equivalence between the two modulation strategies in linear modulation area can be conceivable in terms of control performance point of view. In other words, in linear modulation area, the control performances of the two modulation strategies are comparable. If this statement is true again, it can be demonstrated that the statement becomes untrue when the modulation index approaches 1 due to the limited dc bus voltage or high modulation references.

When the modulation index a approaches 1, as shown by the algorithm in Sec-

tion 2.2.4, $T_1 + T_2$ approaches T_0 and the space for 0-axis modulation tends to zero. This strategy implies a higher priority for the modulation of $\alpha - \beta$ axes than that of the 0-axis when the dc bus voltage is limited. In other words, when the 0-axis modulation is saturated at T_0 , the modulation of $\alpha - \beta$ references can still be linear. This is not the case in sine wave PWM, where the total modulation reference is saturated

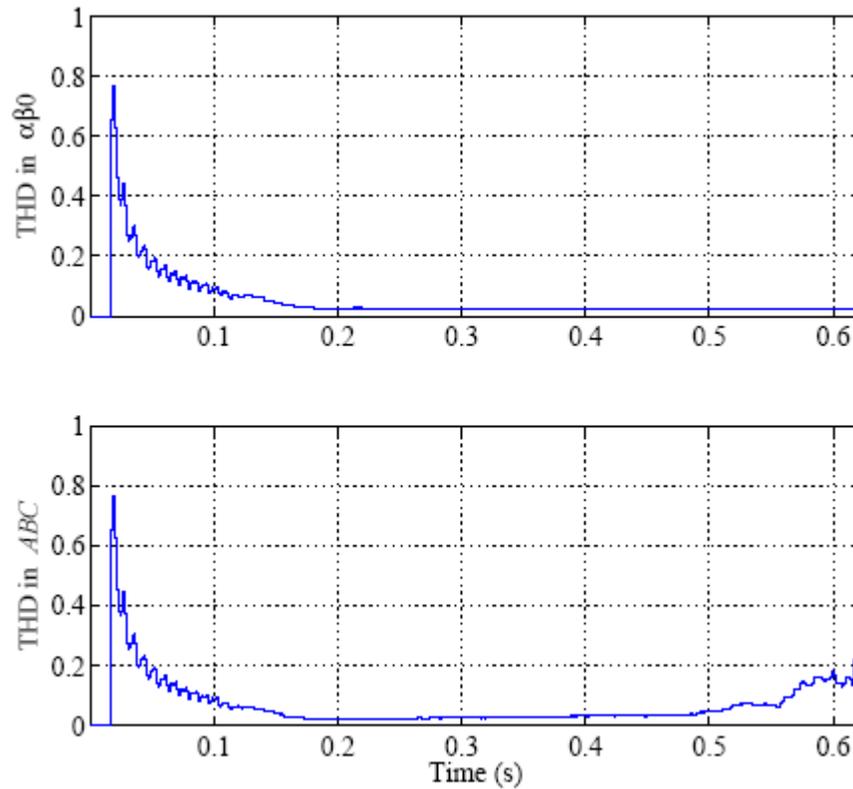


Figure 2.46: THD curves of the same control conducted in $\alpha\beta 0$ and ABC reference frames.

as the modulation index approaches 1 given the condition that over-modulation is not allowed due to its negative impact on the modulation.

Simulation results have demonstrated that the above difference about the reference

frames does matter in the control performance. In the simulations using two different reference frames, the same load, the same L - C filter, the same dc bus voltage ± 257.5 V, and the same controllers, are used for the comparison purpose. Figure 2.46 shows the THD performances of the two. The one using $\alpha\beta 0$ reference frame and MSVPWM yields steady low THD consistently while the one using ABC reference frame and sine-wave PWM ends up with rising THD and losing stability.

The above comparison indicates that the control in the stationary $\alpha\beta 0$ reference frame with MSVPWM to allows use of lower dc bus voltage than the one using ABC reference frame and sine wave PWM. This property is desirable in control of DG units with the three-phase four-wire split dc bus topology because the relatively low dc bus voltage utilization of this topology tends to ask for better usage of the dc bus voltage to avoid using very high dc bus voltage for cost concerns.

2.4 The Robust Stability

2.4.1 Basic ideas about uncertainty, robust stability, and μ -analysis

The proposed DG control technique, including the RSC and DSMC controllers, is a model based control. However, the mathematical model can never precisely describe the true physical process. The mismatch between the model and the true

process is caused by unmodeled dynamics which is so called uncertainty. Uncertainty mostly contains two sources - parametric uncertainty and external disturbances. The uncertainty is unknown in practice but it is reasonable to assume its boundary is known, which enables mathematical analysis. There are two typical ways to model uncertainty - to model it as external inputs or as parametric perturbation to a nominal model [119]. In this section, the latter approach will be used. There are also two ways to analyze uncertainty - to analyze it as unstructured uncertainty or structured uncertainty. Unstructured uncertainty refers to the case where all sources of uncertainty are lumped into a single perturbation [47]. With this strategy, a single boundary of all perturbations is used which yields very conservative analysis result in terms of robust stability. Structured uncertainty refers to the case where the individual sources of uncertainty are described separately [47]. This approach increases the complexity of the analysis but gives a less conservative result. Structured uncertainty based analysis will be used in this section.

As stated in Section 1.2.3, a feedback control system is said to achieve robust stability if it remains stable for all considered perturbations caused by uncertainty in the plant.

Structured singular value μ can be used to analyze the stability robustness of a multi-input-multi-output (MIMO) linear system under structured uncertainty. In order to do so, an uncertainty model needs to be constructed as shown in Figure 2.47, where M represents a state space representation of transfer matrix of a known stable

MIMO linear system with a dimension $n \times n$ and Δ is a structured uncertainty matrix typically with block diagonal format including perturbation values of all uncertainty sources. Define set

$$\Delta = \{\text{diag}[\delta_1 I_{r_1}, \dots, \delta_S I_{r_S}, \Delta_1, \dots, \Delta_F]: \delta_i \in \mathbb{C}, \Delta_j \in \mathbb{C}^{m_j \times m_j}\}, \quad (2.39)$$

where $\delta_i I_i$ denotes a repeated scalar block and Δ_j denotes a full block, integers S and F represent the number of repeated scalar blocks and the number of full blocks, respectively, and \mathbb{C} denotes the complex set. Then $\Delta \in \Delta$ and

$$\sum_{i=1}^S r_i + \sum_{j=1}^F m_j = n.$$

For $M \in \mathbb{C}^{n \times n}$, the structured singular value is defined as

$$\mu_{\Delta}(M) \triangleq \frac{1}{\min\{\bar{\sigma}(\Delta): \Delta \in \Delta, \det(I - M\Delta) = 0\}}, \quad (2.40)$$

where $\bar{\sigma}(\Delta)$ is the largest singular value of Δ , unless no $\Delta \in \Delta$ makes $I - M\Delta$ singular, in which case $\mu_{\Delta}(M) \triangleq 0$.

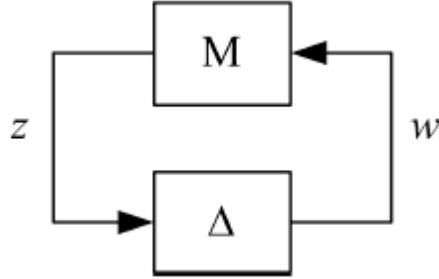


Figure 2.47: Generalized uncertainty model for robust stability analysis.

According to Theorem 10.7 in [119], robust stability of system in Figure 2.47 is

achieved for all Δ with $\|\Delta\|_{\infty} < 1$ if and only if

$$\sup \mu_{\Delta}(M) \leq 1. \quad (2.41)$$

The value of μ is difficult to obtain in a real system while the upper bound can be calculated using Matlab[®] function `mu ()` in the Robust Control Toolbox.

2.4.2 Linear fractional transformation and uncertain open-loop model

In order to perform μ -analysis on the robust stability of the system, an uncertain model with the structure shown in Figure 2.47 needs to be constructed.

As stated in Section 2.4.1, uncertainty is modeled as perturbations to a nominal model. In the DG unit discussed in this research, the perturbations include load disturbances. Therefore, the load model should be included in the plant model also,

as shown in Figure 2.48, where all parameters are in per-unit values, and admittance model is used for modeling an inductive load, i.e., $Y_G = 1/R_{load}$, is the complement of the parallel load resistance and $Y_B = 1/L_{load}$ is the complement of the parallel load inductance. Nonlinear load is not considered in this analysis.

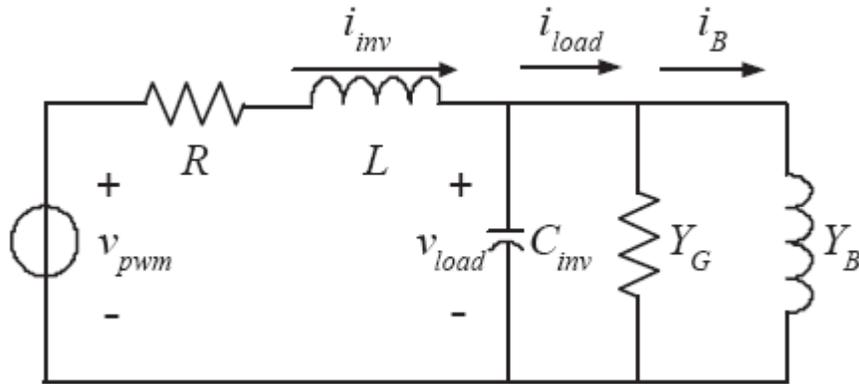


Figure 2.48: One dimensional equivalent circuit for robust stability analysis.

The parametric uncertainty of a component is usually bounded by its manufacturing tolerance. The manufacturing tolerances of the discussed circuit components are

- filter inductor tolerance: $\pm 15\%$,
- filter inductor loss tolerance $\pm 50\%$, and
- filter capacitor tolerance $\pm 6\%$.

The nominal load admittance is 1. Assuming a power factor of 0.8 lagging, the conductance is 0.8 and the susceptance is 0.6. The specification of the DG unit

requires a stable operation range without performance degradation under load from 0 to 200%. This is equivalent to conductance variation from 0 to 1.6 and susceptance variation from 0 to 1.2. Therefore $Y_{G;nom} = 0.8$ and $Y_{B;nom} = \omega_1 B_{nom} = 2\pi \times 60 \times 0.6 = 226.19$ with the same tolerance of $\pm 100\%$.

Therefore, the circuit parameters can be redefined by adding perturbations on top of their nominal values defined in Section 2.1.3 as shown below:

$$L = L_{nom}(1 + L_{tol}\delta L), |\delta L| < 1, \quad (2.42)$$

$$R = R_{nom}(1 + R_{tol}\delta R), |\delta R| < 1, \quad (2.43)$$

$$C = C_{nom}(1 + C_{tol}\delta C), |\delta C| < 1, \quad (2.44)$$

$$Y_G = Y_{G;nom}(1 + Y_{G;tol}\delta G), |\delta G| < 1, \quad (2.45)$$

and

$$Y_B = Y_{B;nom}(1 + Y_{B;tol}\delta B), |\delta B| < 1, \quad (2.46)$$

where L_{nom} , R_{nom} , and C_{nom} equal to the per-unit circuit parameters L , R , and C defined in Section 2.1.3 respectively and $L_{tol} = 0.15$, $R_{tol} = 0.5$, $C_{tol} = 0.06$, $Y_{G;tol} = 1$, and $Y_{B;tol} = 1$.

The dynamic model of the equivalent circuit in Figure 2.48 with redefined parameters where the perturbations are included can be represented by

$$\dot{v}_{load} = -\frac{Y_G}{C}v_{load} + \frac{1}{C}i_{inv} - \frac{1}{C}i_B, \quad (2.47)$$

$$\dot{i}_{inv} = -\frac{1}{L}v_{load} - \frac{R}{L}i_{inv} + \frac{1}{L}v_{pwm}, \quad (2.48)$$

and

$$\dot{i}_B = Y_B v_{load}. \quad (2.49)$$

With the parameter perturbations defined above, linear fractional transformations (LFT) have to be performed to construct an uncertain open-loop model. The purpose for LFT is to pull the perturbations out and make them separate from the nominal model while keeping their interconnections with their own sources.

LFT is defined as follows. Let M be a complex matrix partitioned as

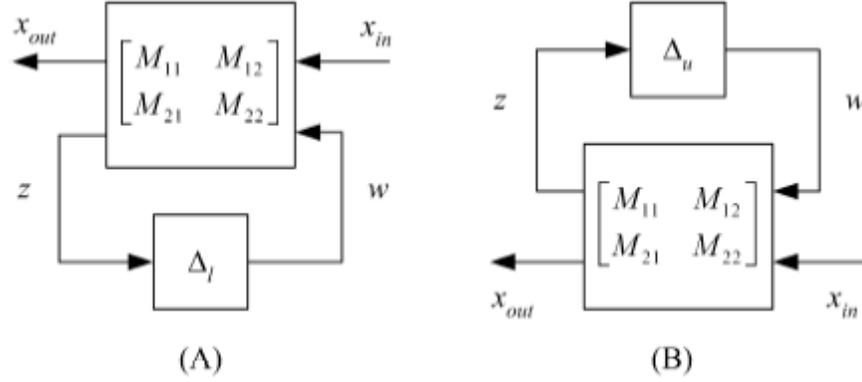


Figure 2.49: A lower LFT (A) and an upper LFT (B).

and let $\Delta_\ell \in \mathbb{C}^{q_2 \times p_2}$ and $\Delta_u \in \mathbb{C}^{q_1 \times p_1}$ be two other complex matrices. A lower LFT with respect to Δ_ℓ can be defined as

$$\mathcal{F}_\ell(M, \Delta_\ell) \triangleq M_{11} + M_{12}\Delta_\ell(I - M_{22}\Delta_\ell)^{-1}M_{21}, \quad (2.50)$$

provided that the inverse $(I - M_{22}\Delta_\ell)^{-1}$ exists. An upper LFT with respect to Δ_u can be defined as

$$\mathcal{F}_u(M, \Delta_u) \triangleq M_{22} + M_{21}\Delta_u(I - M_{11}\Delta_u)^{-1}M_{12}, \quad (2.51)$$

provided that the inverse $(I - M_{11}\Delta_u)^{-1}$ exists.

A lower and an upper LFT are illustrated in Figure 2.49 (A) and (B) respectively, where

$$\begin{bmatrix} x_{out} \\ z \end{bmatrix} = M \begin{bmatrix} x_{in} \\ w \end{bmatrix} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \begin{bmatrix} x_{in} \\ w \end{bmatrix},$$

$w = \Delta_\ell z$ for the lower LFT and

$$\begin{bmatrix} z \\ x_{out} \end{bmatrix} = M \begin{bmatrix} w \\ x_{in} \end{bmatrix} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \begin{bmatrix} w \\ x_{in} \end{bmatrix},$$

$w = \Delta_u z$ for the upper LFT. In the construction of the uncertain open-loop model, only the lower LFT is used.

In Equations 2.47 to 2.49, perturbed parameters L and C appear in denominators.

A lower LFT of L is

$$\frac{1}{L} = \frac{1}{L_{nom}(1 + L_{tol}\delta_L)} = \frac{1}{L_{nom}} - \frac{L_{tol}}{L_{nom}}\delta_L(1 + L_{tol}\delta_L)^{-1} = \mathcal{F}_\ell(M_L, \delta_L),$$

where

$$M_L = \begin{bmatrix} \frac{1}{L_{nom}} & -L_{tol} \\ \frac{1}{L_{nom}} & -L_{tol} \end{bmatrix}.$$

Similarly, $\mathcal{F}_\ell(M_C, \delta_C)$ can be obtained with

$$M_C = \begin{bmatrix} \frac{1}{C_{nom}} & -C_{tol} \\ \frac{1}{C_{nom}} & -C_{tol} \end{bmatrix}.$$

As for the perturbed parameters R , Y_G , and Y_B which are in numerators, their lower

LFTs can be obtained as

$$M_R = \begin{bmatrix} R_{nom} & \Delta R \\ 1 & 0 \end{bmatrix},$$

$$M_{Y_G} = \begin{bmatrix} Y_{G,nom} & \Delta Y_G \\ 1 & 0 \end{bmatrix},$$

and

$$M_{Y_B} = \begin{bmatrix} Y_{B,nom} & \Delta Y_B \\ 1 & 0 \end{bmatrix},$$

where

$$\Delta R \triangleq R_{nom} \cdot R_{tol}, \quad \Delta Y_G \triangleq Y_{G,nom} \cdot Y_{G,tol}, \quad \text{and} \quad \Delta Y_B \triangleq Y_{B,nom} \cdot Y_{B,tol}.$$

These LFTs can be illustrated in Figures 2.50 and 2.51.

After interconnecting all modules in Figures 2.50 and 2.51 based on the relation in Equations 2.47 to 2.49, the system structured perturbation can be illustrated in Figure 2.52.

The dynamics in Figure 2.52 can be represented by the following augmented equation:

$$Y_{aug} = P_{aug} U_{aug}, \tag{2.52}$$

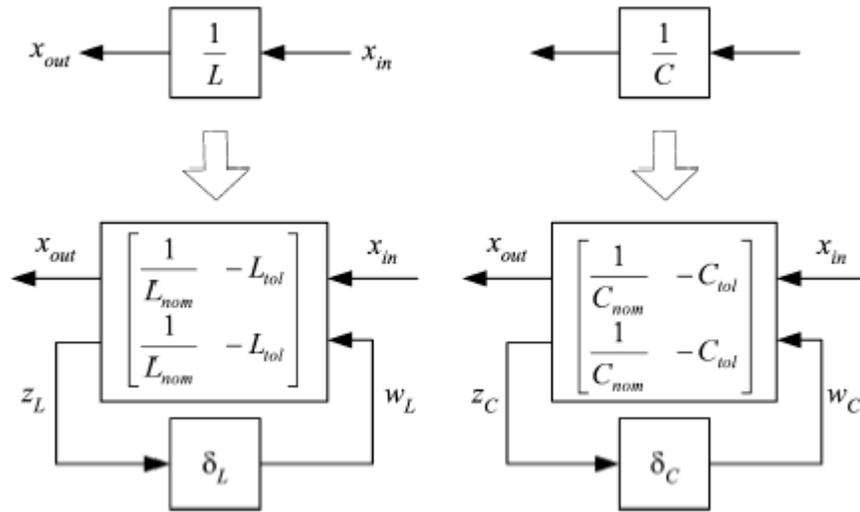


Figure 2.50: LFTs of L and C .

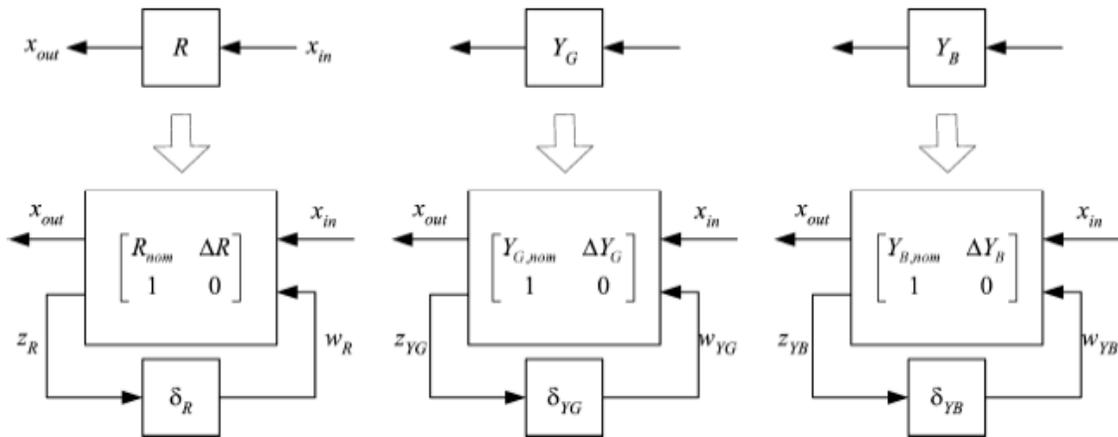


Figure 2.51: LFTs of R , Y_G and Y_B .

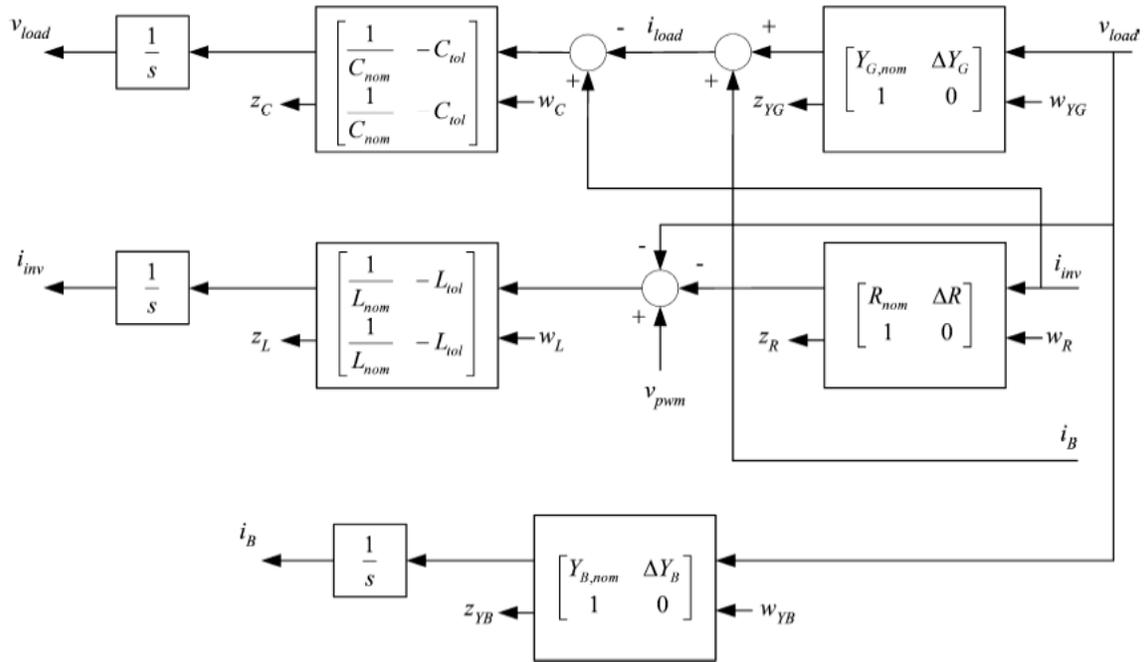


Figure 2.52: Uncertain open-loop model with structured perturbations.

where

$$Y_{aug} = \begin{bmatrix} \dot{v}_{load} \\ \dot{i}_{inv} \\ \dot{i}_B \\ v_{load} \\ i_{inv} \\ i_{load} \\ z_C \\ z_L \\ z_R \\ z_{YB} \\ z_{YG} \end{bmatrix},$$

$$P_{aug} = \begin{bmatrix} -\frac{Y_{G,nom}}{C_{nom}} & \frac{1}{C_{pnom}} & -\frac{1}{C_{nom}} & 0 & -C_{tol} & 0 & 0 & 0 & -\frac{\Delta Y_G}{C_{nom}} \\ -\frac{1}{L_{nom}} & -\frac{R_{nom}}{L_{nom}} & 0 & \frac{1}{L_{nom}} & 0 & -L_{tol} & -\frac{\Delta R}{L_{nom}} & 0 & 0 \\ Y_{B,nom} & 0 & 0 & 0 & 0 & 0 & 0 & \Delta Y_B & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ Y_{G,nom} & 0 & 1 & 0 & 0 & 0 & 0 & 0 & \Delta Y_G \\ -\frac{Y_{G,nom}}{C_{nom}} & \frac{1}{C_{pnom}} & -\frac{1}{C_{nom}} & 0 & -C_{tol} & 0 & 0 & 0 & -\frac{\Delta Y_G}{C_{nom}} \\ -\frac{1}{L_{nom}} & -\frac{R_{nom}}{L_{nom}} & 0 & \frac{1}{L_{nom}} & 0 & -L_{tol} & -\frac{\Delta R}{L_{nom}} & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix},$$

and

$$U_{aug} = \begin{bmatrix} v_{load} \\ i_{inv} \\ i_B \\ v_{pwm} \\ w_C \\ w_L \\ w_R \\ w_{Y_B} \\ w_{Y_G} \end{bmatrix}.$$

The LFTs allow the perturbation block matrix Δ to be pulled out from the nominal model while remaining the perturbation structures through the interconnections -

$W = \{w_C, w_L, w_R, w_{Y_B}, w_{Y_G}\}$ and $Z = \{z_C, z_L, z_R, z_{Y_B}, z_{Y_G}\}$, as shown in Figures 2.53

and 2.54, where v_{pwm} and $Y = \{v_{load}, i_{inv}, i_{load}\}$ are the external input and output.

The model represented in Figures 2.53 and 2.54 are the uncertain open-loop model.

2.4.3 Uncertain closed-loop model

In order to study the impacts of the perturbations on the closed-loop system stability, the controllers have to be taken into consideration. With the external input and output ports, v_{pwm} and v_{load} , i_{inv} , i_{load} , given in Figure 2.53, the controllers can be interconnected with the uncertain open-loop model to form an uncertain closed-loop model.

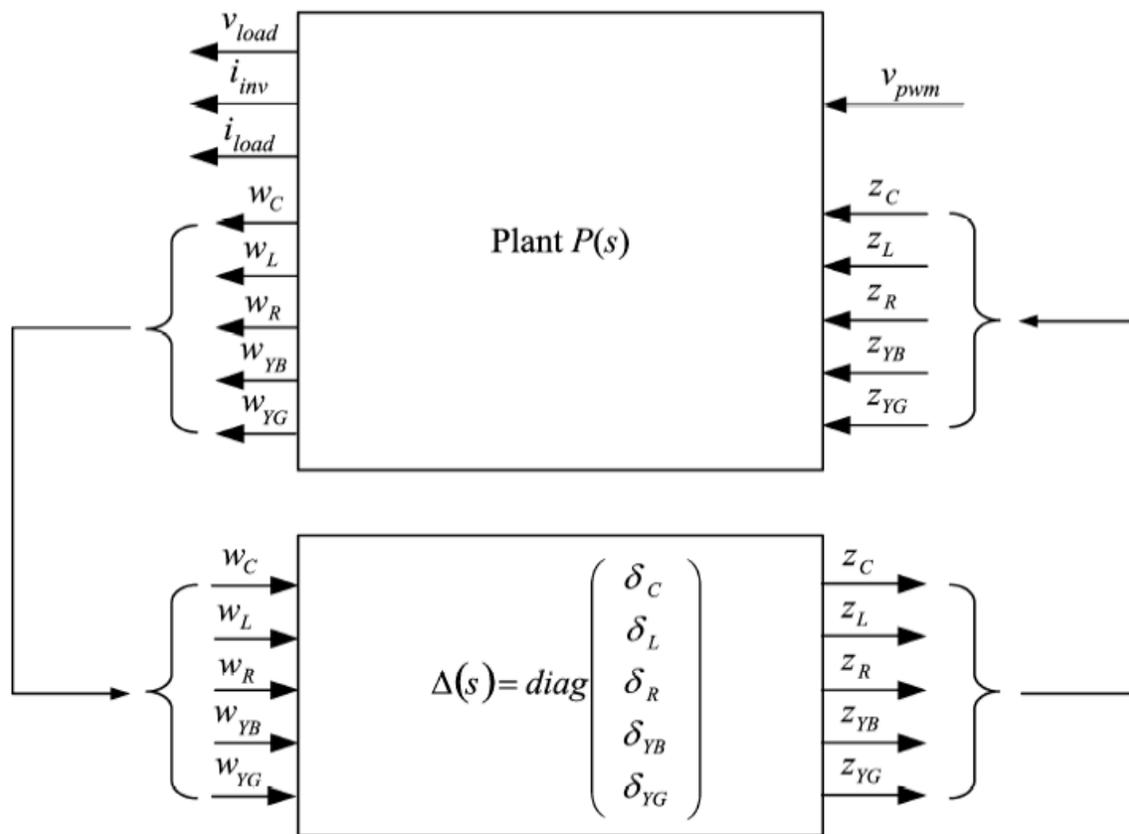


Figure 2.53: Uncertain open-loop model showing the perturbation block matrix.

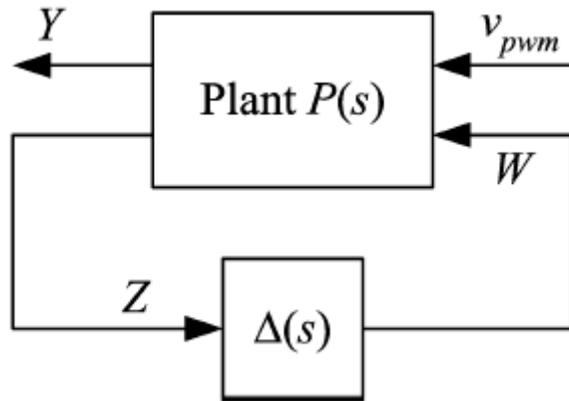


Figure 2.54: Uncertain open-loop model - a higher level block diagram.

The dynamics of the controllers, the DSMC and RSC can be constructed using the designed control parameters obtained in Sections 2.2.1 and 2.2.2. Matlab, with its Control System Toolbox and μ -Analysis and Synthesis Toolbox have been utilized to conduct the interconnection and conversions between continuous time and discrete time.

The following steps are necessary to obtain the closed-loop plant model:

1. Apply Zero Order Hold to the continuous plant $P(s)$, to include the effect of the sample and hold process of the digital sampling process.
2. Transform the discretized plant back to continuous system by applying an inverse Tustin transformation, which has the property of preserving the frequency response of the discrete time systems.
3. Obtain state space representations of the RSC and DSMC with inputs and outputs definitions as shown in Figure 2.55. The combined controller state-space system, containing both the the RSC and DSMC, can be calculated using

Matlab[®] command `sysic()`.

4. The combined controller system is then transformed into a complex plane in continuous domain using the inverse Tustin transformation.
5. Finally, the closed loop plant model M is obtained by invoking the command `sysic()` again to complete the interconnections between the combined controller and the uncertain open-loop model to obtain an uncertain closed-loop model.

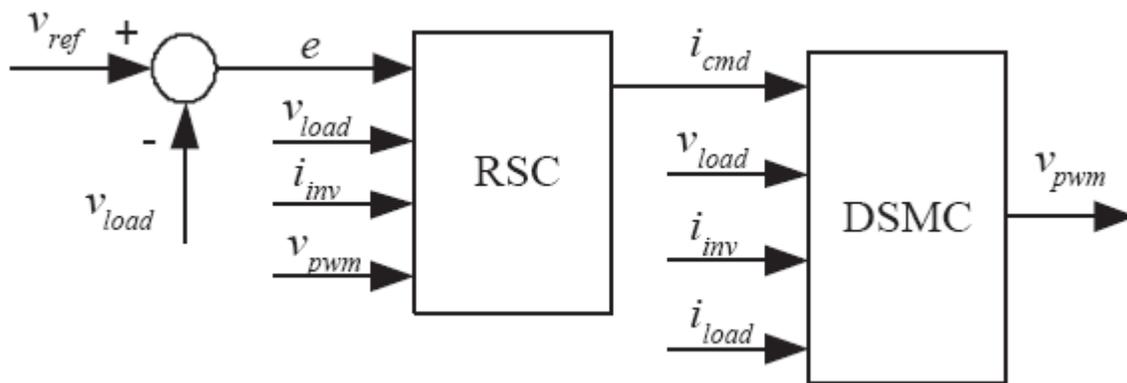


Figure 2.55: Block diagram of the controllers showing the input and output ports.

The uncertain closed-loop model are shown in Figures 2.56 and 2.57 where the latter is a high level diagram resembling the standard format for studying robust stability of systems with uncertainty as shown in Figure 2.47.

2.4.4 Robust stability and gain tuning

With the existence of uncertain closed-loop model, it is possible to conduct robust stability analysis under structured perturbations using the structured singular value

$\mu_{\Delta}(M)$ and study the impact of control gains to the robust stability.

The control parameters obtained for the DSMC in Section 2.2.1 are fixed and there is no need to tune them while those of the RSC can be tuned. As shown in Section 2.2.2, the control gain K is obtained by solving the algebraic Riccati equation in Equation 2.26. The solution of the Riccati equation is dependent on the weight matrix Q which is a function of weights w_p , w_1 , and w_h . Therefore, K can be tuned by adjusting w_p , w_1 , and w_h . Different K values yield different control performances. An example is given in Figure 2.58, which is a simulation comparison of the RMS transient responses of the output voltage v_{load} to the step-up load (0-100%) and step-down load (100%-0) disturbances under three different w_p values, i.e., 0.5, 0.05, and

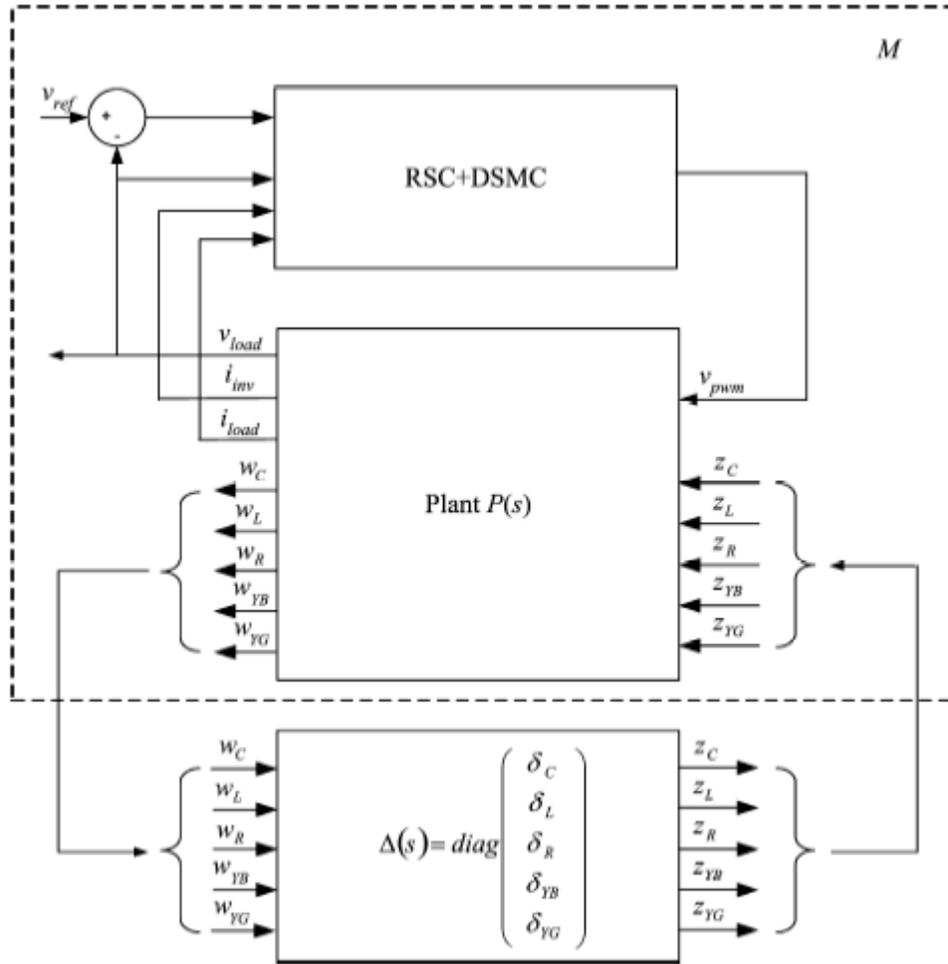


Figure 2.56: Uncertain closed-loop model showing the perturbation block matrix.

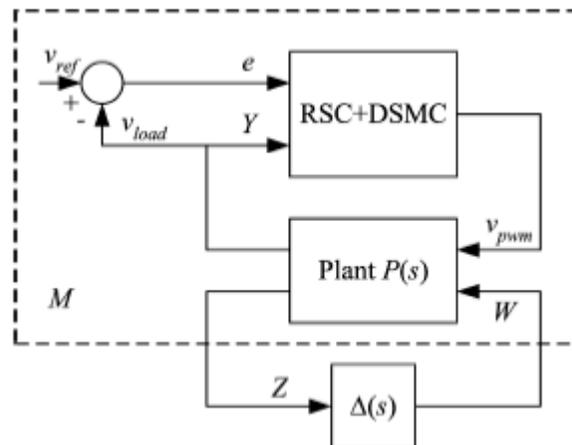


Figure 2.57: Uncertain closed-loop model - a higher level block diagram.

0.005 respectively, where the values of w_1 and w_h are fixed at 5×10^7 and 5×10^5 , respectively. In the simulation, the weight for the control commands is set to 10^{-5} . Since the linear quadratic control is practiced here, it is straightforward that the less the weight on one part of the performance index as shown in Equation 2.25, the more the gain will be resulted for the other part of the performance index. Therefore, less w_p leads to higher gain on the servo states, which yields better tracking/rejecting performance at the specified frequencies. This statement can be verified by observing the curves in Figure 2.58. The figure shows that negative variations of the RMS output voltage are caused under the step-up load transient and positive variations are caused under the step-down case. In both cases, the gain $w_p = 0.005$ leads to the least variations among the three, which is the result of its highest servo gain. However, the above study is conducted without any perturbations. If the perturbations as defined in Equations 2.42 to 2.46 are applied, the robust stability issue will be raised. The robust stability of the perturbed system under different gains has been studied by performing μ -analysis on the system. The robust stability can be checked by observing the the upper bound of $\mu_{\Delta}(M)$ over frequency span of interest as shown in Figure 2.59. In this figure, $w_p = 0.005$ makes the upper bound of μ exceed the robust stability criterion, i.e., $\sup \mu < 1$, at $\omega \approx 25,000$ rad/s, which means unstable. However, the other weight values $w_p = 0.05$ and $w_p = 0.5$ give $\sup \mu < 1$ for the entire frequency span and the lower servo gain case, i.e., $w_p = 0.5$ has more stability margin.

The existing five perturbation sources do not share the contribution to the instability evenly. A study on the contributions of individual perturbations to the same system as studied above has been conducted by calculating frequency responses

$\frac{|z_i(j\omega)|}{|w_i(j\omega)|}$, where $i = 1, \dots, 5$, at $w_p = 0.5$. The resulted frequency responses have been plotted in Figure 2.60, where trace 1 to 5 are the cases with perturbation only on C , L , R , Y_B , and Y_G , respectively. These plots agree with the robust stability analysis result given above that the system achieves the robust stability because all the five magnitude response has a gain less than 1, which is the criterion. However, these five cases yield different robust stability margin. The response to the filter inductance perturbation is the one closest to 1, which yields the least robust stability margin, given the tolerances defined in Section 2.4.2. The robust stability of the closed-loop system under parametric perturbations on the filter inductance has been investigated by finding the positions of the poles representing the dynamics of the inductance under various amount of perturbation measured by the value of δ_L . The pole-zero map is presented in Figure 2.61 where the poles under $\delta_L \in \{0, -0.5, -1.0, -1.5, -2.0, -2.5\}$ have been shown. It can be observed that the closed-loop tends to be unstable when the value of δ_L decreases in that the poles drift to the right half of the complex plane.

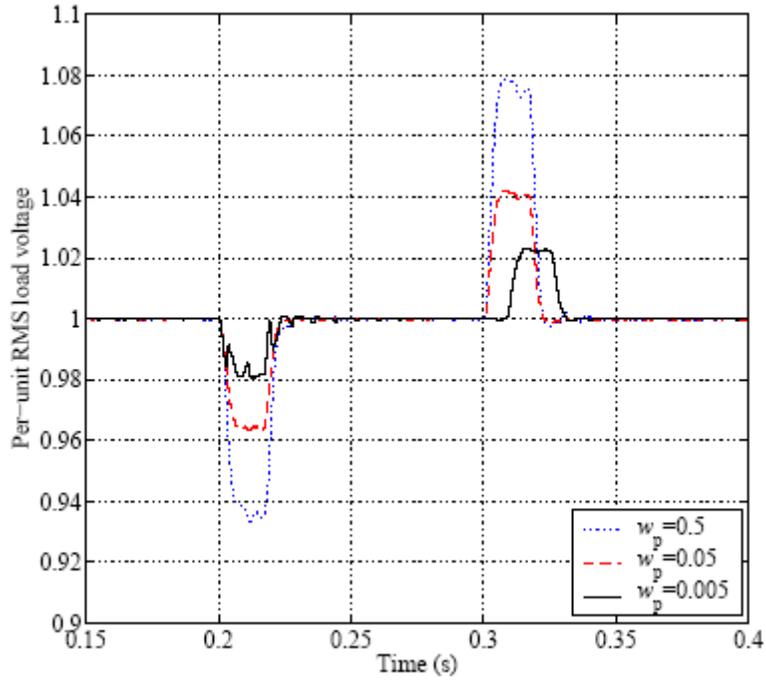


Figure 2.58: RMS performance under different w_p values.

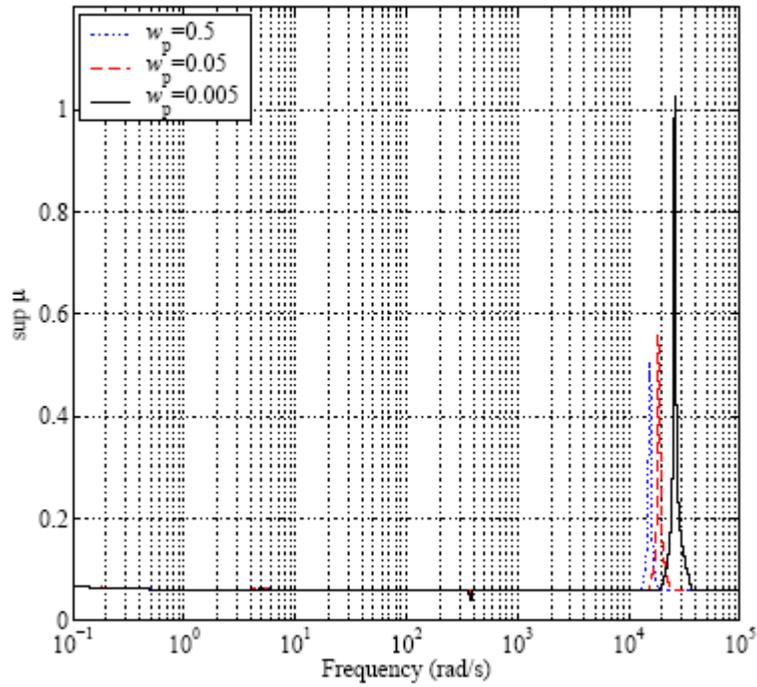


Figure 2.59: Upper bound of $\mu_{\Delta}(M)$ under different w_p values.

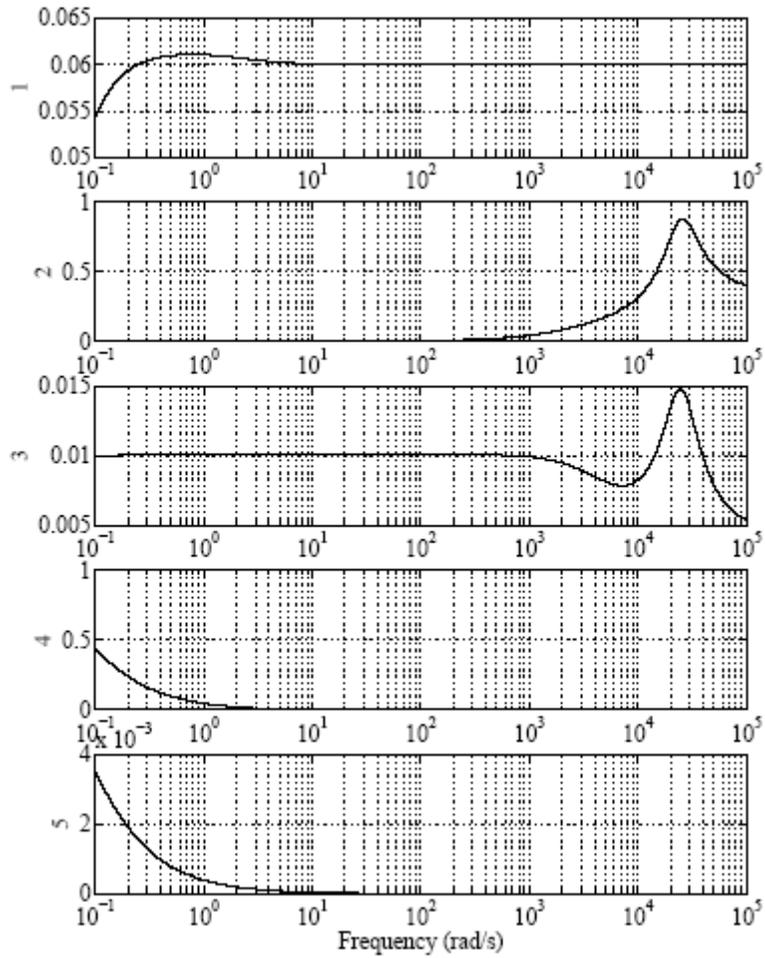


Figure 2.60: Frequency responses under individual perturbations at $w_p = 0.05$, magnitude only, i.e., $\frac{|z_i(j\omega)|}{|w_i(j\omega)|}$, where $i = 1, \dots, 5$: 1 - perturbation on C , 2 - perturbation on L , 3 - perturbation on R , 4 - perturbation on Y_B , and 5 - perturbation on Y_G .

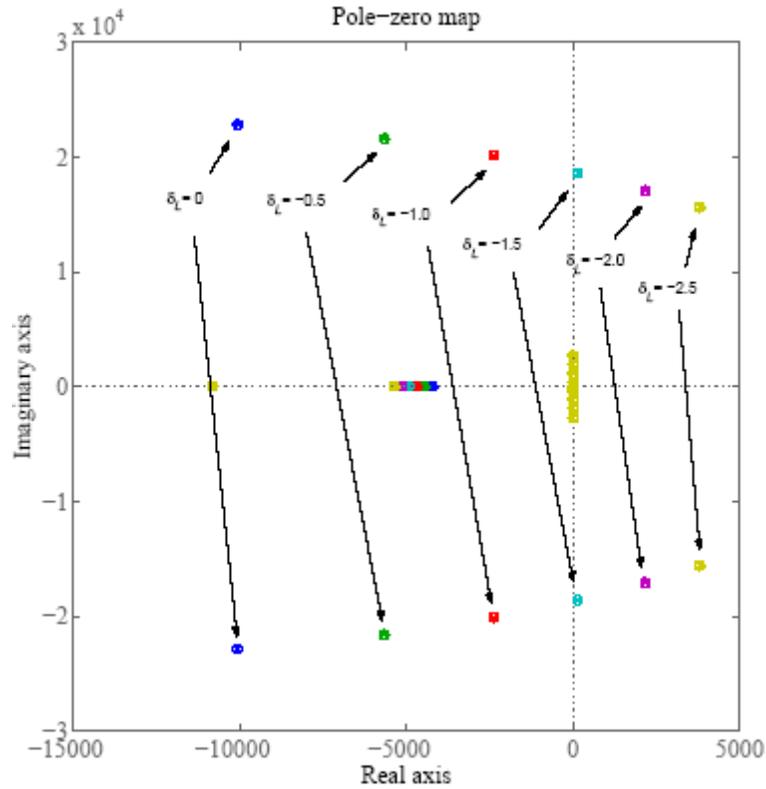


Figure 2.61: Closed-loop pole and zero map with $w_p = 0.05$ and various δ_L values, including both stable and unstable cases.

2.5 Summary of Chapter

In this chapter, a new control technique for a three-phase four-wire DG unit with split dc bus topology has been proposed. This technique is a combination of discrete-time sliding mode control (DSMC) and robust servomechanism control (RSC). The development of the control algorithm have been presented based on a one dimensional equivalent circuit model of the system in stationary $\alpha\beta 0$ reference frame and per-unit values.

A modified space vector PWM technique, i.e., the MSVPWM, has been proposed to perform three dimensional control on an $\alpha\beta 0$ basis. The pulse duration algorithm yielding higher priority on the non-zero-axis dimensions, i.e., α and β , under limited dc bus voltage has been presented. Simulation comparison has shown the advantage of this approach over the conventional sine wave PWM in the ABC reference frame. A series of analysis and studies have been performed on the proposed control technique, including the $L - C$ filter design issue, closed-current-loop and closed-voltage-loop responses, and time domain simulations and experiments under various load scenarios. All these analysis, simulations, and experiments have demonstrated the effectiveness of the proposed control solution.

The robust stability of the proposed solution in existence of linear load disturbances and parametric uncertainty has been verified structured singular value based method. It has been shown that the weight adjustment in the optimal control performance index provides a way of tuning the transient performance of the controller while maintaining stability robustness of the system under perturbations.

CHAPTER 3

POWER FLOW CONTROL OF A SINGLE DISTRIBUTED GENERATION UNIT

A distributed generation (DG) unit with distributed energy sources, such as fuel cells, micro-turbines, and photovoltaic devices, can be connected to utility grid, pumping power into the grid besides providing power to their local loads. In this research, the DG unit is interfaced with utility grid through a three-phase inverter. With inverter control, both real and reactive power pumped into the utility grid from the DG unit can be controlled. Real power flow P control determines whether the utility grid is taking power from the DG or supplying the local load together with the DG and how much this power should be. Reactive power flow control allows the DG unit to be used as static var compensation unit besides an energy source. With possible existence of nonlinear local load or harmonic distorted utility voltage, the line current is still desired to be sinusoidal and harmonic free. As reviewed in Section 1.2.5, the existing power control solutions have limitations, e.g., not suitable for DG applications with existence of local load, slow response, coupling between P and Q control, and sensitiveness of line current to harmonic distorted utility grid, etc. This chapter will present a DG unit real and reactive power control technique to a three-phase DG unit with three-phase three-wire topology and isolation transformer. This technique provides robust voltage regulation with harmonic elimination in island running mode. In grid connected mode, the control performs online power system identification estimating the Thevenin equivalent parameters of the utility grid and

uses the acquired information to conduct a feedforward power control together with the traditional integral control. A harmonic power controller will be proposed to handle possible harmonic distorted utility grid voltage. The proposed technique yields fast and less coupled real and reactive power flow control with line current conditioning capability even under nonlinear local load and harmonic corrupted grid voltage in grid-connected mode.

The power control technique proposed in this chapter is based on existing voltage and current control strategy of individual DG unit control in island model as described in Chapter 2, which combines discrete-time sliding mode current control and robust servomechanism voltage control but is developed for a three-wire topology. As reviewed in Section 1.2.2, the three-wire topology has advantage in reduced dimension of control plant and nonexistence of 0-axis current, both leading to ease of control. This is why this topology has been chosen to perform the grid-connected studies. The closed-loop P and Q control stability will be proved using Lyapunov direct method.

3.1 The Control System

The proposed control solution is developed for a grid-connected DG unit shown in Figure 3.1. The DG unit consists of a dc bus powered by any dc source or ac source with a rectifier, a voltage source inverter, an L - C filter stage, a Δ/Y_g type isolation transformer with secondary side filtering. The DG unit has a local load, linear or

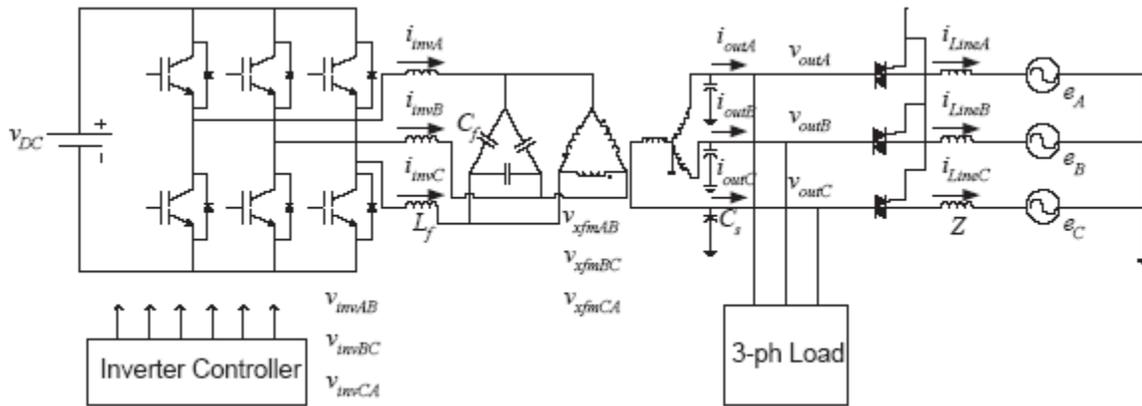


Figure 3.1: A grid-connected DG unit with local load.

nonlinear, and is connected to the utility grid through a three-phase static switch.

The utility grid is modelled by Thevenin's Theorem as an equivalent three-phase ac source with an equivalent internal impedance.

In island mode, the inverter conducts voltage control, where the load voltage V_{outABC} should track the given reference. The voltage control goal is strong voltage regulation, low static error in RMS, fast transient response, and low total harmonic distortion (THD). If the voltage of the utility main E_{ABC} is measured and used as the reference, V_{outABC} will be controlled to match E_{ABC} in magnitude and synchronized in phase angle.

In grid-connected mode, the DG unit conducts power control, where the output active power P and reactive power Q from the DG unit to the utility grid should be regulated to desired values P_{ref} and Q_{ref} . Both P_{ref} and Q_{ref} can be positive or

negative, which provides possibility for the DG unit to help with the energy production and stability enhancement of the power system or sustain power supply to local load when it exceeds the capacity of the DG. The control goal of power regulation is stability, low static error, and fast response with low coupling between P and Q . A conventional solution is integral control, forcing the DG unit to perform like a large generator with fast dynamics. This approach is a purely feedback control not requiring any plant knowledge. However, with the measurable variables and existing computing power of microprocessors, it is possible to acquire some useful plant information which can play instructive role in developing power controller. In practice, the utility grid voltage can often be harmonic distorted or the local load draws harmonic current from the unit. These situations make it necessary to have the power controller to handle the problem and yield low harmonic line power and sinusoidal line current. The power flow control strategy will be presented in details here in this chapter addresses these issue and provides solutions.

As stated above, the power flow control technique developed in this research is on the basis of a three-phase three-wire version of RSC plus DSMC voltage and current control solution similar to the technique discussed in Chapter 2. For the completeness and considering the difference between the three-wire and four-wire topology, the main attributes of the voltage and current controls will still be reviewed.

3.1.1 Voltage and current control

For high quality of V_{outABC} with strong regulation, low THD, and overload protection, a dual-loop voltage and current control structure is used as shown in Figure 3.2, where the inner loop is for current control and outer loop is for voltage control. A robust servomechanism controller (RSC) is used for voltage control and a discrete-time sliding mode controller (DSMC) is used for current control. The three-phase quantities are transformed from ABC reference frame into a stationary $\alpha\beta$ reference frame since there is no 0-axis current involved in control. The details of this approach have been given in [45, 70].

The DSMC is used in the current loop to limit the inverter current under overload condition because of the fast and overshoot-free response it provides. The RSC is adopted for voltage control due to its capability to perform zero steady state tracking error under unknown load and eliminate harmonics of any specified frequencies with guaranteed system stability. The theory behind the RSC is based on the solution of robust servomechanism problem (RSP) [24] where the internal model principle [33] and the optimal control theory for linear systems are combined. The internal model principle is applied in the DG voltages control by including the fundamental frequency mode and the frequency modes of the harmonics to be eliminated into the controller. The linear quadratic LQ optimal control theory of linear systems is combined in the RSC in order to guarantee the stability of the closed-loop system and providing arbitrary good transient response based on desired control priorities.

In a DG unit shown in Figure 3.1, most of the voltage harmonics, like the triplets (3rd, 9th, 15th, . . .) and even harmonics, are either non-existing or uncontrollable, or

negligible in values. Therefore, only the fundamental and the 5th and 7th harmonics are left for the control to handle. Since the overload protection is a strongly desired feature for inverter systems, a DSMC is included in the inner loop to limit the current under overload conditions. With the existence of the DSMC in the inner loop, the RSC in the outer loop are designed taking the dynamics of the DSMC into account, so that the stability and robustness of the overall control system is guaranteed.

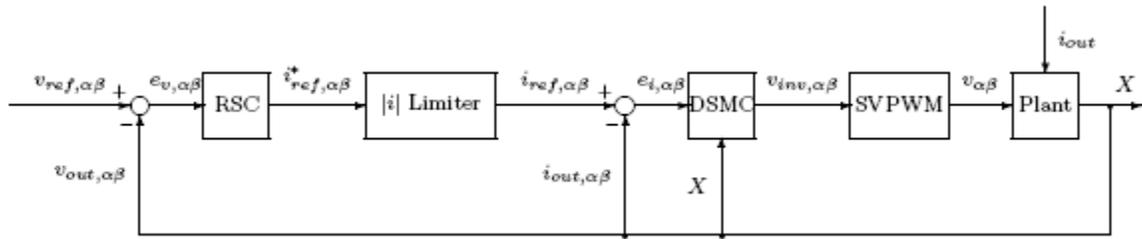


Figure 3.2: Control structure for island mode.

The discrete-time sliding mode current control

The circuit shown in Figure 3.1 is a linear system and can be modeled in state space. The current controller controls the inverter current, i.e., the inductor current.

The L - C filter can be represented in discrete time as

$$\begin{cases} X_i(k+1) = A_i X_i(k) + B_i v_{inv}(k) + E_i i_{out}(k) \\ y_i(k) = C_i X_i(k) \end{cases} \quad (3.1)$$

where $X_i(k) = [v_{x_{fm}}^T(k) \quad i_{inv}^T(k)]^T$, v_{inv} , and load disturbance i_{out} are all represented in $\alpha\beta$ reference frame. Given inverter current command $i_{ref}(k)$, the DSMC equivalent control law is

$$v_{inv,eq}(k) = (C_i B_i)^{-1} [i_{ref}(k) - C_i A_i X_i(k) - C_i E_i i_{out}(k)]. \quad (3.2)$$

With inverter control voltage limit v_{max} determined by the dc bus voltage and PWM technique, the actual control voltage becomes

$$v_{inv} = \begin{cases} v_{inv,eq} & \text{if } \|v_{inv,eq}\| \leq v_{max} \\ \frac{v_{max}}{\|v_{inv,eq}\|} v_{inv,eq} & \text{otherwise.} \end{cases} \quad (3.3)$$

The robust servomechanism voltage control

The voltage controller generates current command i_{ref} for the current controller.

For the system shown in Figure 3.1, considering the dynamics of the DSMC current controller, the overall state space model is

$$X(k+1) = AX(k) + Bi_{ref}(k) + Ei_{out}(k), \quad (3.4)$$

where $X(k) = [v_{xfm}^T(k) \quad i_{inv}^T(k) \quad v_{out}^T(k) \quad i_{xfm}^T(k)]^T$, with all element vectors represented under $\alpha\beta$ reference frame, and i_{xfm} is the transformer secondary current and will be replaced by i_{out} feedback in the control due to the negligible difference.

An RSC is a combination of a stabilizing compensator and a servo compensator.

The stabilizing compensator is the state feedback of (3.4) times a gain K_0 . The servo compensator is a second order filter represented by

$$\eta(k+1) = A_s \eta(k) + B_s e_v(k), \quad (3.5)$$

where η is the state vector, $e_v(k)$ is the instantaneous voltage regulation error vector, and matrix A_s has poles at specified frequencies to be cancelled from $e_v(k)$, e.g., the fundamental, 5th and 7th harmonics. All quantities are in the $\alpha\beta$ reference frame.

The current command for the current controller can be obtained as

$$i_{ref}(k) = K_0 X(k) + K_1 \eta(k), \quad (3.6)$$

where the gains K_0 and K_1 are obtained by solving the linear quadratic optimization problem of the augmented system of X and η . Therefore, run-time gain calculation is not necessary.

3.1.2 Real and reactive power control problems

Since the DG unit uses a voltage source inverter with a strong voltage control, its output active and reactive power are determined by the unit's output voltage, including magnitude and phase angle, as stated in

$$P = \frac{V_{out} E}{X} \sin \delta, \quad (3.7)$$

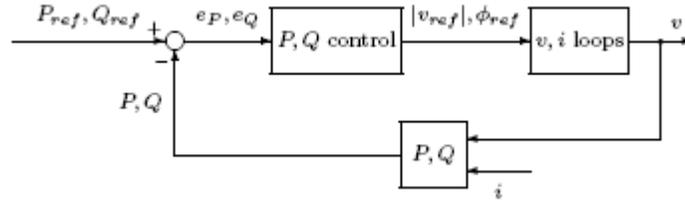


Figure 3.3: Control structure for grid-connected mode.

$$Q = \frac{V_{out}^2 - V_{out}E \cos \delta}{X}, \quad (3.8)$$

where E is the equivalent main voltage, X is the equivalent line reactance where the resistance is ignored, and δ is the power angle. Since the DG unit output voltage control already exists, the task of the power controller is to generate voltage command for the voltage controller based on the desired power values P_{ref} and Q_{ref} and actual values P and Q as illustrated in Figure 3.3.

It is apparent that the desired DG output voltage V and the power angle δ can be calculated from (3.7) and (3.8) given desired P and Q values and system parameter X . If this is true, the power control problem is solved. However, in practical systems, the above approach is not feasible based on the existing techniques due to the following three reasons:

- Equations 3.7 and 3.8 show that the power system parameters, both X and E , need to be known to solve the equations, which is difficult based on the existing

approaches. Practically, the value of X may change due to the operation of the power system.

- Both P and Q are sensitive to variation of X since it appears in the denominators and especially when X is small. The more the difference between the power system capacity and the DG's power rating, the less the value of X could be.
- Both the equations are nonlinear which are difficult to solve in real time which prevents the idea being implemented in practice.

Therefore, power control solutions requiring knowledge of X have not been practically used and people tends to search for other solutions, e.g., the integral control.

3.1.3 The conventional integral control

It can be observed from (3.7) and (3.8) that both P and Q will be affected by only adjusting one of V and δ , which is so called coupling between P and Q . However, variations of V and δ have different levels of impact on P and Q as described in the following partial derivatives -

$$\frac{\partial P}{\partial \delta} = \frac{V_{out}E}{X} \cos \delta, \quad (3.9)$$

$$\frac{\partial P}{\partial V_{out}} = \frac{E}{X} \sin \delta, \quad (3.10)$$

$$\frac{\partial Q}{\partial \delta} = \frac{V_{out} E}{X} \sin \delta, \quad (3.11)$$

$$\frac{\partial Q}{\partial V_{out}} = \frac{2V_{out} - E \cos \delta}{X}. \quad (3.12)$$

These partial derivatives are plotted in three-dimensional manner as shown in Figure 3.4 to illustrate the significance of the impacts of V and δ variations on P and Q under different V and δ values. The values of V , E , and X are normalized in Figure 3.4 for comparison purposes.

It can be observed from Figure 3.4 that, when $|\delta|$ is small and V is close to 1 which is true for large capacity power systems, $\frac{\partial P}{\partial \delta}$ is close to 1 and $\frac{\partial P}{\partial V_{out}}$ is close to

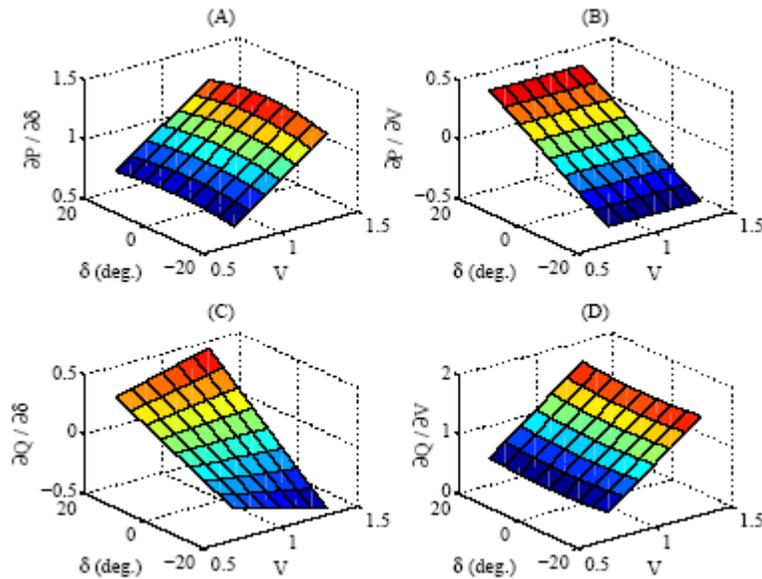


Figure 3.4: Sensitivity of P and Q to V and δ variations with normalized V , E , and

X: (A) $\frac{\partial P}{\partial \delta}$, (B) $\frac{\partial P}{\partial V_{out}}$, (C) $\frac{\partial Q}{\partial \delta}$, (D) $\frac{\partial Q}{\partial V_{out}}$.

0 and reversely, $\frac{\partial Q}{\partial \delta}$ is close to 0 and $\frac{\partial Q}{\partial V_{out}}$ is close to 1. This fact indicates that P is more sensitive to δ and Q is more sensitive to V_{out} especially when the DG unit is connected to a large capacity system where the power angle δ is usually small. The different levels of sensitivity of P and Q to δ and V_{out} provide a chance to control P and Q relatively independently, not completely independently though.

Based on the above analysis, an integral approach to conduct the power flow control can be developed to control P by adjusting δ and control Q by adjusting V_{out} . If the phase angle associated to the system voltage E is assumed to be 0, $\delta = \phi$ holds, where ϕ is the phase angle associated to V_{out} . The voltage and phase angle references can be generated as

$$\phi_{ref} = \int [K_P(P_{ref} - P) + \omega_n] dt + \phi_0, \quad (3.13)$$

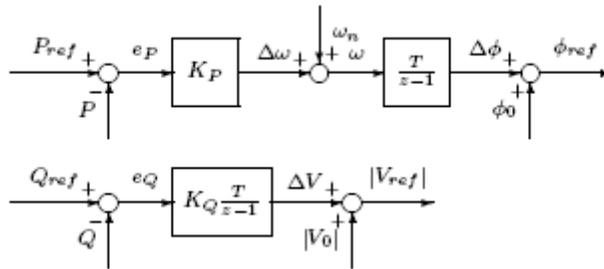


Figure 3.5: The power regulator for P and Q.

$$V_{ref} = \int K_Q(Q_{ref} - Q)dt + V_0, \quad (3.14)$$

where $\omega_n = 2\pi \times 60 \text{rad./sec.}$ is the system nominal angular frequency, ϕ_0 and V_0 are the initial voltage and phase angle at the moment that the DG unit is connected to the grid from island running mode. The proposed power controller is illustrated in Figure 3.5 where the integration is implemented in discrete-time.

3.1.4 The stability issue

In the integral control, P and Q controls are decoupled under steady state due to the integration of the errors. However, in the transient, the P Q coupling cannot be eliminated. Moreover, both P and Q are nonlinear functions of V_{out} and ϕ , which increases the complexity to analyze the system behavior. Due to the coupling issue and the nonlinearity, the stability of the power control must be investigated.

Due to the strong regulation of the DG output voltage V_{out} and its phase angle ϕ , the dynamics of the voltage control loop can be simplified into a first-order system with a transfer function representation

$$\phi(s) = \frac{a_\phi}{s + a_\phi} \phi_{ref}(s), \quad (3.15)$$

$$V_{out}(s) = \frac{a_V}{s + a_V} V_{ref}(s), \quad (3.16)$$

where a_ϕ and a_V are the inverses of the time constants of ϕ and V_{out} dynamics. Since the scope of this discussion is about power control stability of a DG unit connected to a large power system, whose time constant is in a range of seconds and much greater than that of the voltage tracking response measured in a range of 0.01 sec. or less, the DG power response has the room to be much slower than the voltage tracking and still fast compared to the power system. Therefore, it is reasonable to ignore the dynamics of the voltage tracking when power control is concerned, i.e. $a_\phi \rightarrow \infty$, $a_V \rightarrow \infty$, and $\phi \rightarrow \phi_{ref}$, $V_{out} \rightarrow V_{ref}$.

At the moment that the DG is switched from island mode to grid-connected mode, V_0 and ϕ_0 should match E and ϕ_E , where ϕ_E denotes the phase angle associated to E . Therefore, (3.13) and (3.14) can be rewritten into

$$\delta = \int [K_P(P_{ref} - P) + \omega_n] dt, \quad (3.17)$$

$$\Delta V = \int K_Q(Q_{ref} - Q) dt \quad (3.18)$$

where $\delta = \phi_{ref} - \phi_E$ and $\Delta V = V_{ref} - E$. Assuming large capacity power system with small power angle δ , it is reasonable to have $\sin \delta \approx \delta$ and $\cos \delta \approx 1$. Equations (3.17) and (3.18) can be rewritten in differential format

$$\dot{\delta} = K_P(P_{ref} - \frac{EV_{out}}{X}\delta), \quad (3.19)$$

$$\Delta\dot{V} = K_Q(Q_{ref} - \frac{V_{out}}{X}\Delta V) \quad (3.20)$$

Since the dynamics of DG voltage tracking is ignored, the stability of the power loop can be evaluated using Lyapunov's direct method where there is no external excitation, i.e., $P_{ref}=0$ and $Q_{ref}=0$.

A Lyapunov function can be defined as

$$\xi(\Delta V, \delta) = \frac{1}{2}\Delta V^2 + \frac{1}{2}\delta^2, \quad (3.21)$$

where $\xi > 0$ holds unless $\Delta V=0$ and $\delta=0$. The derivative of the above function is

$$\begin{aligned} \xi(\Delta V, \delta) &= \Delta V \cdot \Delta\dot{V} + \delta \cdot \dot{\delta} \\ &= -K_Q \frac{V_{out}}{X} \Delta V^2 - K_P \frac{EV_{out}}{X} \delta^2. \end{aligned} \quad (3.22)$$

From (3.22), it can be observed that $\dot{\xi}(\Delta V, \delta) < 0$ holds when $\Delta V \neq 0$ or $\delta \neq 0$, given positive values of K_P , K_Q , E , V_{out} , and X . Therefore, the proposed power control loop is asymptotically stable at vicinity of the equilibrium point $\Delta V=0$ and $\delta=0$.

3.1.5 Newton-Raphson parameter estimation and feedforward control

Newton-Raphson Parameter Identification

The power flow control plant is governed by the two nonlinear equations given in Equations 3.7 and 3.8. Recall the initiative idea mentioned in Section 3.1.2 that direct solution of V_{ref} and δ_{ref} is desired assuming that the other parameters are known.

This thought has not become practice only because it lacks means of implementation. The thought itself is very reasonable and inspiring. In these two equations, under conventional integral control, V , δ , P , and Q are all known. If the nonlinear equations can be solved for E and X , the Thevenin equivalent circuit parameters are obtained and can be used to improve the power flow control performance. Direct analytical solution of these equations are messy due to the nonlinearity. In this research, a real time achievable numerical solution based on Newton-Raphson Method has been developed. The algorithm is presented as follows.

To avoid messy mathematical derivation, it is reasonable to replace the equations from reactance model based to susceptance model based, i.e., use system susceptance B to take the place of $1/X$. This change does not affect the goal of identifying the

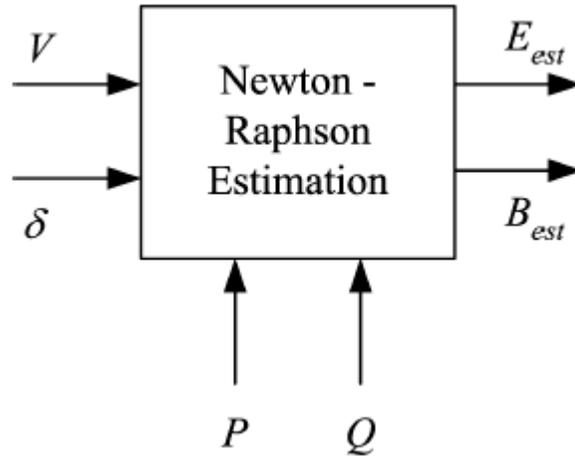


Figure 3.6: A Newton-Raphson Method based nonlinear parameter estimator.

system parameters to get achieved and meantime simplifies the problem and leads to a Newton-Raphson parameter estimator as depicted in Figure 3.6.

Rewrite the equations into the form of

$$\begin{cases} f(E, B) = BVE \sin \delta - P = 0, \\ g(E, B) = BV^2 - BVE \cos \delta - Q = 0. \end{cases} \quad (3.23)$$

The Jacobian is then obtained as

$$J_{est} = \begin{bmatrix} \frac{\partial f}{\partial E} & \frac{\partial f}{\partial B} \\ \frac{\partial g}{\partial E} & \frac{\partial g}{\partial B} \end{bmatrix}, \quad (3.24)$$

where

$$\frac{\partial f}{\partial E} = BV \sin \delta,$$

$$\frac{\partial f}{\partial B} = VE \sin \delta,$$

$$\frac{\partial g}{\partial E} = -BV \cos \delta,$$

and

$$\frac{\partial g}{\partial B} = V^2 - VE \cos \delta.$$

Given initial values E_0 and B_0 , the iterations can be conducted. Solve the linearized equation

$$J_{est} \begin{bmatrix} \Delta E_k \\ \Delta B_k \end{bmatrix} = \begin{bmatrix} f(E_k, B_k) \\ g(E_k, B_k) \end{bmatrix} \quad (3.25)$$

for ΔE_k and ΔB_k , and

$$E_{k+1} = E_k - \Delta E_k, \quad (3.26)$$

$$B_{k+1} = B_k - \Delta B_k. \quad (3.27)$$

Newton-Raphson is known for fast convergence. However, if the nonlinear equation has saddles or multiple roots, the algorithm may not converge to the desired root. Therefore, the convergence condition needs to be checked before this approach

can be practiced.

It can be observed from Equation 3.24 that all four Jacobian elements hold monotonicity with given parameters. Therefore, no saddles or multiple roots exist and the iteration converges to the right solution.

Due to the fast convergence, three to five iterations can yield solutions close enough to the true ones. Each control period can run one or multiple iterations depending on the load of control tasks. Plus no derivatives need to be taken in generating the Jacobian and the linear equation solution can be obtained using precalculated formula to save time, the proposed parameter estimation technique can be implemented on microprocessor controllers in real time.

Newton-Raphson feedforward control

Given the real-time implementation of Newton-Raphson parameter estimation, the Thevenin equivalent circuit parameters of the power system can be approximately obtained. The acquired information can be used to perform P and Q feedforward

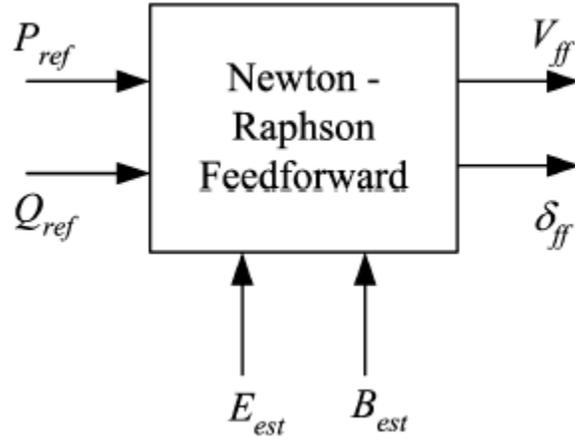


Figure 3.7: A Newton-Raphson Method based nonlinear feedforward controller.

control using the similar technique - with knowledge of the parameters E , B , from estimation, and P_{ref} and Q_{ref} , from desired power flow requirement, the voltage command can be solved also using Newton-Raphson Method. This technique makes the idea of direct solution of V_{ref} and δ_{ref} implementable in real time and results in a P and Q feedforward controller as depicted in Figure 3.7. The algorithm can be derived as follows.

Rewrite the equations into the form of

$$\begin{cases} f(V_{ref}, \delta_{ref}) = BV_{ref}E \sin \delta_{ref} - P_{ref} = 0, \\ g(V_{ref}, \delta_{ref}) = BV_{ref}^2 - BV_{ref}E \cos \delta_{ref} - Q_{ref} = 0. \end{cases} \quad (3.28)$$

The Jacobian is then obtained as

$$J_{ff} = \begin{bmatrix} \frac{\partial f}{\partial V_{ref}} & \frac{\partial f}{\partial \delta_{ref}} \\ \frac{\partial g}{\partial V_{ref}} & \frac{\partial g}{\partial \delta_{ref}} \end{bmatrix}, \quad (3.29)$$

where

$$\begin{aligned} \frac{\partial f}{\partial V_{ref}} &= BE \sin \delta_{ref}, \\ \frac{\partial f}{\partial \delta_{ref}} &= BV_{ref}E \cos \delta_{ref}, \\ \frac{\partial g}{\partial V_{ref}} &= 2BV_{ref} - BE \cos \delta_{ref}, \end{aligned}$$

and

$$\frac{\partial g}{\partial \delta_{ref}} = BV_{ref}E \sin \delta_{ref}.$$

Given initial values $V_{ref,0}$ and $\delta_{ref,0}$, the iterations can be conducted. Solve the linearized equation

(3.30)

for $\Delta V_{ref,k}$ and $\Delta \delta_{ref,k}$, and

$$V_{ref,k+1} = V_{ref,k} - \Delta V_{ref,k}, \quad (3.31)$$

$$\delta_{ref,k+1} = \delta_{ref,k} - \Delta \delta_{ref,k}. \quad (3.32)$$

Similarly, the convergence condition needs to be checked before this approach can

be practiced.

It can be observed from Equation 3.29 that all four Jacobian elements hold monotonicity with given parameters. Therefore, no saddles or multiple roots exist and the iteration converges to the right solution.

Also similar to the parameter estimator proposed above, due to the fast convergence of Newton-Raphson Method, three to five iterations can yield solutions close enough to the true ones. Each control period can run one or multiple iterations depending on the load of control tasks. Plus no derivatives need to be taken in generating the Jacobian and the linear equation solution can be obtained using pre-calculated formula to save time, the proposed parameter estimation technique can be implemented on microprocessor controllers in real time.

Combining the proposed Newton-Raphson based feedforward controller with the conventional integral control, it can be stated that even though small convergence

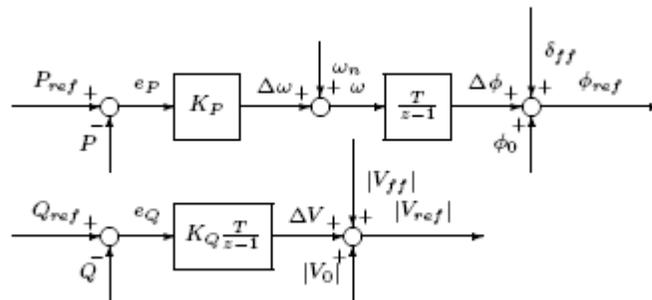


Figure 3.8: Power regulator combining integral control and feedforward.

errors still exist after a small number of iterations, the resulted V_{ref} and δ_{ref} are close

to the steady state value and stability of the integral control can be maintained due to the global stability of the technique proved in Section 3.1.4. The overall power regulator is shown in Figure 3.8.

3.1.6 Harmonic power control

A harmonic power controller has been proposed to be applied together with the proposed fundamental power flow technique to handle harmonic distorted grid line voltage and prevent harmonic power from flowing between the DG unit and the utility grid. The block diagram of the i -th harmonic power controller is shown in Figure 3.9. This harmonic controller has the same algorithm of the conventional integral power control of the fundamental power. Specially, $P_{ref,i}$ and $Q_{ref,i}$ are both zero for desired zero P_i and Q_i . The nominal frequency and phase angle of the i -th harmonic, $\omega_{0,i}$ and $\phi_{0,i}$, are obtained from a standard phase-locked loop (PLL) as given in Figure 3.10. The nominal voltage of the harmonic $|V_{0,i}|$ is calculated by a harmonic magnitude estimation algorithm as shown in Figure. 3.11.

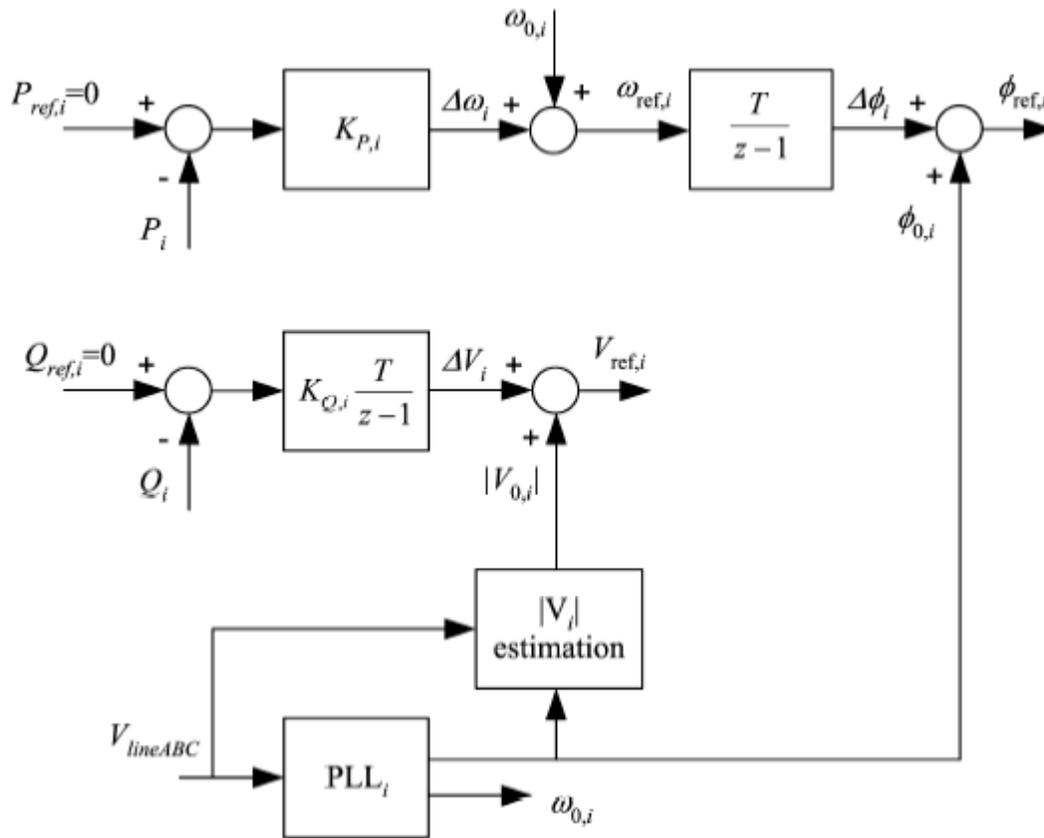
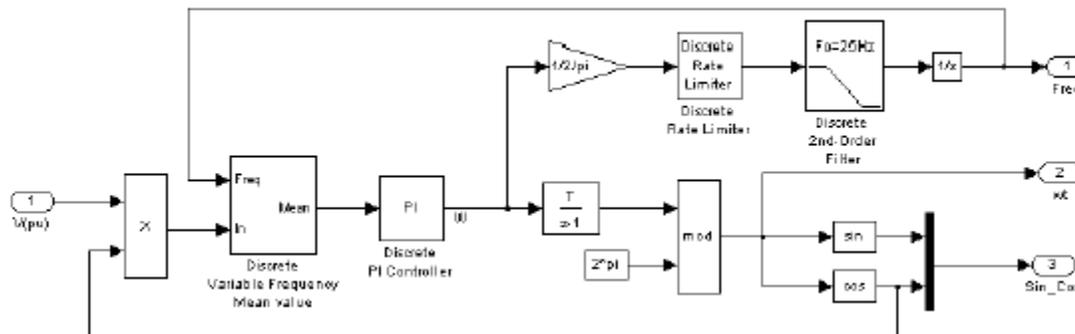


Figure 3.9: Control block diagram of harmonic compensation under harmonic distorted grid voltage.

Discrete 1-phase PLL

Pierre Giroux, Gilbert Sybille
Power System Laboratory, IREQ
Hydro-Quebec



Note: $\sin(a) * \cos(b) = 1/2 * \sin(a+b) + 1/2 * \sin(a-b)$

Figure 3.10: Simulink[®] implementation of a PLL by Hydro-Quebec[®].

Discrete PLL Driven Fundamental Value

Pierre Groux, Gilbert Sybille
 Power System Simulation Laboratory
 IREQ, Hydro-Quebec

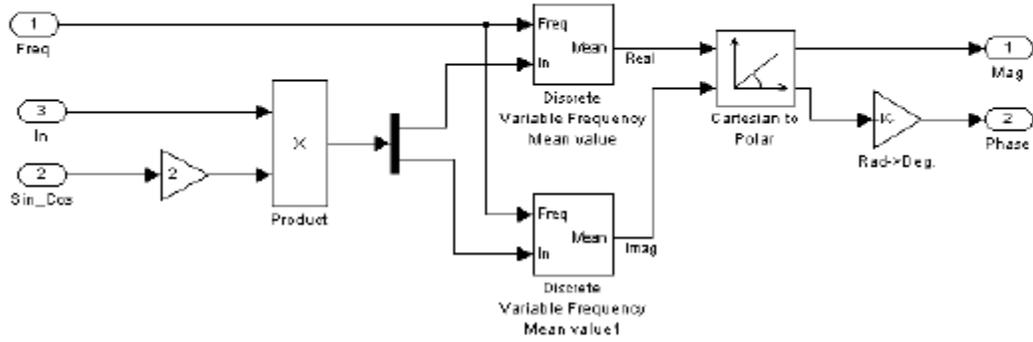


Figure 3.11: Simulink[®] implementation of a harmonic magnitude estimator by Hydro-Quebec[®].

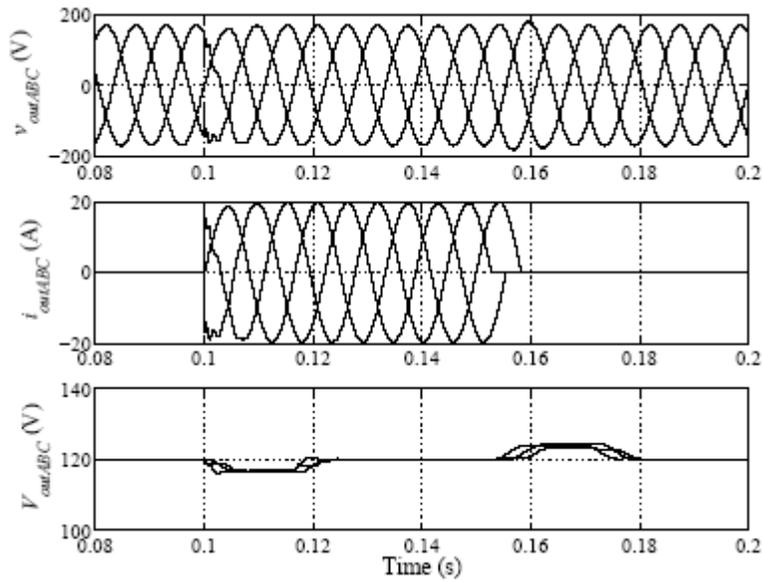


Figure 3.12: Transient response of V_{out} in instantaneous and RMS at step load increase from 0 to 100% and decrease from 100% to 0.

3.2 Simulation Results

Simulations have been conducted on a 5 kVA DG unit with a topology shown in Figure 3.1 connected to a 120V line-to-neutral power system with an equivalent reactance 0.1Ω under a number of different scenarios as shown below.

3.2.1 In island mode

Under island mode, a 100% step load increase is applied to the DG output terminal. After steady state is reached, the load steps back down to zero. The voltage response under these transients are shown in Figure 3.12.

Simulation data shows that the voltage tracking error under steady state is nearly zero and the THD is 0.4%. It can be observed from Figure 3.12 that the load disturbance has little impact on V_{out} waveform and the RMS transients last for only 0.02 second with 3% or so peak variations.

Recall that similar results obtained from the four-wire split dc bus topology have already been discussed in Section 2.3.2.

3.2.2 In grid-connected mode

Under grid-connected mode, P and Q output to the utility grid need to be controlled for system stabilizing, compensation, or handling local load disturbances. Figure 3.13 illustrates the P and Q regulation under various step references under nonlinear local load without the Newton-Raphson parameter estimation and feedforward. Figure 3.14 illustrates that with the Newton-Raphson parameter estimation and feedforward. It can be observed from these figures that under the power command step changes, transient coupling between P and Q cannot be removed while the steady state decoupling can be achieved. By comparing these two figures, it is obvious that the one with the Newton-Raphson parameter estimation and feedforward yields significant less transient coupling and overshoot, and therefore more effective.

When nonlinear local load exists, the line current i_{kine} is supposed not be affected with the proposed control. Figure 3.15 exhibits the current waveforms at three different locations of the system including the line current i_{line} , the unit output current i_{out} , and the inverter current i_{inv} . The waveforms show that all current harmonics are taken by the DG unit and the system line current is clean. This is because the

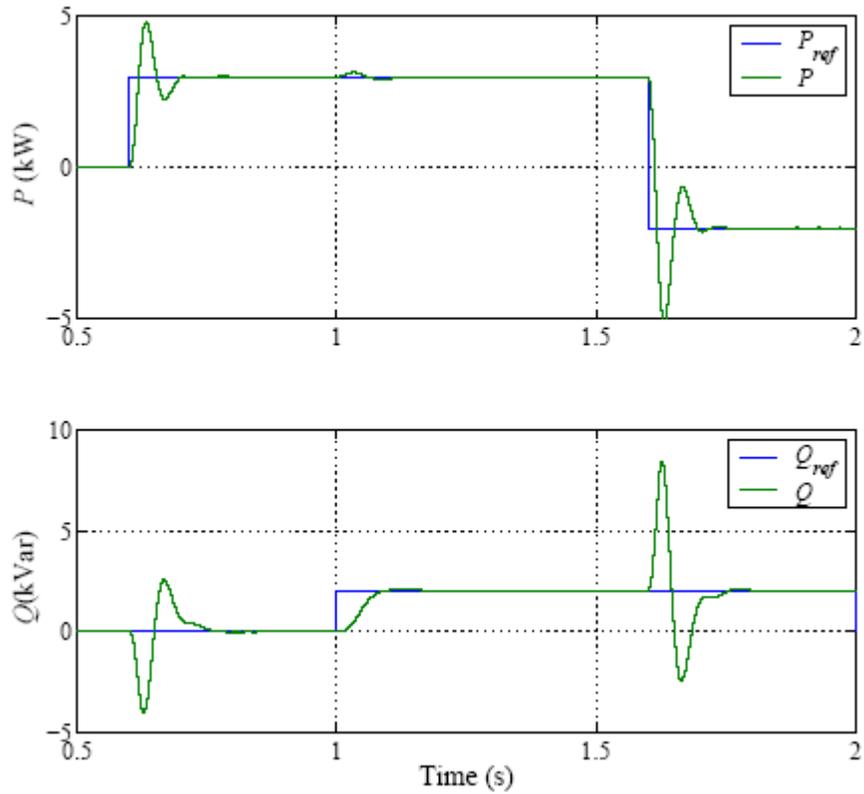


Figure 3.13: P , Q regulation under nonlinear local load without feedforward.

voltage control loop eliminates the voltage harmonics at the DG output which avoids harmonic current flow to or from the utility grid.

3.2.3 Line current conditioning under harmonic distorted grid

voltage

The effectiveness of the harmonic power controller have been demonstrated by comparing two simulation scenarios where one has while the other does not have the harmonic power controller under a 5th harmonic distorted utility grid voltage. The waveforms under the scenario where there is no harmonic power control is shown

in Figure 3.16 while the other one, where there is the harmonic power controller, is shown in Figure 3.17.

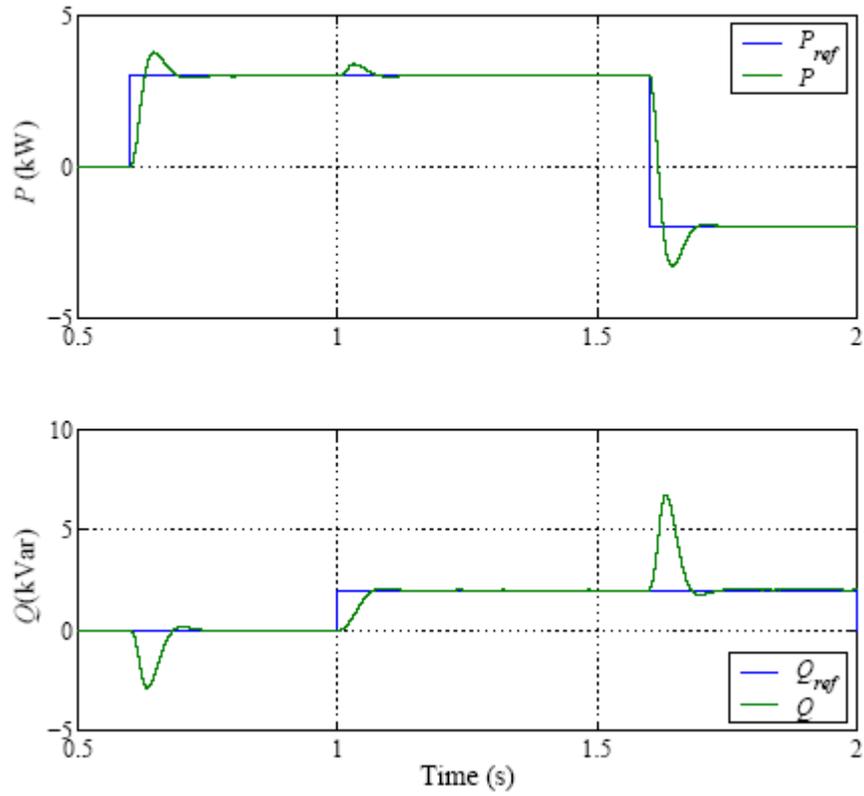


Figure 3.14: P , Q regulation under nonlinear local load with feedforward.

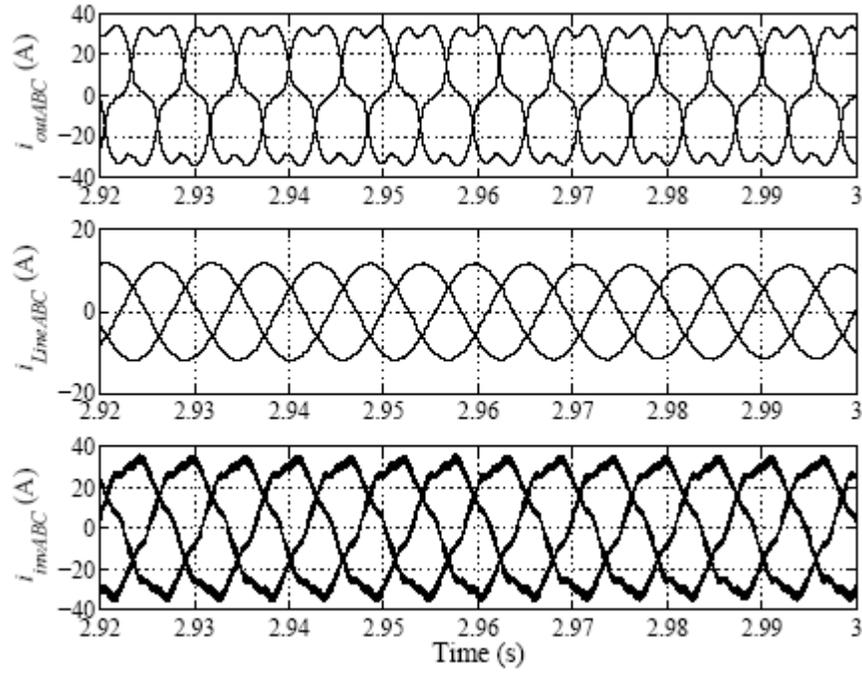


Figure 3.15: Current waveforms of DG unit output current i_{out} , system line current i_{line} , and inverter current i_{inv} under nonlinear local load.

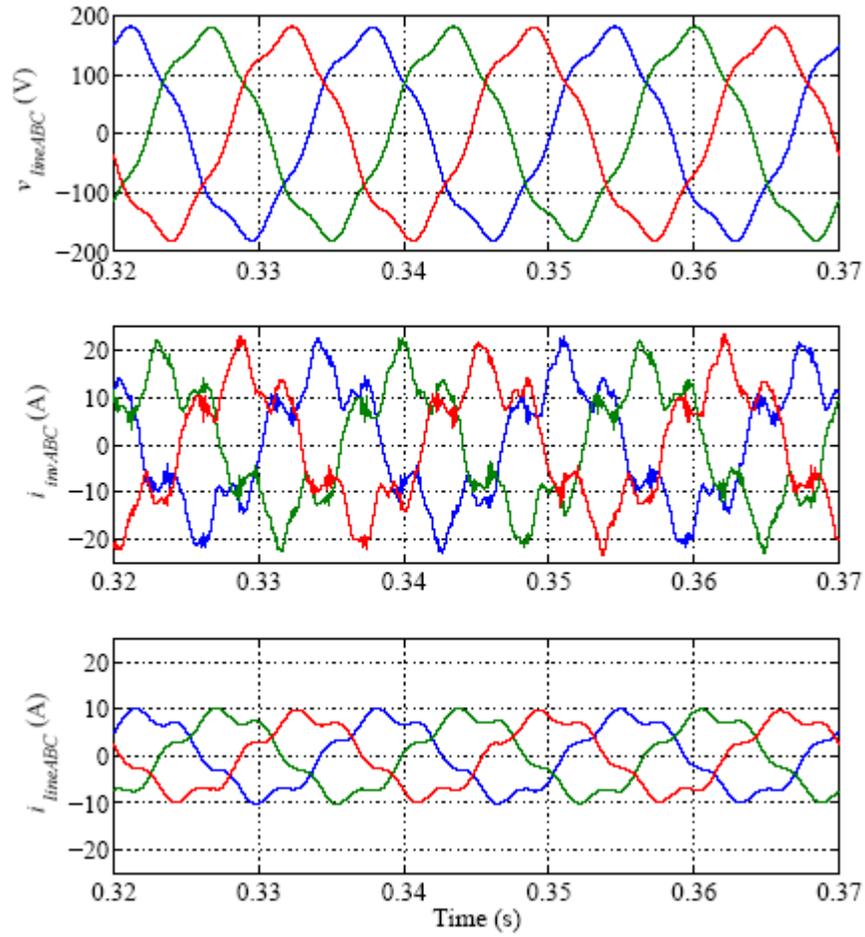


Figure 3.16: $v_{lineABC}$, i_{invABC} , and $i_{lineABC}$ under the 5th harmonic distorted grid voltage without the 5th harmonic power control.

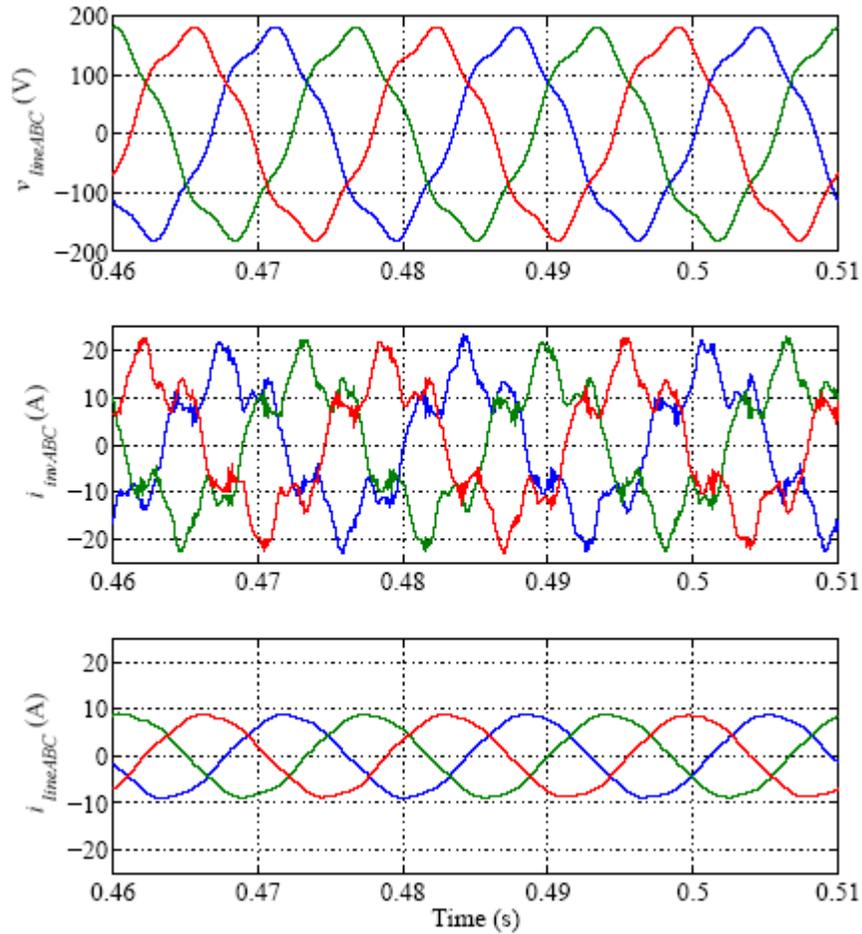


Figure 3.17: $v_{lineABC}$, i_{invABC} , and $i_{lineABC}$ under the 5th harmonic distorted grid voltage with the 5th harmonic power control.

It is clearly seen from the trace 3 of the two figures that the result with the harmonic power control yields much less line current harmonics which has verified the importance of this technique under harmonic corrupted utility grid voltage.

3.3 Experimental Results

Power flow control experiments have been conducted on a 5 kVA grid-connectable

inverter unit, where the main parameters are: dc bus voltage 540 V, output filter inductance 1.8 mH, filter capacitance 55 μ F, Δ/Y isolation transformer equivalent leakage reactance 5%, transformer secondary filter capacitor 5 μ F. SEMIKRON[®] IGBT modules SKM 50GB 123D are used in the inverter. A Texas Instruments[®] TMS320LF2407A digital signal processor (DSP) with a Spectrum Digital[®] evaluation module (EVM) have been used as the digital controller. A Omron[®] relay controlled contactor is used to operate the grid connection.

The Newton-Raphson parameter estimation and feedforward control have been developed and included in the power control code on the DSP, where the estimated parameters are used in the feedforward. The power control performance of the real-time implementation of the technique has been demonstrated by Figure 3.19 better than the case where the technique is not used as shown in Figure 3.18 in that the former is much faster, even though the latter has a slightly smaller but also slower transient coupling between P and Q .

The single-phase current transients under the above two scenarios have been presented and compared in Figure 3.20, where the envelopes of the two current waveforms can be clearly seen and the bottom trace which includes the feedforward yields better performance.

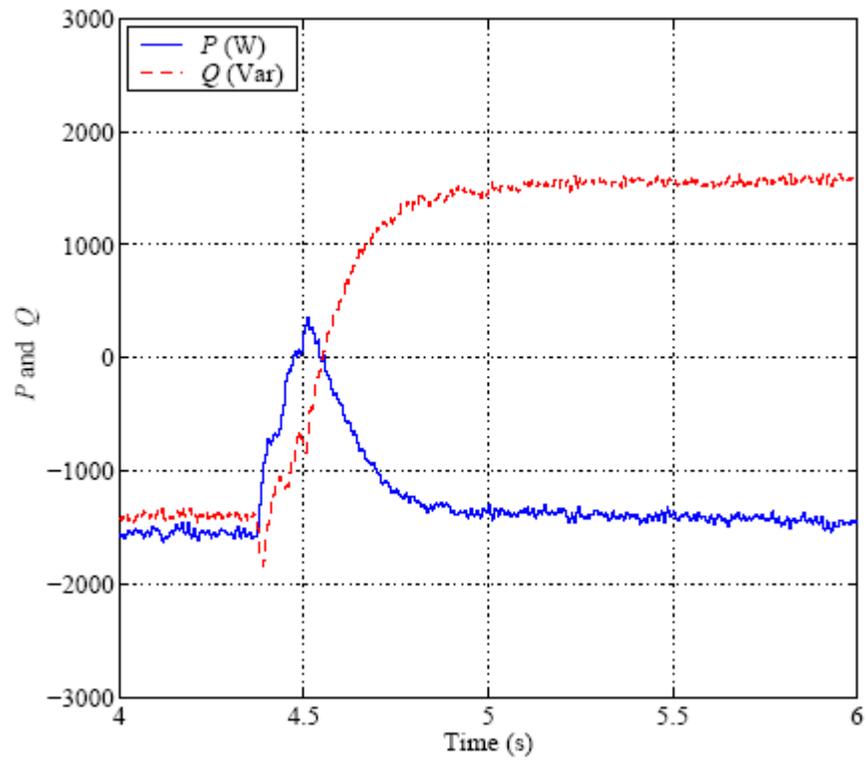


Figure 3.18: Experimental P , Q regulation transients without feedforward.

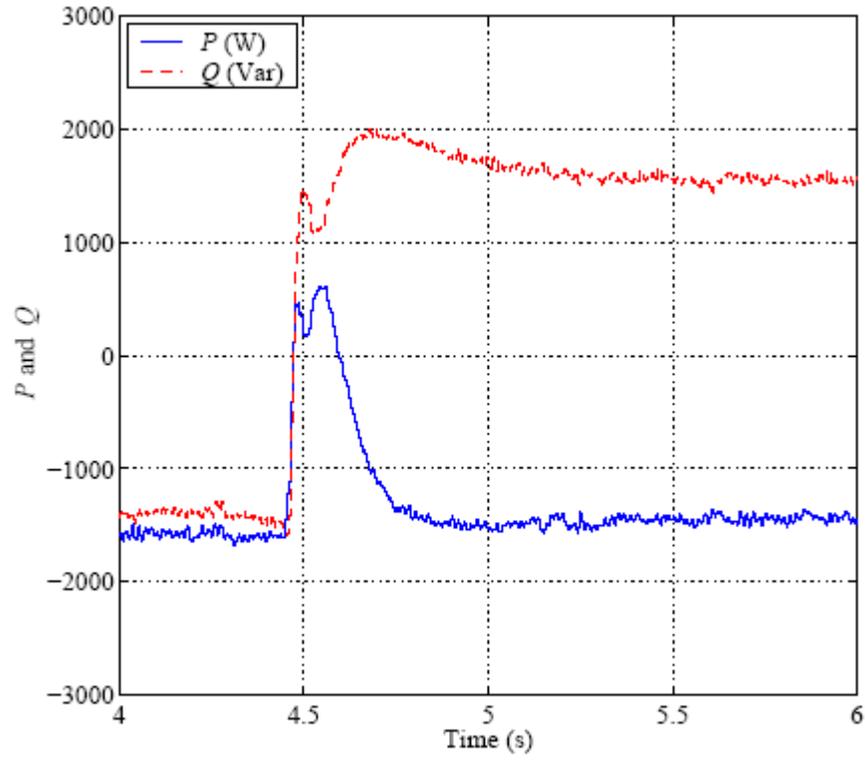


Figure 3.19: Experimental P , Q regulation transients with feedforward.

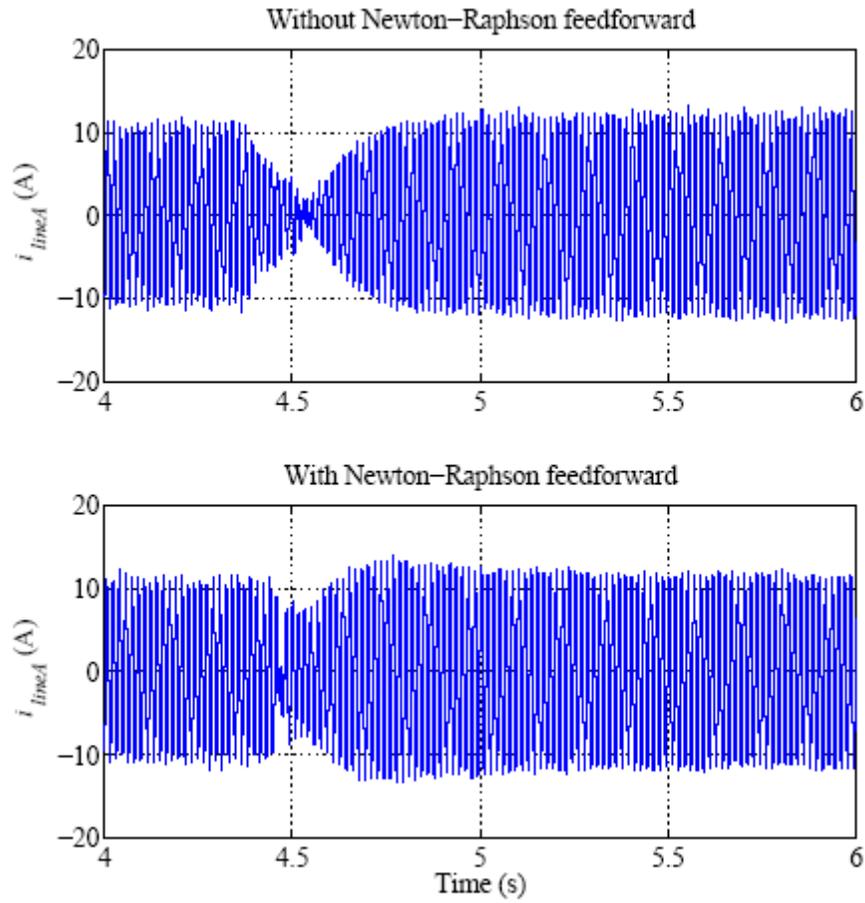


Figure 3.20: Experimental i_a transients without feedforward (the top trace) and with feedforward (the bottom trace).

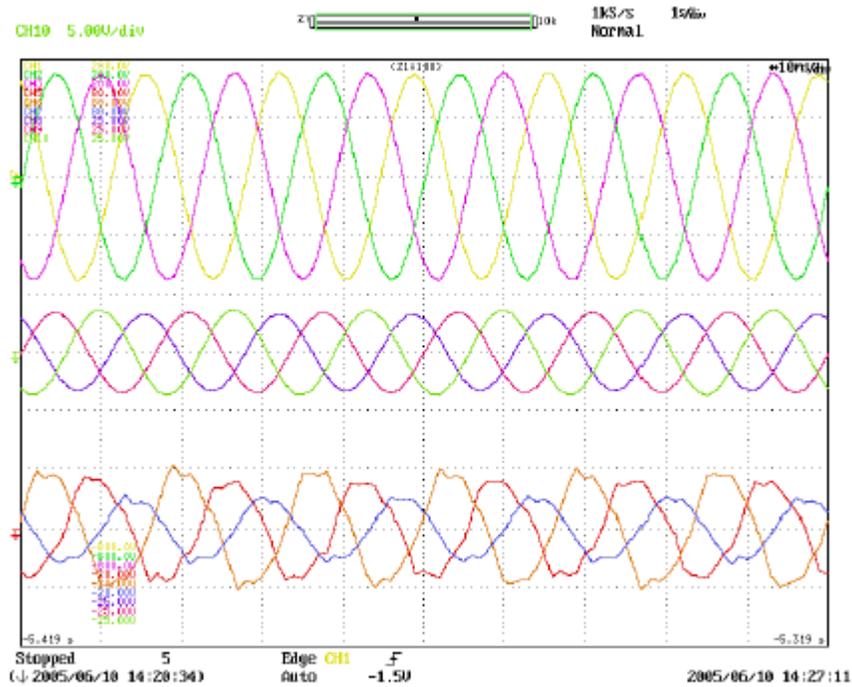


Figure 3.21: $v_{lineABC}$ (top), $i_{loadABC}$ (middle), and $i_{lineABC}$ (bottom) under harmonic distorted grid voltage: $P = -1500$ W and $Q = -1500$ W.

Since the harmonic power controller has not been implemented in experiments, the line current waveforms shown in Figures 3.21 and 3.22 contain significant amount of harmonic current. This is due to, first, of course, the harmonic distorted utility grid voltage, and secondly, the fundamental output voltage of the DG unit has been mostly cancelled or evened out by that of the grid voltage, which makes the harmonic voltage components in the grid voltage take a more significant row in generating the line current. This explains why the line current contains much more harmonics compared to the load current.

3.4 Summary of Chapter

This chapter has presented a power flow control approach for a single distributed generation unit connected to utility grid with a local load. The proposed control

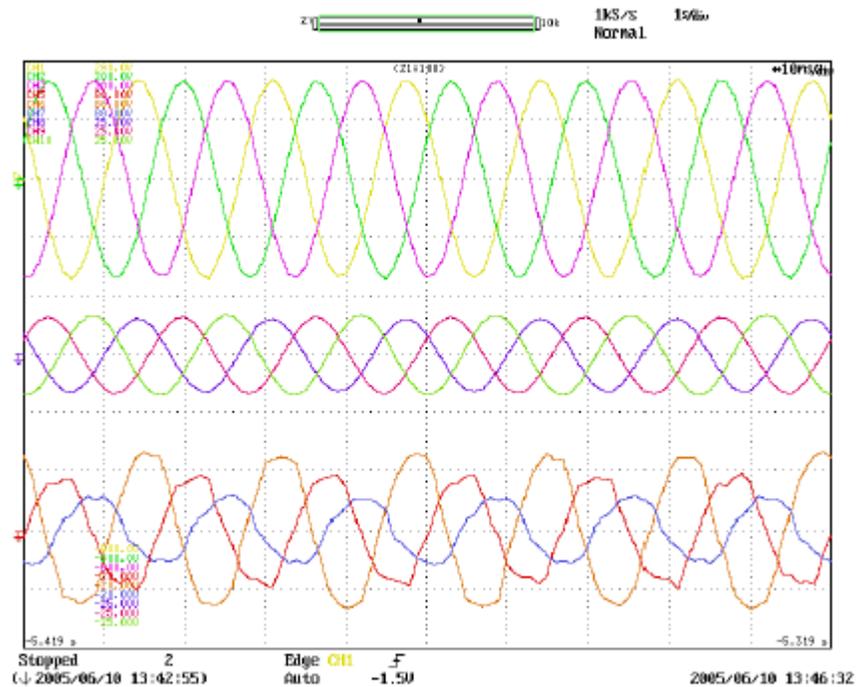


Figure 3.22: $v_{lineABC}$ (top), $i_{loadABC}$ (middle), and $i_{lineABC}$ (bottom) under harmonic distorted grid voltage: $P = -1500$ W and $Q = 1500$ W.

technique is based on a robust servomechanism voltage controller and a discrete-time sliding mode current controller designed for a three-phase three-wire inverter topology with isolation transformer. In order to obtain the parameters of the utility grid and use the information to generate feedforward control of power flow, a Newton-Raphson Method based parameter estimation and feedforwrd control technique have

been developed and combined with traditional integral power control. The stability of the power control loop has been proved using Lyapunov direct method. A harmonic power control technique based on PLL have been proposed to handle harmonic distorted utility grid voltage and yield harmonic free line current. Both simulation and experimental results under various scenarios have demonstrated the effectiveness of the proposed technique in power regulation and line current conditioning.

CHAPTER 4

A PWM RECTIFIER CONTROL TECHNIQUE FOR THREE-PHASE DOUBLE CONVERSION UPS UNDER UNBALANCED LOAD

PWM rectifiers are widely used in three-phase ac-dc-ac systems due to its capability in dc voltage boost and regulation, input power factor correction, and input current harmonic control. However, with the conventional rectifier control technique, the input current tends to be unbalanced under unbalanced inverter load, which contaminates input power source and is therefore undesirable. In this chapter, the cause of the unbalancing is disclosed by evaluating the spectra of the switching functions of the full bridge three-phase inverter analytically using Bessel function under standard space vector PWM switching scheme, which relates the dc link current and voltage ripples to the inverter load balancing. The analysis shows that the dc link voltage contains significant second order harmonic component which affects the voltage loop of the rectifier controller, especially when the control gain is high. A notch filter based voltage control loop is proposed to eliminate the second harmonic component in the dc-link voltage feedback signal and achieve balanced three-phase input currents. Simulation and experimental results are presented to demonstrate the effectiveness of the proposed control technique in decoupling the rectifier and the inverter under unbalanced load.

4.1 Introduction

Three-phase ac-dc-ac voltage stiff systems consisting of a front-end rectifier, a dc link with a capacitor, and an inverter are widely used in motor drive, on-line UPS, and distributed generation systems. A PWM controlled front-end rectifier is desirable due to its capability of dc voltage boost and regulation, input power factor correction (PFC), and input current harmonic control. Conventional PFC boost rectifier controllers usually have two feedback loops - an outer voltage loop and an inner current loop, where the voltage regulator generates current command for d-axis current while the q-axis current command is zero for unity power factor control as shown in Figure 4.1. Under normal operating conditions, steady state dc bus voltage is a constant and the voltage regulator output, i.e., the d-axis current command, is also a constant, which yields a constant power drawn from the input ac stage and balanced three-phase input currents. However, once the inverter load is not balanced, the output power is no longer a constant, which leads to fluctuation of the dc link voltage. On the rectifier side, the ripple corrupted dc link voltage is fed back to the voltage regulator which generates a fluctuating d-axis current command under a constant dc voltage reference. If the current regulator of d-axis has high bandwidth, it yields fast current tracking and consequently a fluctuating rectifier output current which causes unbalanced front-end input current and high total harmonic distortion (THD) in the input current. This is considered contamination of power system if the front-end is fed by utility and therefore undesirable.

Although this particular problem has not been addressed in literature, related researches have been conducted on rectifier control under unbalanced input voltage conditions [18,78,93,98]. Kamran et al. [43] have mentioned dc voltage ripple problem

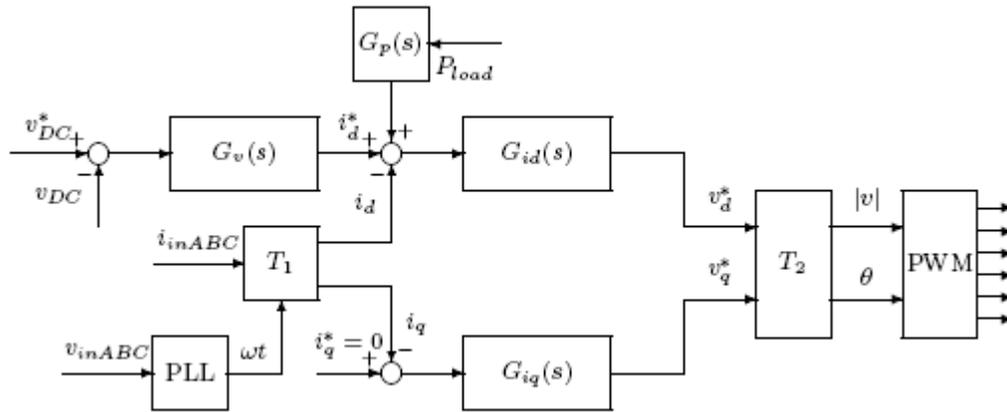


Figure 4.1: A conventional PWM rectifier control system with load power feedforward.

caused by either unbalanced inverter load current or unbalanced input voltage supply. However, their control goal was to minimize the dc link voltage ripple instead of improving the input power quality. Some other researches focused on improving instantaneous power balance between the input and output of a rectifier-inverter system and minimizing the dc coupling capacitance to reduce the cost [46,61,67,102, 107]. The less the dc coupling capacitance is, the better instantaneous power balance the system could yield. However, this is only desirable under balanced load. Once the inverter load is unbalanced, it is apparent that the steady state inverter output power is no longer a constant, and neither is the inverter input dc power. Due to the existence of the dc link capacitor, the rectifier side steady state power can be decoupled from the inverter side and controlled to be a constant without being

affected by the power fluctuation on the inverter side, which will lead to balanced front-end three-phase input currents. To achieve this goal, a new rectifier controller has to be designed to enforce constant input power and not to respond to the dc voltage ripple.

In this research, a switching function concept will be used under standard space vector PWM to quantify the harmonic components in the dc link. According to the analysis result, a notch filter will be designed and applied to eliminate the undesired harmonic component from the feedback signal. The proposed controller with the notch filter will yield constant rectifier power under steady state and balanced three-phase input currents.

The switching function concept for power converters has been used in [78], [98], and [18] to show the existence of harmonics in dc bus voltage. However, none of these works has quantified the harmonic components analytically and used the result to handle the ripple problem in the systems as this chapter will do.

Both simulation and experimental test results will be presented to demonstrate the effectiveness of the proposed control technique.

4.2 System Analysis

In this research, a standard on-line UPS system as shown in Figure 4.2 is analyzed.

This system consists of a boost type front-end rectifier, a dc link, and a voltage source inverter. Both power converters use standard space vector PWM switching scheme as described in [110]. The inverter is controlled using the approach presented in [45] and [70], which yields fast voltage regulation with minimized THD. The output power feedforward technique as proposed in [46, 61, 67, 102, 107] is not included as a part of the solution of the control problem raised in this research due to the following two considerations. One is that independent control of the rectifier and inverter leads to lower cost and higher reliability and the other, which is more critical, is that the objective of the power feedforward technique is to achieve fast dc bus voltage

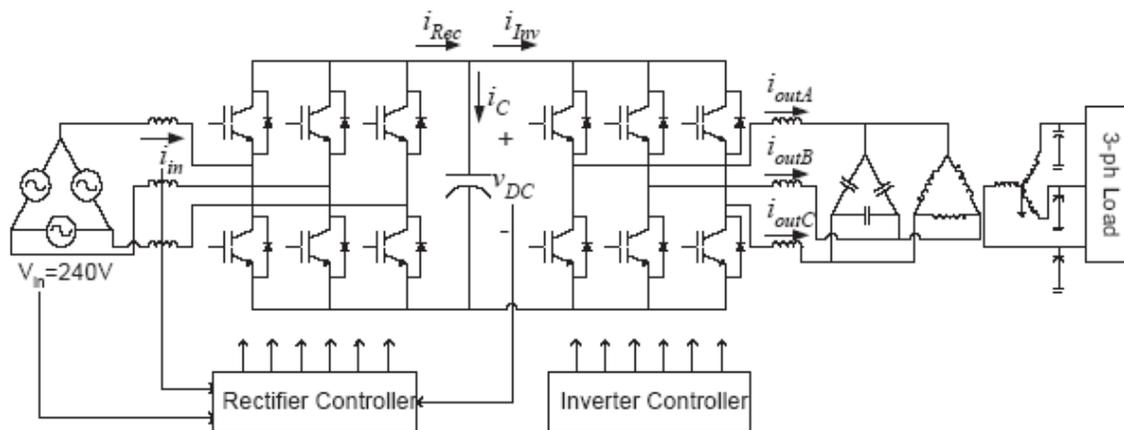


Figure 4.2: The three-phase ac-dc-ac system topology.

regulation, which is inherently against the control goal in this research. The control goal in this research is to eliminate the effects of unbalanced three-phase inverter load on the front-end input current and still guarantee unity power factor and fast dc bus voltage regulation against load disturbances.

The effect of load balancing is analyzed as follows. The inverter input current is

$$i_{inv} = S_A i_{outA} + S_B i_{outB} + S_C i_{outC}, \quad (4.1)$$

where S_A , S_B , and S_C are the switching functions of the top switches of the three inverter legs. When the top switch of leg i is on, $S_i = 1$, otherwise, $S_i = 0$, where $i \in \{A, B, C\}$. Expand the spectra of these switching functions assuming purely sinusoidal phase currents as

$$\begin{aligned} i_{inv}(t) = & \sum_{k=1}^{\infty} A_k \sin k\omega t \cdot I_{outA} \sin(\omega t + \phi_A) \\ & + \sum_{k=1}^{\infty} A_k \sin k(\omega t - 120^\circ) \cdot I_{outB} \sin(\omega t - 120^\circ + \phi_B) \\ & + \sum_{k=1}^{\infty} A_k \sin k(\omega t + 120^\circ) \cdot I_{outC} \sin(\omega t + 120^\circ + \phi_C), \end{aligned} \quad (4.2)$$

where A_k is the magnitude of the k -th order component and $A_k \equiv 0$ for all even k .

After trigonometric transform, it can be obtained that

$$\begin{aligned}
i_{inv}(t) &= \frac{I_{outA}}{2} \sum_{k=1}^{\infty} A_k \{ \cos[(k-1)\omega t - \phi_A] - \cos[(k+1)\omega t + \phi_A] \} \\
&\quad + \frac{I_{outB}}{2} \sum_{k=1}^{\infty} A_k \{ \cos[(k-1)\omega t - (k-1)120^\circ - \phi_B] \\
&\quad - \cos[(k+1)\omega t - (k+1)120^\circ + \phi_B] \} \\
&\quad + \frac{I_{outC}}{2} \sum_{k=1}^{\infty} A_k \{ \cos[(k-1)\omega t + (k-1)120^\circ - \phi_C] \\
&\quad - \cos[(k+1)\omega t + (k+1)120^\circ + \phi_C] \} \\
&= I_{inv0} + \sum_{n=1}^{\infty} I_{invn} \sin n(\omega t + \theta_n),
\end{aligned} \tag{4.3}$$

where I_{inv0} is the dc component of the inverter input current and I_{invn} is the magnitude of n -th order component of the current [78]. From (4.3), it is apparent that $I_{outA}=I_{outB}=I_{outC}$ and $\phi_A=\phi_B=\phi_C$ hold and $I_{invn}=0$ for $n > 0$ if the three-phase load currents are balanced. Otherwise, ac components exist in the current and cause ripple.

It can be observed from (4.3) that, given fixed three-phase currents, I_{inv0} is proportional to A_1 only, I_{inv2} is a linear combination of A_1 and A_3 , I_{inv4} is a linear combination of A_3 and A_5 , and so on. Within the low frequency range, $I_{invn}=0$ for odd n since $A_k \equiv 0$ for even k .

The values of A_k must be calculated to evaluate the significance of each order of the harmonics. Under the standard space vector PWM, the first few components can be calculated using the algorithm in [11]

$$A_{2q+1} = \frac{4}{\pi(2q+1)\frac{\omega_m}{\omega_c}} \times J_{2q+1}\left(\frac{\pi a}{2}(2q+1)\frac{\omega_m}{\omega_c}\right), \quad (4.4)$$

where $q = 0, 1, 2, \dots, \infty$, ω_m is the modulation frequency, ω_c is the carrier frequency, $\omega_m \ll \omega_c$, a is the modulation index, and $J_v(z)$ is the first kind of Bessel function.

Equation (4.4) is valid only at the frequency range much less than the carrier frequency where the side band of the carrier frequency is negligible. In the system studied in

this research, $\frac{\omega_m}{\omega_c} = \frac{1}{90}$ is applied and the first several terms are calculated assuming normalized modulation index: $A_1 = 1$, $A_3 = 1.142 \times 10^{-4}$, $A_5 = 3.020 \times 10^{-8}$, and $A_7 = 1.030 \times 10^{-11}$. Apparently, compared to A_1 , all other terms can be ignored.

Based on the above analysis, it can be seen that the A_1 terms only contributes to I_{inv0} and I_{inv2} , where the latter is not desired. Therefore, an undesirable second harmonic component must be generated in i_{inv} by the load unbalance and the magnitude of the harmonic is determined by the significance of the unbalance.

The second harmonic current fed into the inverter causes fluctuation of the capacitor voltage in the same order. This fluctuation is fed back to the rectifier side voltage regulator which generates a fluctuating d-axis current command i^*_d as shown in Figure 4.1. Usually the current regulator has high bandwidth and yields fast response which causes a second harmonic component in the rectifier output current i_{rec} . Due to the same theory as analyzed above, this second harmonic will cause unbalance in the front-end three-phase input currents.

Even though the second harmonic ripple on the dc link voltage seems annoying, suppressing it would not solve the front-end current unbalance problem since the current i_{rec} is still distorted. The strategy proposed in this chapter is to leave the voltage ripple uncontrolled but remove the second harmonic from i_{rec} . However, the rectifier voltage regulation still has to respond to disturbances on the dc bus voltage other than the second harmonic caused by the unbalanced load. Therefore, the second harmonic component needs to be identified and removed from the feedback.

4.3 The Control Strategy

In power supply applications, the nominal frequency is 60 Hz. With a 60 Hz fundamental inverter voltage output, the dc bus ripple must be 120 Hz. A digital band-stop filter can be designed to suppress the ripple with known frequency. A digital Butterworth filter with order $2n$ and lower and upper cutoff frequencies ω_1 and ω_2 can be designed using Matlab[®] function `butter()`. This filter will be applied to the measured v_{dc} and its output will be used by the voltage regulator.

A PI controller is used for voltage regulation and a discrete-time sliding mode controller (DSMC) is used for the inner current loop since it has been proved more effective than PI [45]. The DSMC is described as follows.

The rectifier circuit including the input inductance shown in Figure 4.2 can be modelled as an LTI system and represented in state space. The current controller

controls the input current, i.e., the inductor current. In discrete time, the system can be described by

$$i_{in}(k+1) = A_i i_{in}(k) + B_i v_{pwm}(k) + E_i v_{in}(k) \quad (4.5)$$

where the input current i_{in} , rectifier control voltage v_{pwm} , and input supply voltage v_{in} are all represented in synchronous dq reference frame and A_i , B_i , and E_i are all system coefficients determined by the circuit parameters. Given inverter current command $i_{ref}(k)$, the DSMC equivalent control law is

$$v_{pwm,eq}(k) = B_i^{-1} [i_{ref}(k) - A_i i_{in}(k) - E_i v_{in}(k)]. \quad (4.6)$$

With the rectifier control voltage limit v_{max} determined by the dc bus voltage and the PWM technique used, the actual control voltage becomes

$$v_{inv} = \begin{cases} v_{pwm,eq} & \text{if } \|v_{pwm,eq}\| \leq v_{max}, \\ \frac{v_{max}}{\|v_{pwm,eq}\|} v_{pwm,eq} & \text{otherwise.} \end{cases} \quad (4.7)$$

4.4 Simulation Results

Simulations have been performed to compare the performance of the proposed control technique to that of the conventional control. An unbalanced load, where $P_A = 1.6$ kW, i.e., approximately 100% load on one phase, and $P_B = P_C = 0$ is

applied to a 5 kVA system as shown in Figure 4.2. The notch filter design parameters are $n = 2$, $\omega_1 = 140\pi$, and $\omega_2 = 540\pi$. Some steady state performances are recorded in Table 4.1, where the rectifier three-phase input currents are measured and converted to positive-negative-zero sequence frame to observe the significance of unbalance, where I_{+in} and I_{-in} are the positive and negative sequence quantities respectively. THD of the input current is also monitored. Table 4.1 shows that the undesirable negative sequence component in the input current has been nearly eliminated, the input current THD is also reduced under certain amount of load. This result implies that the decoupling between the inverter and the rectifier is achieved by the dc link in that load imbalance on the inverter side does not affect the front-end rectifier and its input current.

The dynamic performance of the proposed control with harmonic compensation is also compared to that of the convention controller as shown in Figure 4.3 and Figure 4.4, where phase A load steps up from 0 to 100%.

It can be observed by comparing the v_{dc} traces in these figures that the proposed control technique yields balanced three-phase input currents with low THD and simultaneously perform fast v_{dc} regulation under significant load disturbances.

	Conventional	Proposed
I_{in}^+ (A)	7.602	7.566
I_{in}^- (A)	1.486	0.085
I_{inA} THD	5.92%	4.48%

Table 4.1: Steady state simulations - I_{+in} & I_{-in} are the rectifier input positive & negative sequence currents, and I_{inA} THD is the total harmonic distortion of Phase A input current.

4.5 Experimental Results

Experimental tests have been performed on a 5 kVA laboratory setup which has the topology in Figure 4.2. Two Texas Instruments[®] TMS320LF2407A DSPs are used to control the rectifier and inverter respectively.

The same load as used above in the simulation has also been applied in the experiments. Figure 4.5 shows the data of measured v_{dc} and the filtered values collected online under steady state. It is apparent that the directly measured v_{dc} represented by the dashed trace has a dominant 120 Hz component which is significantly suppressed by the 4th-order notch filter as illustrated by the solid trace with existence of measurement noise. Transient tests as done above in the simulation have also been duplicated on the experimental setup and the results are presented by Figure 4.6 and Figure 4.7. It can be observed that the proposed control technique improves the balance of the three-phase input currents while maintains the v_{dc} regulation capability to transient load disturbances unaffected. The resemblance of the waveforms to those in Figure 4.3 and Figure 4.4 has validated the simulation results.

4.6 Summary of Chapter

A novel control technique has been proposed for the front-end PWM rectifier in standard rectifier-inverter systems to achieve decoupling between the converters with the capacitive dc link under unbalanced three-phase inverter load. Analytical work has been conducted to disclose the mechanism how the inverter load unbalancing affects the control of the front-end rectifier. On basis of the analysis, a notch filter is then designed and utilized in the voltage loop to suppress the undesired 2nd harmonic component in the dc link voltage feedback, which implements the power decoupling between the rectifier and the inverter and yields balanced input current and does not undermine the dynamic response of dc bus voltage regulation. The effectiveness of the proposed control technique has been demonstrated by both simulations and experimental tests.

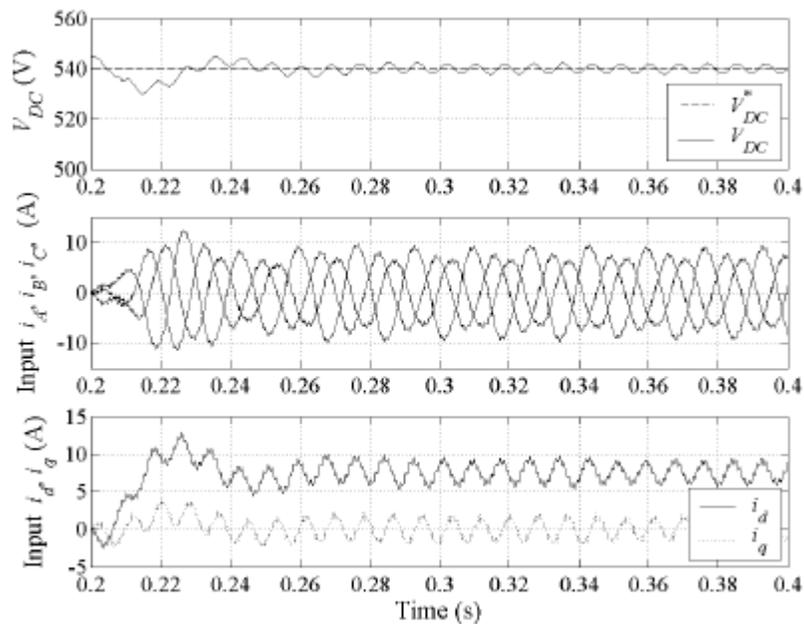


Figure 4.3: Simulation results - transients under conventional control.

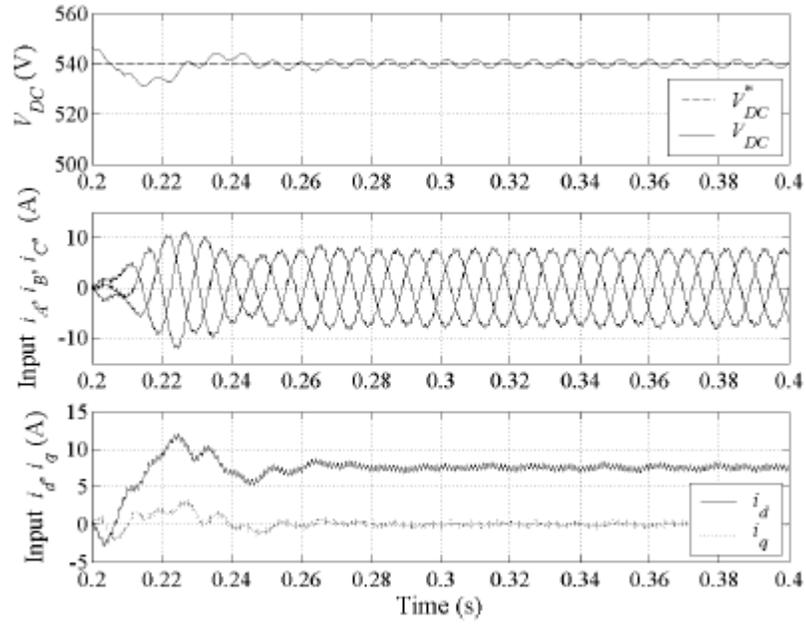


Figure 4.4: Simulation results - transients under the proposed control.

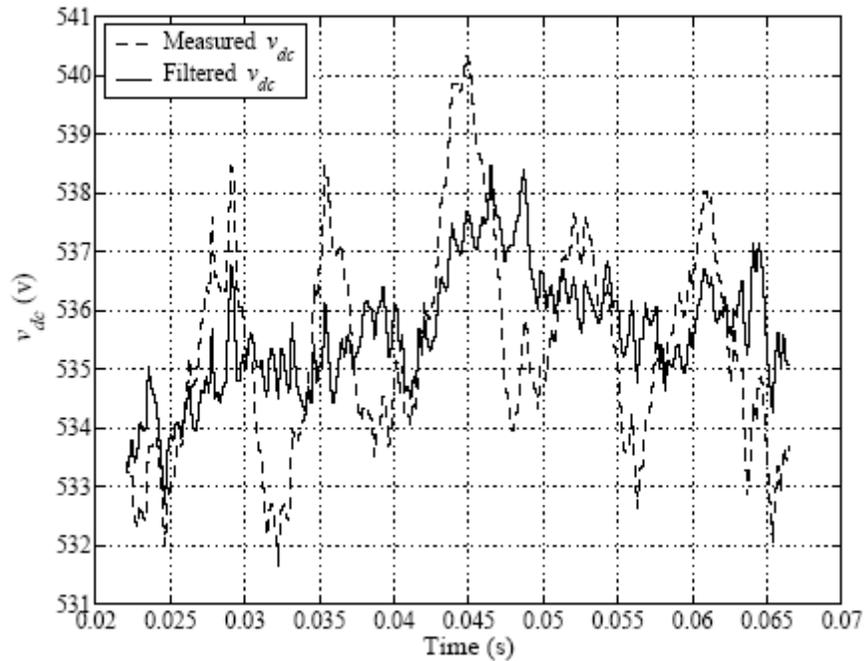


Figure 4.5: Experimental results - measured vs. filtered v_{dc} .

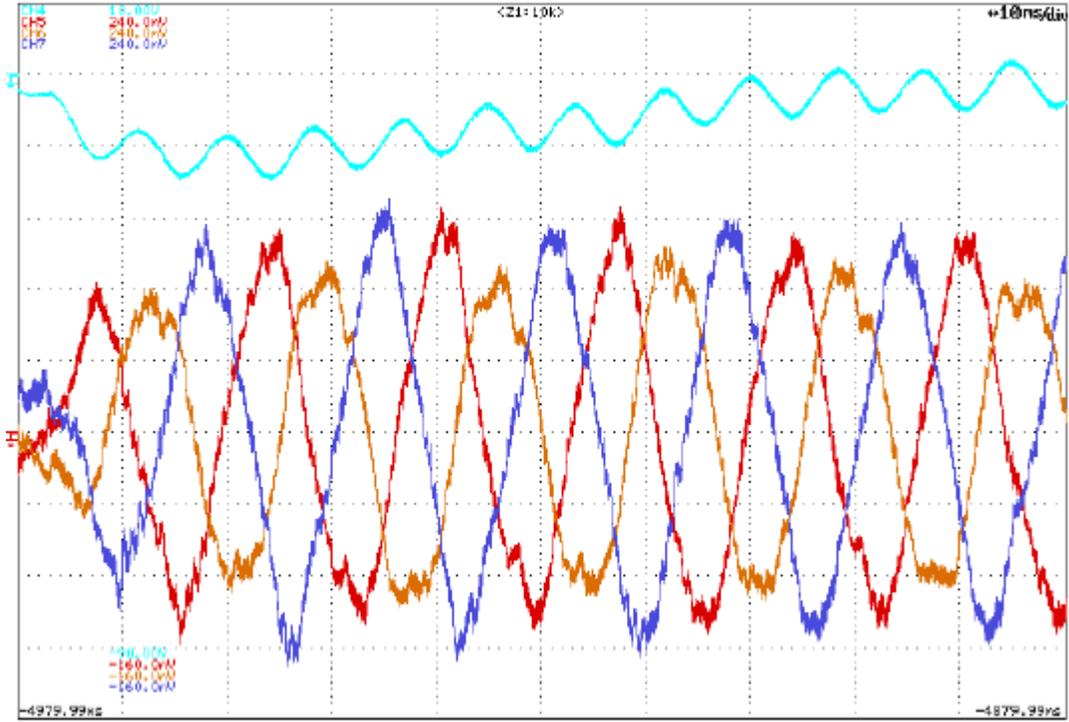


Figure 4.6: Experimental results - conventional, v_{dc} (top trace) and i_{inABC} .

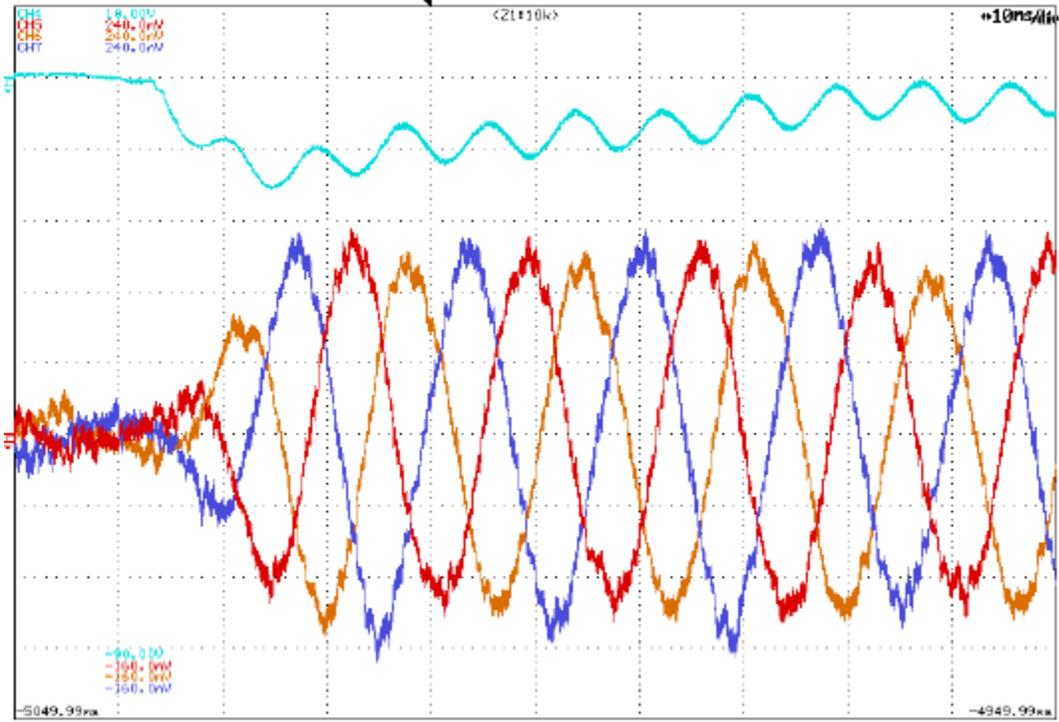


Figure 4.7: Experimental results - proposed, v_{dc} (top trace) and i_{inABC} .

CHAPTER 5

MATLAB CODE FOR ANALYSIS

5.1 Frequency Domain Analysis

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
% Frequency domain analysis of 3-ph 4-wire transformerless inverter
% control using RSC and DSMC. Frequency responses of the open-loop plant,
% closed current loop, and closed voltage loop with nominal parameters
% are
% calculated.
% Min Dai 06/16/2005
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%

clear all

% PWM Inverter Voltage Rating and Filter Components
KVA=5e3;
inv_volt=240/sqrt(3);           % L-L Inverter Cap Voltage
out_volt=120;                  % L-N output voltage
tr=out_volt/inv_volt;         % transformer turn ratio
Cinv=55e-6;                   % Inverter filter capacitor
Linv=10.2e-3;                 % Inverter filter inductor = 1.8+2*4.2
                                % 3 reactors connected in series
                                % RMS current <= 12 Amperes
Rinv=1;                       % many inductors connected in series

fs=40e6/2/3704;              % PWM switching frequency

% Define control sampling time
Tsamp=1/fs;
%Tsamp=1e-6*fix(Tsamp*1e6);

% Define fundamental frequency
ffun=60;
wfun=2*pi*ffun;

%% Define harmonics frequencies
w1=wfun;          % 1st harmonic
w2=2*wfun;       % 2rd harmonic
w3=3*wfun;       % 3rd harmonic
w4=4*wfun;       % 4rd harmonic
w5=5*wfun;       % 5th harmonic
w7=7*wfun;       % 7th harmonic

%% Define KVA, voltages, currents, and impedance bases
KVAb=1/3*5e3;    % Single phase KVA base
Vb_load=out_volt*sqrt(2); % Load voltage base
Ib_load=KVAb/out_volt*sqrt(2); % Load current base
Zb_load=Vb_load/Ib_load; % Load impedance base

%% Compute perunit value of filter components
xCinv=1/(wfun*Cinv)/Zb_load % Inverter capacitor filter
xLinv=(wfun*Linv)/Zb_load % Inverter inductor filter
xRinv=Rinv/Zb_load;
```

```

%% Per Unit Current Limit
Ilimit=3;          % 300% inverter current limit

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Start design of discrete SM current controller
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Define the plant for the current controller

A=[0                xCinv*wfun ;
  -1/(xLinv/wfun)   -xRinv/(xLinv/wfun)];
B=[0;
  1/(xLinv/wfun)];
E=[-xCinv*wfun;
  0];
F=[0;
  -1];
C=[0 1];
D=0;

% Discretize the plant for the current controller

sysc=ss(A,B,C,zeros(size(C,1),size(B,2)), 'inputdelay',0);
sysd=c2d(sysc,Tsamp,'zoh');
[Acurrd,Bcurrd,Ccurrd,Dcurrd]=ssdata(sysd);
CBinv=inv(Ccurrd*Bcurrd);
CA=Ccurrd*Acurrd;
CD=Ccurrd*F;
sysc=ss(A,E,C,zeros(size(C,1),size(B,2)), 'inputdelay',0);
sysd=c2d(sysc,Tsamp,'zoh');
[Acurrd1,Ecurrd,Ccurrd1,Dcurrd1]=ssdata(sysd);
CE=Ccurrd1*Ecurrd;

%%% Discrete sliding mode controllers gains
Ksm_q=[CBinv(1,1) -CBinv(1,1)*CA(1,1)*[1.5 -0.5] ...
  -CBinv(1,1)*CA(1,2)*[1.5 -0.5] -CBinv(1,1)*CE(1,1)*[1.5 -0.5] ];
%Ksm_q=[CBinv(1,1) -CBinv(1,1)*CA(1,1)*[1 0] ...
%       -CBinv(1,1)*CA(1,2)*[1 0] -CBinv(1,1)*CE(1,1)*[1 0] ];
%                                     % no prediction

% Define Discrete Sliding Mode Controller for frequency domain analysis,
% see below.
% x=[vinv(k-1) iinv(k-1) iload(k-1)]
% u=[icmd viinv iinv iload]
% y=vpwm

Asm=zeros(3,3);

Bsm=[0 1 0 0;
     0 0 1 0;
     0 0 0 1];

Csm=[Ksm_q(3) Ksm_q(5) Ksm_q(7)];

Dsm=[Ksm_q(1) Ksm_q(2) Ksm_q(4) Ksm_q(6)];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Start design of Perfect RSP voltages controllers
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

```

%% Define the true plant
Ao=A;
Bo=B;
Co=[1 0];
Do=0;

%% Define the analog servo compensator
Ch1=[0 1;
     -w1^2 0];
Ch2=[0 1;
     -w2^2 0];
Ch3=[0 1;
     -w3^2 0];
Ch4=[0 1;
     -w4^2 0];
Ch5=[0 1;
     -w5^2 0];
Ch7=[0 1;
     -w7^2 0];

Ch_star=[[Ch1      zeros(2,2)  zeros(2,2)  zeros(2,2) ];
         [zeros(2,2) Ch3      zeros(2,2)  zeros(2,2) ];
         [zeros(2,2) zeros(2,2) Ch5      zeros(2,2) ];
         [zeros(2,2) zeros(2,2) zeros(2,2) Ch7      ]
        ];

Bh_star=[0;
         1;
         0;
         1;
         0;
         1;
         0;
         1;
         ];

% Discretize true plant
sysc=ss(Ao,Bo,Co,Do,'inputdelay',0.5*Tsamp);
sysd=c2d(sysc,Tsamp,'zoh');
[Aod,Bod,Cd, Dd]=ssdata(sysd);

C1=[1 0 0;
     0 1 0 ];
Ad=Aod-Bod*CBinv*CA*C1;
Bd=Bod*CBinv;

Cc_star=eye(size(Ch_star,1));
% Discretize and compute balanced realization of the controller
csysc=ss(Ch_star,Bh_star,Cc_star,zeros(size(Ch_star,1),size(Bh_star,2)));
[csysbc,Tbal]=ssbal(csysc);
csysd=c2d(csysbc,Tsamp,'zoh');
[Acon_d,Bcon_d,Ccon_d,Dcon_d]=ssdata(csysd);

```

```

% Form the augmented equivalent plant and the servo compensator
Ad_big=[Ad zeros(size(Ad,1),size(Acon_d,2));
        -Bcon_d*Cd Acon_d];
Bd_big=[Bd ; -Bcon_d*Dd];

% Define the weighting matrices
epsilon=1e-5;
% state_W=0.005; WP
% fund_servo_W=3e5; 5e5; %WS1
% harm_servo_W=1e-3*1e4; WH

state_W=0.005; %WP
fund_servo_W=5e5; %5e5; %WS1
harm_servo_W=5e5; %WH

Q1=state_W*eye(size(Ad,1));

Q2=eye(size(Acon_d,1));
Q2(1:2,:)=fund_servo_W*Q2(1:2,:);
Q2(3:8,:)=harm_servo_W*Q2(3:8,:);

Q=[ Q1 zeros(size(Ad,1),size(Acon_d,2));
    zeros(size(Acon_d,1),size(Ad,2)) Q2];

R=epsilon;

% Now perform the optimal calculations of the gains
[Kd,S,E]=dlqr(Ad_big,Bd_big,Q,R);
Kd=-Kd;

% Frequency domain analysis for the 3-ph 4-wire inverter system
% (performed in discrete-time):

% LC filter characteristic, in real values
LC_sys=tf(1,[Linv*Cinv Rinv*Cinv 1]);
natural_freq=1/sqrt(Linv*Cinv) % in rad/s
damping_ratio=Rinv*sqrt(Cinv/(4*Linv))

% parameter definition, in per unit
B=0.6; % per-unit susceptance of load parallel inductor
YB=wfun*B; % convert into complement of inductance
YG=0.8; % load parallel resistor

Cnom=xCinv*wfun;
Lnom=xLinv/wfun;
Rnom=xRinv;

r_epsilon=0.01; % per-unit series resistance in the load inductive
branch, negligible

Ap=[ -YG/Cnom 1/Cnom -1/Cnom;
     -1/Lnom -Rnom/Lnom 0;
     % YB 0 0 ];
     YB 0 -r_epsilon*YB ];

Bp=[ 0 ;
     1/Lnom ;
     0 ];

Cp=[ 1 0 0;
     0 1 0];

```

```

        YG          0          1  ];

Dp=[    0;
       0;
       0    ];

sysp=ss (Ap, Bp, Cp, Dp);           % the plant

N1=500;
W1=logspace (2, 4, N1);
[LCmag, LCphase]=bode (LC_sys, W1);
for i=1:N1,
    LCmagdb(i)=20*log10 (LCmag (1, 1, i));
    LCph(i)=LCphase (1, 1, i);
end
figure (1)
%bode (sysp);                       % open-loop plant bode plot
%bode (LC_sys);                     % open-loop LC filter
bode plot
%grid;
subplot (2, 1, 1);
semilogx (W1, LCmagdb, 'b-');grid;zoom on;
title ('Bode Plot', 'FontName', 'times new roman', 'FontSize', 16);
ylabel ('Magnitude (dB)', 'FontName', 'times new roman', 'FontSize', 16);
set (gca, 'FontName', 'times new roman');
set (gca, 'FontSize', 16);

subplot (2, 1, 2);
semilogx (W1, LCph, 'b-');grid;zoom on;
ylabel ('Phase (deg)', 'FontName', 'times new roman', 'FontSize', 16);
set (gca, 'FontName', 'times new roman');
set (gca, 'FontSize', 16);
xlabel ('Frequency (rad/s)', 'FontName', 'times new roman', 'FontSize',
16);
% End of figure (1).

sysp.inputdelay=[0.5*Tsamp];
syspd=c2d (sysp, Tsamp, 'zoh');      % discrete time plant with
input time delay

%sysp_w=d2c (syspd, 'tustin');      % continuous plant with input
time delay
%[Ap_d, Bp_d, Cp_d, Dp_d]=ssdata (sysp_w); % do it in continuous time
[Ap_d, Bp_d, Cp_d, Dp_d]=ssdata (syspd); % do it in discrete-time

dsm=pck (Asm, Bsm, Csm, Dsm);       % see above for the definitions
of the ABCD

Aservo=[    Acon_d    zeros (8, 1);
          zeros (1, 8)  0          ];

Bservo=[    Bcon_d    zeros (8, 3);
          zeros (1, 3)  1    ];

Cservo=[    Kd (4:11)    Kd (3)    ];

Dservo=[    0    Kd (1:2)  0    ];

servo=pck (Aservo, Bservo, Cservo, Dservo);
systemnames='dsm servo';
inputvar=' [err; plant{3}]';       % plant{3} includes Vload, Iinv,
Iload
outputvar=' [dsm]';

```

```

input_to_dsm='[servo; plant(1,2,3)]';
input_to_servo='[err; plant(1:2) ; dsm]';
sysoutname='Hcontrol_d';
cleanup_sysic = 'no';
sysic;

[Acontrol,Bcontrol,Ccontrol,Dcontrol]=unpck(Hcontrol_d);
sys_con_d=ss(Acontrol,Bcontrol,Ccontrol,Dcontrol,Tsamp);
%sys_con_c=d2c(sys_con_d,'tustin'); % continuous
controller
%[Acontrol,Bcontrol,Ccontrol,Dcontrol]=ssdata(sys_con_c);

plant_nom_w=pck(Ap_d,Bp_d,Cp_d,Dp_d);
controller_w=pck(Acontrol,Bcontrol,Ccontrol,Dcontrol);
systemnames='plant_nom_w controller_w';
inputvar='[vref]';
%outputvar='[vref-plant_nom_w(1)]';
outputvar='[plant_nom_w(1)]';
input_to_plant_nom_w='[controller_w]';
input_to_controller_w='[vref-plant_nom_w(1);plant_nom_w(1:3)]';
sysoutname='clp_w';
cleanup_sysic = 'no';
sysic;

[Avlp,Bvlp,Cvlp,Dvlp]=unpck(clp_w);
%sys_vloop=ss(Avlp,Bvlp,Cvlp,Dvlp);
sys_vloop=ss(Avlp,Bvlp,Cvlp,Dvlp,Tsamp);

[Vmag, Vphase, W2]=bode(sys_vloop);
N2=length(W2)
for i=1:N2,
    Vmagdb(i)=20*log10(Vmag(1,1,i));
    Vph(i)=Vphase(1,1,i);
end
figure(2)
subplot(2,1,1);
semilogx(W2, Vmagdb,'b-');grid;zoom on;
axis([1e-3 1e5 -200 50]);
title('Bode Plot', 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
ylabel('Magnitude (dB)', 'FontName','times new roman', 'FontSize', 16);

subplot(2,1,2);
semilogx(W2, Vph-360,'b-');grid;zoom on;
axis([1e-3 1e5 -180 180]);
ylabel('Phase (deg)', 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
xlabel('Frequency (rad/s)', 'FontName','times new roman', 'FontSize',
16);
% End of figure(2).
figure(3)
pzmap(sys_vloop);
axis([-1 1 -1 1]);
grid % done with closed voltage loop analysis
title('Pole-Zero Map', 'FontName','times new roman', 'FontSize', 16);
ylabel('Imaginary Axis', 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
xlabel('Real Axis', 'FontName','times new roman', 'FontSize', 16);

```

```

% Closed current loop (open voltage loop) analysis
systemnames='plant_nom_w dsm';
inputvar='[icmd]';
outputvar='[plant_nom_w(2)]';
input_to_plant_nom_w='[dsm]';
input_to_dsm='[icmd;plant_nom_w(1:3)]';
sysoutname='clp_i';
cleanup_sysic = 'no';
sysic;

[Ailp,Bilp,Cilp,Dilp]=unpck(clp_i);
%sys_iloop=ss(Ailp,Bilp,Cilp,Dilp);
sys_iloop=ss(Ailp,Bilp,Cilp,Dilp,Tsamp);

[Imag, Iphase, W3]=bode(sys_iloop);
N3=length(W3)
for i=1:N3,
    Imagdb(i)=20*log10(Imag(1,1,i));
    Iph(i)=Iphase(1,1,i);
end
figure(4)
subplot(2,1,1);
semilogx(W3, Imagdb,'b-');grid;zoom on;
axis([1e-2 1e4 -10 10]);
title('Bode Plot', 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
ylabel('Magnitude (dB)', 'FontName','times new roman', 'FontSize', 16);

subplot(2,1,2);
semilogx(W3, Iph,'b-');grid;zoom on;
axis([1e-2 1e4 -225 45]);
ylabel('Phase (deg)', 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
xlabel('Frequency (rad/s)', 'FontName','times new roman', 'FontSize', 16);
% End of figure(4).
figure(5)
pzmap(sys_iloop);
grid % done with closed current loop analysis
title('Pole-Zero Map', 'FontName','times new roman', 'FontSize', 16);
ylabel('Imaginary Axis', 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
xlabel('Real Axis', 'FontName','times new roman', 'FontSize', 16);

```

5.2 Robust Stability Analysis

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%
% Robust stability analysis of 3-ph 4-wire transformerless inverter
% control using RSC and DSMC
% Min Dai 06/12/2005
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%

clear all

% PWM Inverter Voltage Rating and Filter Components
KVA=5e3;

```

```

inv_volt=240/sqrt(3);           % L-L Inverter Cap Voltage
out_volt=120;                   % L-N output voltage
tr=out_volt/inv_volt;          % transformer turn ratio
Cinv=55e-6;                     % Inverter filter capacitor
Lin=10.2e-3;                    % Inverter filter inductor = 1.8+2*4.2
                                % 3 reactors connected in series
                                % RMS current <= 12 Amperes
Rinv=1;                          % many inductors connected in series

fs=40e6/2/3704;                % PWM switching frequency

% Define control sampling time
Tsamp=1/fs;
%Tsamp=1e-6*fix(Tsamp*1e6);

% Define fundamental frequency
ffun=60;
wfun=2*pi*ffun;

%% Define harmonics frequencies
w1=wfun;      % 1st harmonic
w2=2*wfun;    % 2rd harmonic
w3=3*wfun;    % 3rd harmonic
w4=4*wfun;    % 4rd harmonic
w5=5*wfun;    % 5th harmonic
w7=7*wfun;    % 7th harmonic

%% Define KVA, voltages, currents, and impedance bases
KVA=1/3*5e3;      % Single phase KVA base
Vb_load=out_volt*sqrt(2); % Load voltage base
Ib_load=KVA/out_volt*sqrt(2); % Load current base
Zb_load=Vb_load/Ib_load; % Load impedance base

%% Compute perunit value of filter components
%xCinv=1/(wfun*3*Cinv)/Zb_load % Inverter capacitor filter
xCinv=1/(wfun*Cinv)/Zb_load % Inverter capacitor filter
xLin=(wfun*Lin)/Zb_load % Inverter inductor filter
xRinv=Rinv/Zb_load;

%% Per Unit Current Limit
Ilimit=3; % 300% inverter current limit

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Start design of discrete SM current controller
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Define the plant for the current controller

A=[0 xCinv*wfun ;
  -1/(xLin/wfun) -xRinv/(xLin/wfun)];
B=[0;
  1/(xLin/wfun)];
E=[-xCinv*wfun;
  0];
F=[0;
  -1];
C=[0 1];
D=0;

% Discretize the plant for the current controller

```

```

sysc=ss(A,B,C,zeros(size(C,1),size(B,2)),'inputdelay',0);
sysd=c2d(sysc,Tsamp,'zoh');
[Acurrd,Bcurrd,Ccurrd,Dcurrd]=ssdata(sysd);
CBinv=inv(Ccurrd*Bcurrd);
CA=Ccurrd*Acurrd;
CD=Ccurrd*F;
sysc=ss(A,E,C,zeros(size(C,1),size(B,2)),'inputdelay',0);
sysd=c2d(sysc,Tsamp,'zoh');
[Acurrd1,Ecurrd,Ccurrd1,Dcurrd1]=ssdata(sysd);
CE=Ccurrd1*Ecurrd;

%%% Discrete sliding mode controllers gains
Ksm_q=[CBinv(1,1) -CBinv(1,1)*CA(1,1)*[1.5 -0.5] ...

        -CBinv(1,1)*CA(1,2)*[1.5 -0.5] -CBinv(1,1)*CE(1,1)*[1.5 -0.5] ];
%Ksm_q=[CBinv(1,1) -CBinv(1,1)*CA(1,1)*[1 0] ...
%      -CBinv(1,1)*CA(1,2)*[1 0] -CBinv(1,1)*CE(1,1)*[1 0] ]; % no
prediction

%% Define Discrete Sliding Mode Controller for robust stability analysis,
%% see below.
%% x=[vinv(k-1) iinv(k-1) iload(k-1)]
%% u=[icmd viinv iinv iload]
%% y=vpwm

Asm=zeros(3,3);

Bsm=[0 1 0 0;
      0 0 1 0;
      0 0 0 1];

Csm=[Ksm_q(3) Ksm_q(5) Ksm_q(7)];

Dsm=[Ksm_q(1) Ksm_q(2) Ksm_q(4) Ksm_q(6)];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Start design of Perfect RSP voltages controllers
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Define the true plant

Ao=A;

Bo=B;

Co=[1 0];

Do=0;

%% Define the analog servo compensator
Ch1=[0 1;
      -w1^2 0];

Ch2=[0 1;
      -w2^2 0];

Ch3=[0 1;
      -w3^2 0];

Ch4=[0 1;
      -w4^2 0];

Ch5=[0 1;

```

```

-w5^2 0];

Ch7=[0 1;
      -w7^2 0];

Ch_star=[ [Ch1      zeros(2,2)  zeros(2,2)  zeros(2,2) ];
           [zeros(2,2)  Ch3      zeros(2,2)  zeros(2,2) ];
           [zeros(2,2)  zeros(2,2)  Ch5      zeros(2,2) ];
           [zeros(2,2)  zeros(2,2)  zeros(2,2)  Ch7      ]
];

Bh_star=[0;
          1;
          0;
          1;
          0;
          1;
          0;
          1;
          1;];

% Discretize true plant
sysc=ss(Ao,Bo,Co,Do,'inputdelay',0.5*Tsamp);
sysd=c2d(sysc,Tsamp,'zoh');
[Aod,Bod,Cd,Dd]=ssdata(sysd);

% Calculate equivalent plant+DSM current controller
C1=[1 0 0;
     0 1 0 ];
Ad=Aod-Bod*CBinv*CA*C1;
Bd=Bod*CBinv;

Cc_star=eye(size(Ch_star,1));
% Discretize and compute balanced realization of the controller
csysc=ss(Ch_star,Bh_star,Cc_star,zeros(size(Ch_star,1),size(Bh_star,2)));
[csysbc,Tbal]=ssbal(csysc);
csysd=c2d(csysbc,Tsamp,'zoh');
[Acon_d,Bcon_d,Ccon_d,Dcon_d]=ssdata(csysd);

% Form the augmented equivalent plant and the servo compensator
Ad_big=[Ad      zeros(size(Ad,1),size(Acon_d,2));
        -Bcon_d*Cd      Acon_d];
Bd_big=[Bd ; -Bcon_d*Dd];

% Define the weighting matrices
epsilon=1e-5;

state_W=0.05;      %WP
fund_servo_W=5e7;  %5e5;      %WS1
harm_servo_W=5e5;  %WH

Q1=state_W*eye(size(Ad,1));

Q2=eye(size(Acon_d,1));
Q2(1:2,:)=fund_servo_W*Q2(1:2,:);
Q2(3:8,:)=harm_servo_W*Q2(3:8,:);

Q=[ Q1      zeros(size(Ad,1),size(Acon_d,2));
    zeros(size(Acon_d,1),size(Ad,2))      Q2];

R=epsilon;

```

```

% Now perform the optimal calculations of the gains
[Kd,S,E]=dlqr(Ad_big,Bd_big,Q,R);
Kd=-Kd;

% Robust stability analysis for the 3-ph 4-wire inverter system:

% parameter definition, in per unit
B=0.6; % per-unit susceptance of load parallel inductor
YB=wfun*B; % convert into complement of inductance
YG=0.8; % load parallel resistor

Cnom=xCinv*wfun;
Lnom=xLinv/wfun;
Rnom=xRinv;

r_epsilon=0.01; % per-unit series resistance in the load inductive
branch, negligible

Ctol=0.06;
Ltol=0.15;
Rtol=0.5;
YBtol=1;
YGtol=1;

deltaR=xRinv*Rtol;
deltaYB=YB*YBtol;
deltaYG=YG*YGtol;

Ap= [ -YG/Cnom 1/Cnom -1/Cnom;
      -1/Lnom -Rnom/Lnom 0;
      % YB 0 0 ];
      YB 0 -r_epsilon*YB ];

Bp= [ 0 -Ctol 0 0 0 -deltaYG/Cnom;
      1/Lnom 0 -Ltol -deltaR/Lnom 0 0;
      0 0 0 0 0 deltaYB 0 ];

Cp= [ 1 0 0;
      0 1 0;
      YG 0 1;
      -YG/Cnom 1/Cnom -1/Cnom;
      -1/Lnom -Rnom/Lnom 0;
      0 1 0;
      1 0 0;
      1 0 0 ];

Dp= [ 0 0 0 0 0 0;
      0 0 0 0 0 0;
      0 0 0 0 0 deltaYG;
      0 -Ctol 0 0 0 -deltaYG/Cnom;
      1/Lnom 0 -Ltol -deltaR/Lnom 0 0;
      0 0 0 0 0 0;
      0 0 0 0 0 0;
      0 0 0 0 0 0 ];

sysp=ss(Ap,Bp,Cp,Dp); % the plant
sysp.inputdelay=[0.5*Tsamp zeros(1,5)]; % discrete time plant with
syspd=c2d(sysp,Tsamp,'zoh'); % discrete time plant with
input time delay

sysp_w=d2c(syspd,'tustin'); % continuous plant with input
time delay

```

```

[Ap_c,Bp_c,Cp_c,Dp_c]=ssdata(sysp_w);

dsm=pck(Asm,Bsm,Csm,Dsm); % see above for the definitions
of the ABCD

Aservo=[ Acon_d zeros(8,1);
         zeros(1,8) 0 ];

Bservo=[ Bcon_d zeros(8,3);
         zeros(1,3) 1 ];

Cservo=[ Kd(4:11) Kd(3) ];

Dservo=[ 0 Kd(1:2) 0 ];

servo=pck(Aservo,Bservo,Cservo,Dservo);
systemnames='dsm servo';
inputvar='[err; plant{3}]'; % plant{3} includes Vload, Iinv,
Iload
outputvar='[dsm]';
input_to_dsm='[servo; plant(1,2,3)]';
input_to_servo='[err; plant(1:2) ; dsm]';
sysoutname='Hcontrol_d';
cleanupsysic = 'yes';
sysic;

[Acontrol,Bcontrol,Ccontrol,Dcontrol]=unpck(Hcontrol_d);
sys_con_d=ss(Acontrol,Bcontrol,Ccontrol,Dcontrol,Tsamp);
sys_con_c=d2c(sys_con_d,'tustin'); % continuous
controller
[Acontrol,Bcontrol,Ccontrol,Dcontrol]=ssdata(sys_con_c);

plant_nom_w=pck(Ap_c,Bp_c,Cp_c,Dp_c);
controller_w=pck(Acontrol,Bcontrol,Ccontrol,Dcontrol);
systemnames='plant_nom_w controller_w';
inputvar='[vref ; w{5}]';
outputvar='[vref-plant_nom_w(1); plant_nom_w(4:8)]';
input_to_plant_nom_w='[controller_w; w(1:5)]';
input_to_controller_w='[vref-plant_nom_w(1);plant_nom_w(1:3)]';
sysoutname='clp_w';
cleanupsysic = 'yes';
sysic;

omega=logspace(-1,5,500);
clp_g=frsp(clp_w,omega);

clpstab_g=sel(clp_g,2:6,2:6);

figure(1)
for i=1:5
subplot(5,1,i)
vplot('liv,m',sel(clpstab_g,i,i));grid;zoom on;
ylabel(i, 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
end
xlabel('Frequency (rad/s)', 'FontName','times new roman', 'FontSize',
16);

%deltaset = [-1 0;-1 0;-1 0; 1 1; 1 1];
deltaset = [-1 0;-1 0;-1 0; -1 0; -1 0];
[bnds,dvec,sens,pvec] = mu(clpstab_g,deltaset);

```

```

figure(2)
vplot('liv,m',bnds);
grid
pert=dypert(pvec,deltaset,bnds);

%% Compute closed loop poles zero for different delta_L
delta_C=0;
delta_R=0;
delta_YB=0;
delta_YG=0;
%close(3)
figure(3)
hold on
for delta_L=-[0 0.5 1.0 1.5 2.0 2.5]
delta=[ delta_C 0 0 0 0 ;
        0 delta_L 0 0 0 ;
        0 0 delta_R 0 0 ;
        0 0 0 delta_YB 0 ;
        0 0 0 0 delta_YG ];
clp_delta=starp(clp_w,delta);
[Adelta,Bdelta,Cdelta,Ddelta]=unpck(clp_delta);
sys_delta=ss(Adelta,Bdelta,Cdelta,Ddelta);
pzmap(sys_delta);
title('Pole-zero map', 'FontName','times new roman', 'FontSize', 16);
ylabel('Imaginary axis', 'FontName','times new roman', 'FontSize', 16);
xlabel('Real axis', 'FontName','times new roman', 'FontSize', 16);
set(gca,'FontName','times new roman');
set(gca,'FontSize',16);
end

```

CHAPTER 6

EXPERIMENTAL SETUP RECONFIGURATION

The basic configuration of the dual ac-dc-ac power converter units is described in

Technical Report DESIGN AND IMPLEMENTATION OF EXPERIMENTAL TEST

BED FOR 5 KVA UNINTERRUPTIBLE POWER SUPPLY, authored by Dr. M.N.

Marwali and Prof. Keyhani, available at

<http://www.ece.osu.edu/ems/> with Serial Number TR036.

This chapter gives information about reconfiguring the setup for conducting tests on three-phase four-wire system test and grid-connected inverter test.

6.1 Reconfiguration for Three-Phase Four-Wire System Tests

Unit 1 (the left hand side unit connected to host PCs EMS06 and EMS07) has been upgraded allowing reconfiguration for the 4-wire tests.

When a four-wire test is conducted, the power connections on the measurement box can be reconfigured as shown below:

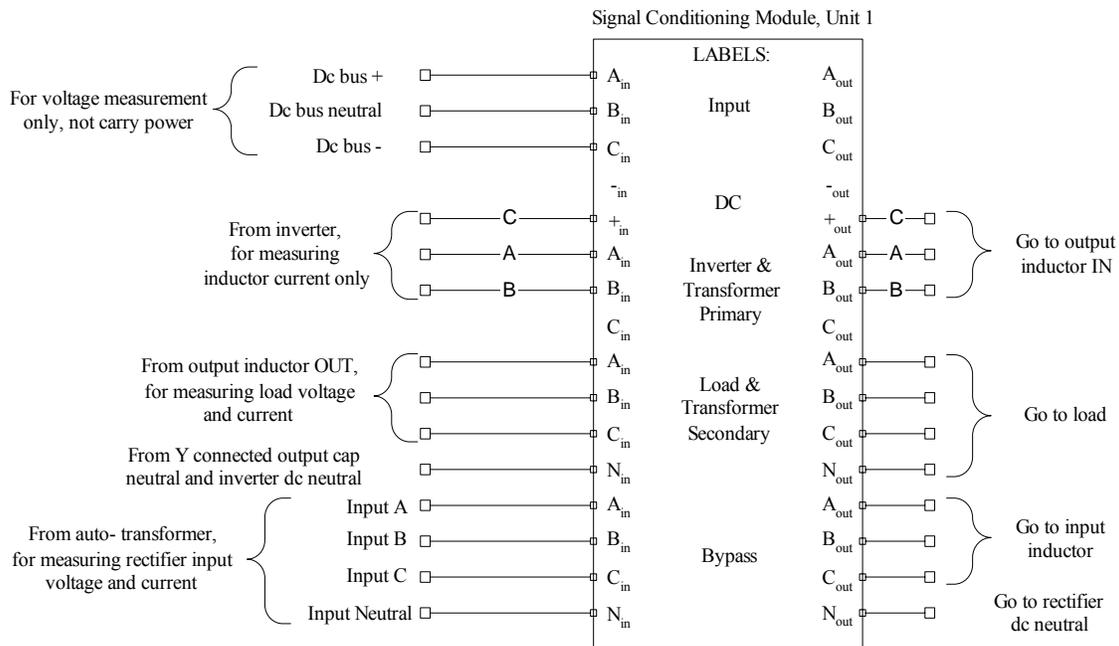


Figure 6.1: The power connection reconfiguration of the measurement box of Unit 1 for 3-phase 4-wire split dc bus ac-dc-ac system tests.

The upgrading is on the rectifier side signal conditioning board – three ac voltage measurement channels have been added (A, B, C, and N, four pins), i.e., popularized with components, to allow measurement of three-phase line-to-neutral voltage of the rectifier front end. The signal conditioning gain used is the “V240 Scale”, the same as the “INPUT” channels. On the rectifier side, the three-phase voltage sensing signals are

introduced out from the box through the 4-pin “Bypass” connector and sent to DSP through the “120VAC” connector, which actually allows 240V line-to-line voltage input. The current sensing signals (three-phase) come out from the box through “BYP A”, “BYP B”, and “BYP C” connectors (2-pin each) and enter the DSP through the “I load A”, “I load B”, and “I load C” connectors. On the rectifier side, the current sensing connectors “INP A” and “INP B” (2-pin each) on the signal conditioning board are not used in the 4-wire tests even though they are connected to the sensors inside the box.

One more voltage sensing connector labeled “INP (2)” (3-pin) has been added on the “Input” section of the box, combining the existing “INP” (3-pin) connector to send positive and negative halves of dc bus voltages to both the rectifier side signal conditioning board and the inverter side one. On the rectifier side board, the signals go to the “INP V” connector and on the inverter side board, the signals go to the “INV V” connector.

One current sensing connector labeled “Idc” (2-pin) has been introduced out from the “DC” section of the box, allowing current measurement on the “+in” to “+out” branch. This branch is used for measuring Phase C current of the inverter output filter inductor. This channel uses the “I Byp C” channel on the inverter side board to go to the DSP. Meanwhile, the sensor signals of Phases A and B of the inductor currents are introduced out from the box through the “Inv A” and “Inv B” connectors (2-pin each) and sent to DSP through the “I Inv A” and “I Inv B” channels.

The load voltage and current measurement follows the original configurations – load voltage connector (4-pin) from the box goes to the “Load” connector on the board and the load current connectors (3, 2-pin each) go to the three load current connectors on the board.

None of the “Vdc” connectors (2-pin each) on either board is used in the 4-wire tests.

6.2 Upgrading of Unit 2 for Grid-Connected Inverter Tests

Upgrading has been conducted on Unit 2 for grid-connected tests. Please refer to Figure 6.2 for the power stage connections on the measurement box. Notice that a 2nd contactor has been installed inside the box for the “Bypass” section to perform the ON/OFF switch between the unit and the utility grid. For protection purpose, three fuses have been installed on the “Bypass” branches. All other power connections are the same as the original UPS unit.

Due to the limit number of ADC channels on the TI 2407 DSP chips (16 channels), measured bypass current “I Byp B” and “I Byp C” on the inverter signal conditioning board are multiplexed to ADC channel 16. The DSP initialization sets the default ON signal to be “I Byp C”. In the control program, ADC channel 16 is read twice each control cycle, one for “I Byp B” and the other or “I Byp C”. Please refer to the code.

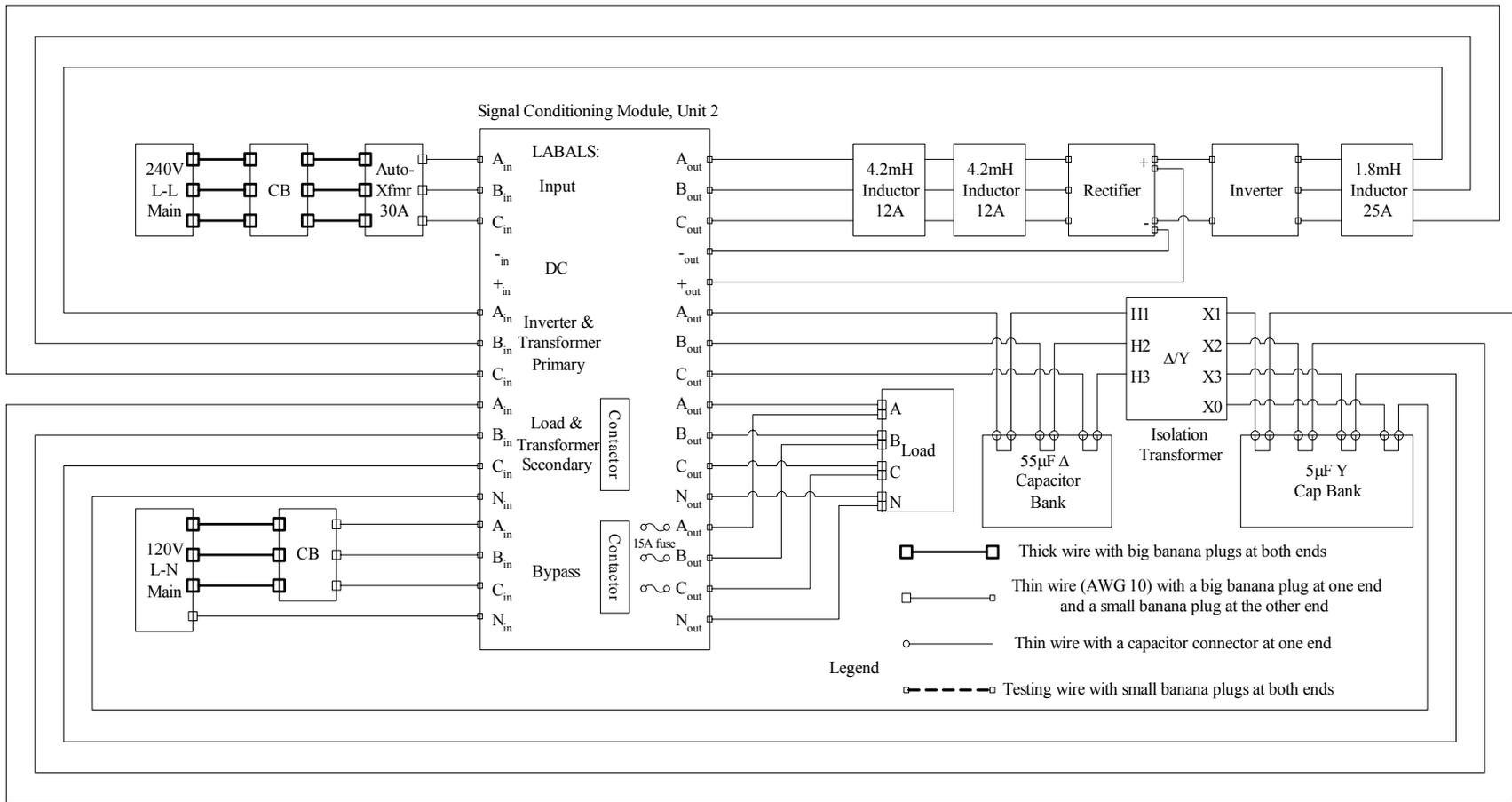


Figure 6.2: The power connection reconfiguration of the measurement box of Unit 2 for 3-phase 3-wire grid-connected inverter system tests.

6.3 The Contactor and Its Drive Circuit

The contactor is Omron® G7J-3A1B-BW-1-AC10012. It is driven by the following control circuit, where the AQH solid state optical relay is the key drive device:

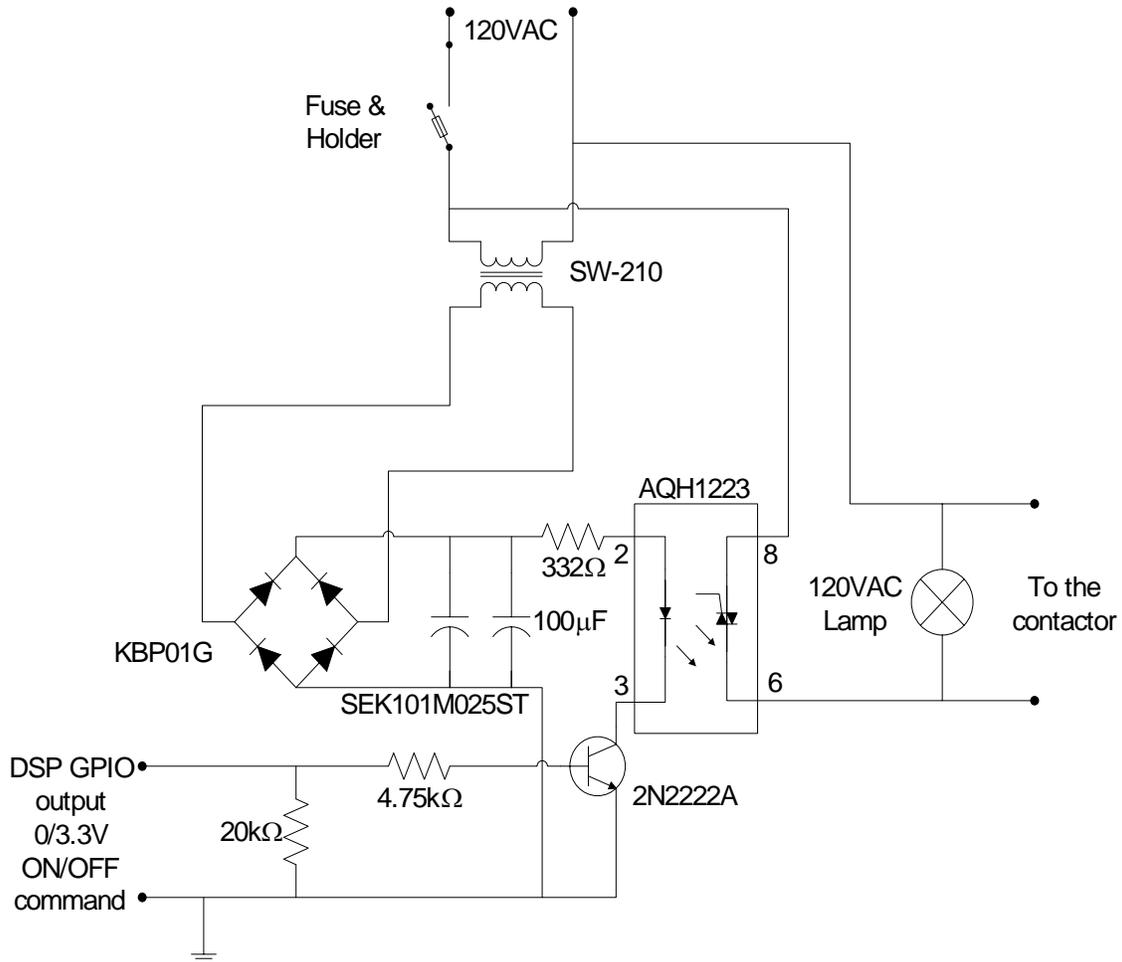


Figure 6.3: The 3-phase contactor drive circuit.

Order the parts from
<http://www.alliedelec.com/>

- 2N2222A: NPN transistor
- KBP01G: diode rectifier bridge
- LM7805CT: volt regulator, not used
- 17265: AC receptacle, not used
- AQH1223: opto coupler for contactor
- G7J-3A1B-BW-1-AC100120: The contactor
- SEK101M025ST: 100µF 25V electrolytic cap
- SW-210: 120V/5V transformer

Resistors as shown in the circuit: $\frac{1}{4}$ watt, 1%

Buy the following parts from Radioshack

A project box

A small general purpose PCB board

4 insulated PCB standoffs

1 fuse holder: $1\frac{1}{4}\times\frac{1}{4}$

1 250V 250mA fuse (fast)

1 120VAC lamp

6.4 The Dc Bus Overvoltage Protection Board Design

A dc bus overvoltage protection board has been designed to provide independent hardware protection on the boosted dc bus besides the rectifier DSP software overvoltage protection for both 3-wire and 4-wire split dc bus protection. The protection circuit detects overvoltage on both top and bottom halves of the dc bus where the neutral of the dc bus is available from the connecting point of the two series connected dc electrolytic capacitors supporting the dc voltage. Once overvoltage is detected on either half of the dc bus, two protective action will be tripped, rectifier PWM shut-down through PDPINTB and discharging of dc bus through a low induction regeneration resistor. The schematic of the protection circuit is shown below (3 pages in total). If the figures do not appear correctly, just print them out and they will appear correctly in hardcopy.

Page 211 shows the top and bottom half dc overvoltage detection circuit, including voltage divider, differential amplifier, and hysteresis comparator stages. The protection triggering thresholds are determined by the resistors used in these three stages. The hysteresis comparator is used to control the discharging branch to be ON when overvoltage is detected and OFF when the dc bus voltage drops below a certain voltage

(190 V for half dc bus). Turning OFF the discharging will stop the large current flow through R (low inductance power resistor – TL88K25R0 25Ω 114W) and let R1 and R2 (attached to the dc capacitors, 22k each) resume the discharging till the voltage drops to the uncontrolled rectifier level, for 3-ph 240V line-to-line input case, this voltage is $\sqrt{2} \times 240 = 340$ V for full dc bus, or say 170V half dc bus. This is used to protect R from heating up by long time conducting, assuming input ac voltage source is not removed. Page 212 shows on-board power management, opto-coupler isolation, and digital logic circuits. Page 213 shows board connectors. Figure 6.4 shows how to connect the board to the power stage, where the error signals Error 1 to 3 are three BNC connectors on the Semikron 3-ph power converter teaching unit. This allow the board also to respond to the error messages sent by the power converter, which will also trigger the PDPINTB and the discharging. The gain and hysteresis designs for are given in the two Matlab files – opamp_gain.m and opamp_calc.m.

There are two identical protection boards in total, one for each unit and sitting on top of the rectifier side signal conditioning board. In grid-connected operation or parallel operation of the units, if the PDPINTB signal on the protection board is introduced to the inverter side PDPINTB pin, the inverter PWM can be shutdown at dc bus overvoltage caused by real power pumped back from the inverter.

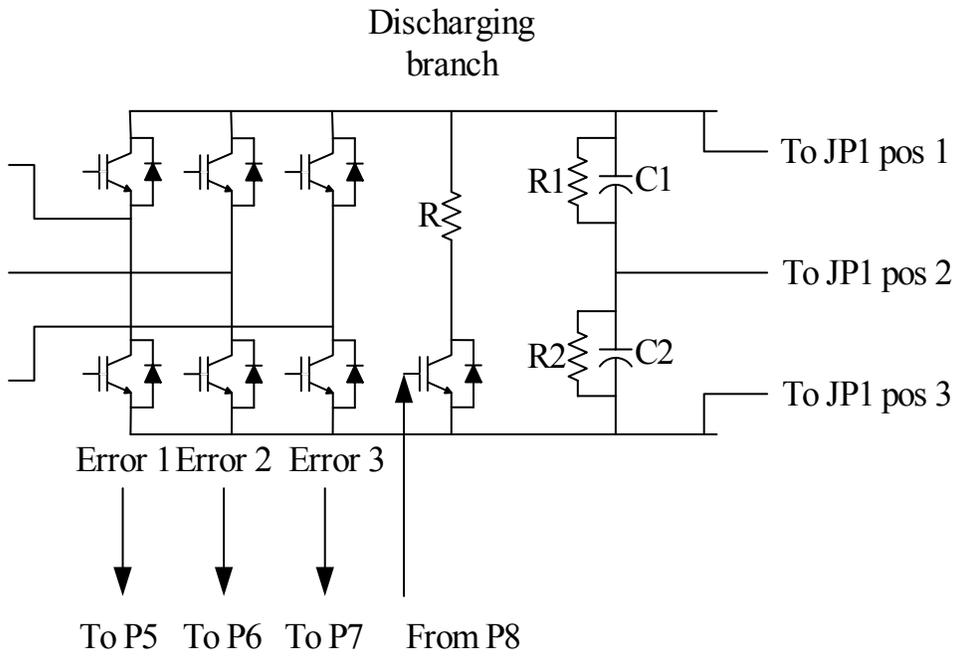
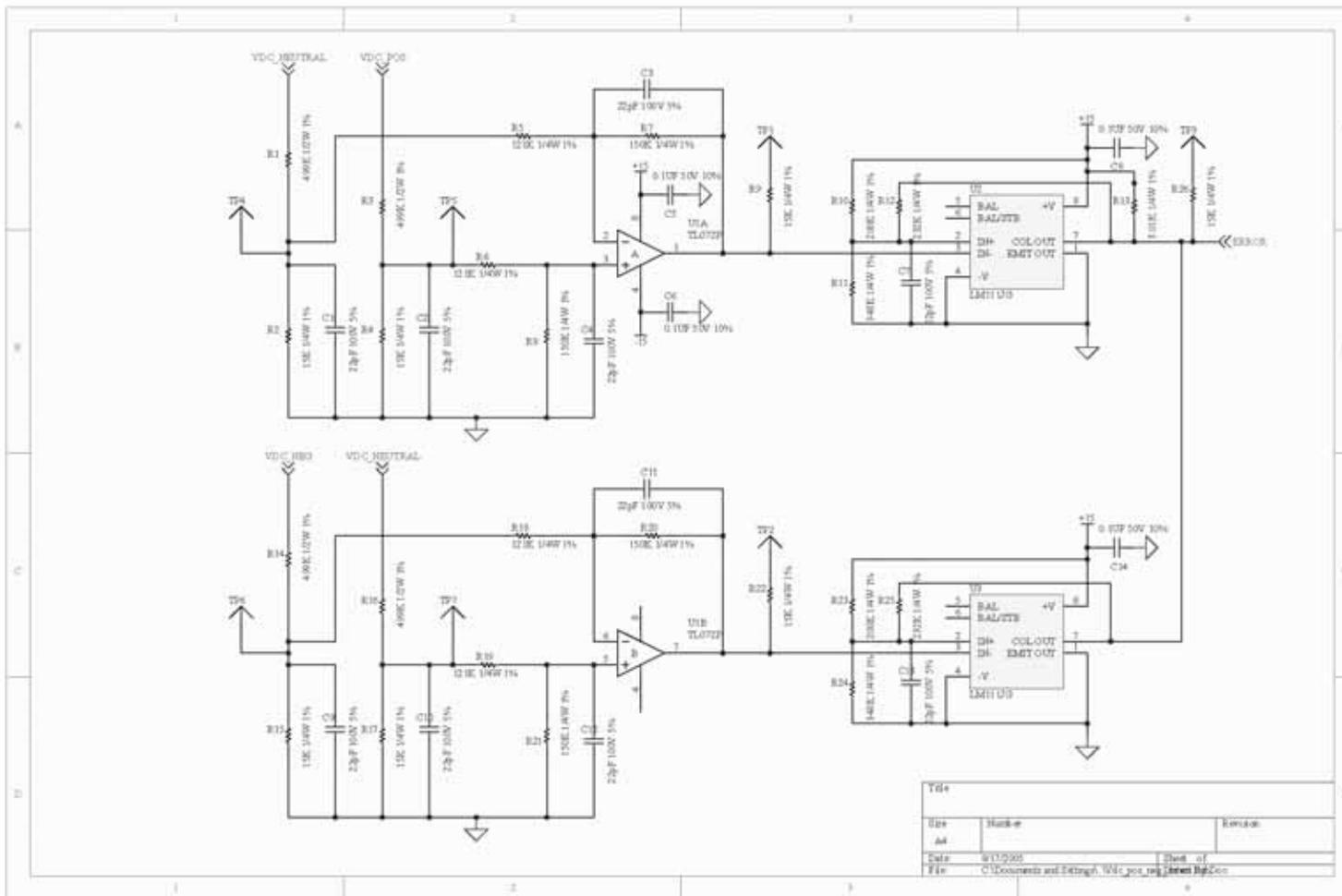
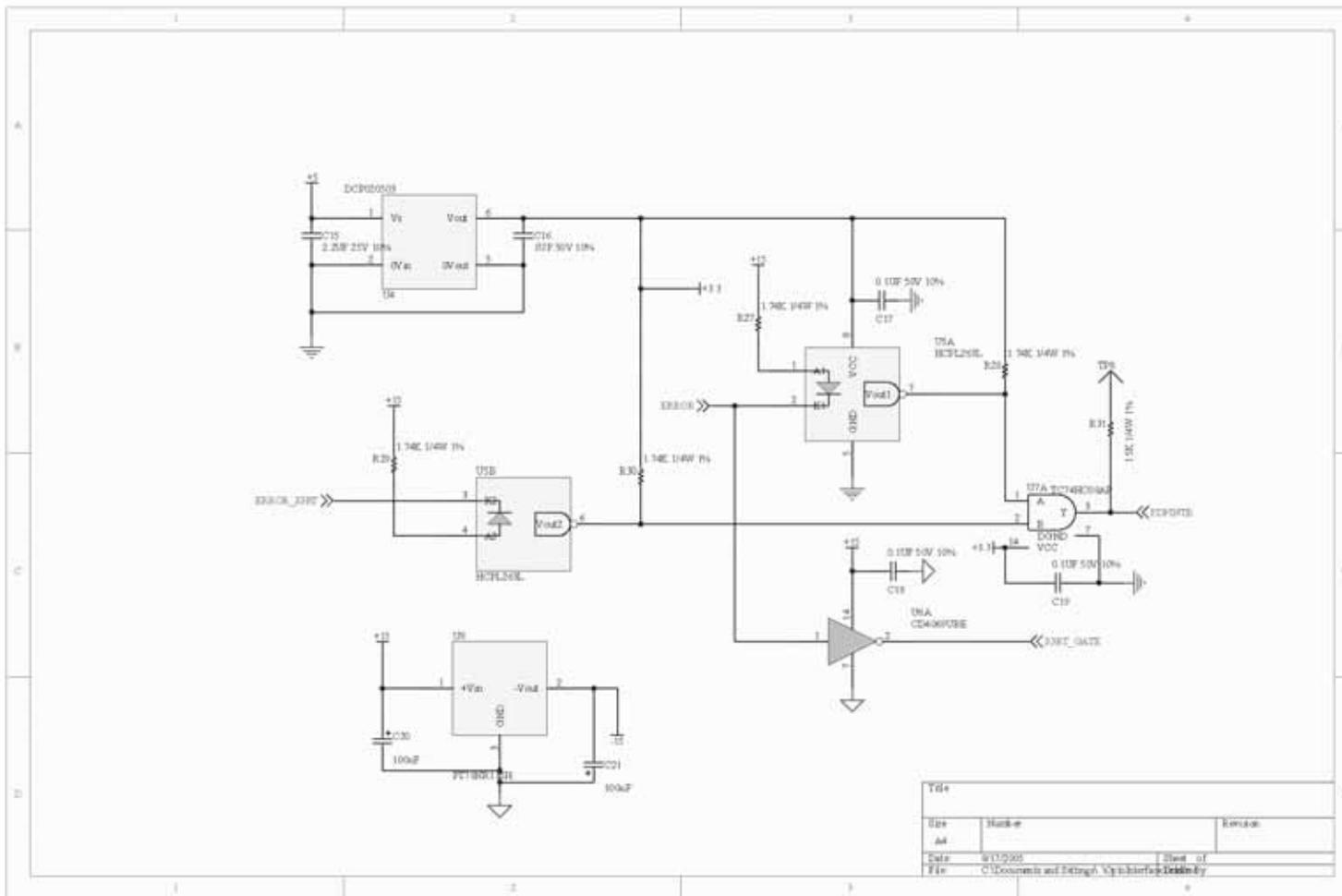
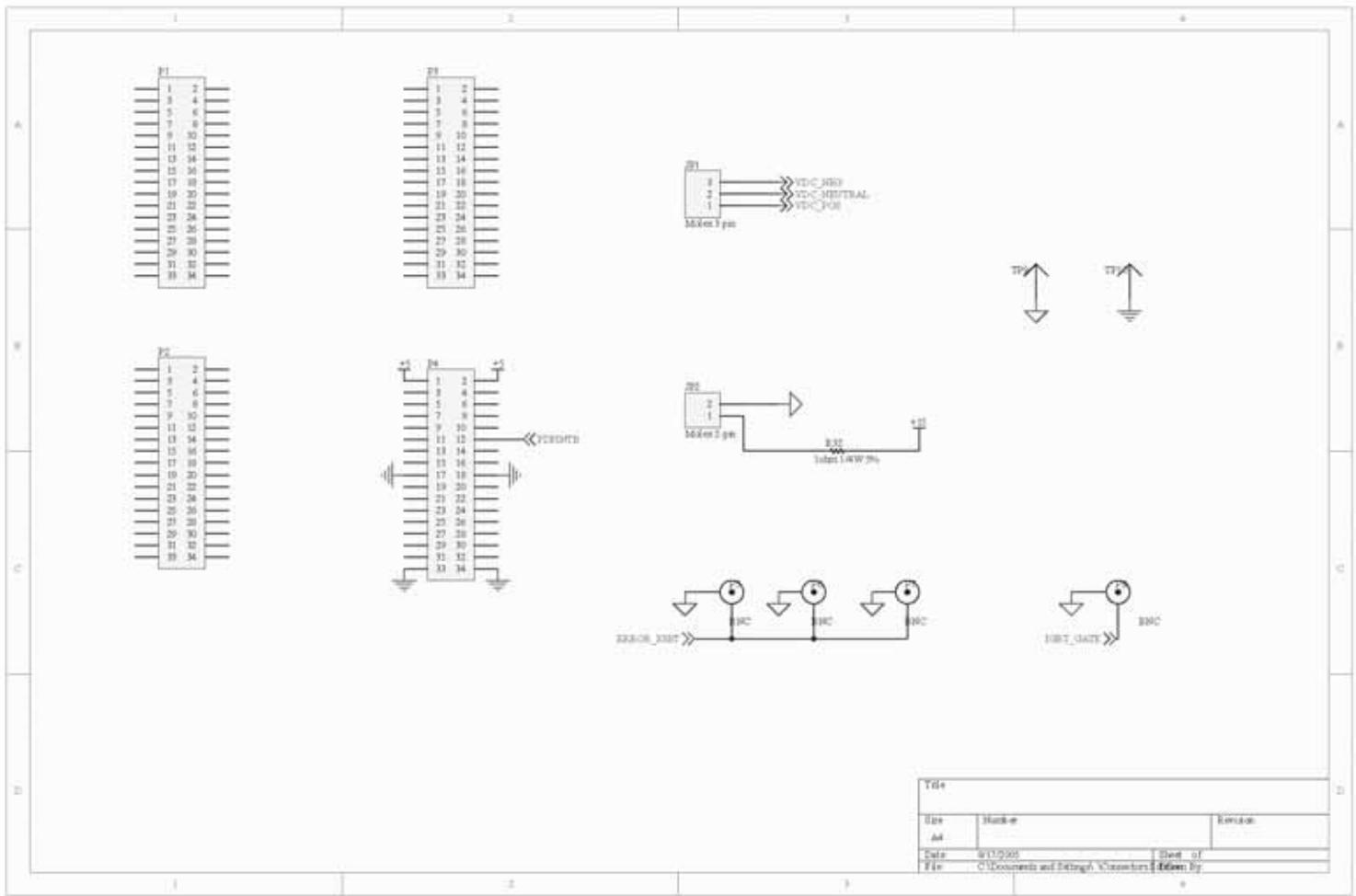


Figure 6.4: Connecting the protection board to the power stage.



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```

% opamp_gain.m
% Dc bus overvoltage protection circuit gain calculation - the opamp
% Only the differential gain considered, no common mode voltage
% considered, for common mode voltage verification, see opamp_calc.m

% Voltage divider and the OpAmp
R3=499e3;      % voltage divider top
R4=15e3;      % voltage divider bottom
R1=121e3;     % OpAmp input resistor
R2=150e3;     % OpAmp feedback and reference input resistor

Vin=170;

R34=R3*R4/(R3+R4);      % R3//R4

Vin_divided=R4/(R3+R4)*Vin
Vout=R4/(R3+R4)*R2/(R1+R34)*Vin
gain=R4/(R3+R4)*R2/(R1+R34)

gain_test=R2/R1      % ignore the voltage divider, test input signal
hooked              % to the differential amplifier directly

Vin1=0.5*Vin_divided
Vin2=-0.5*Vin_divided
V_neg=Vin2-(Vin2-Vout)*(R1+R34)/(R1+R34+R2)      % OpAmp neg pin voltage
V_pos=R2*Vin1/(R1+R34+R2)      % OpAmp pos pin voltage

R3_pwr=Vin^2/R3
R4_pwr=Vin_divided^2/R4

% The hysteresis comparator
Vin_th_hi=350;      % protection threshold voltage, turn on
discharging path
Vin_th_lo=190;      % turn off discharge path

Vth_exp_hi=Vin_th_hi*gain
Vth_exp_lo=Vin_th_lo*gain

R5=200e3;      % comparator reference voltage divider top
R6=348e3;      % comparator reference voltage divider bottom
R7=232e3;      % comparator feedback voltage (to cause
hysteresis)
R8=3.01e3;      % comparator collector out to Vcc resistor

R578=R5*(R7+R8)/(R5+R7+R8);      % R5//(R7+R8)
R67=R6*R7/(R6+R7);      % R6//R7

Vcc=15;
Vth_hi=R6/(R6+R578)*Vcc
Vth_lo=R67/(R5+R67)*Vcc

Vin_th_hi_cal=Vth_hi/gain
Vin_th_lo_cal=Vth_lo/gain

```

```

Vin_test_hi_cal=Vth_hi/gain_test
Vin_test_lo_cal=Vth_lo/gain_test

Vout_hi=(Vcc-Vth_hi)*R7/(R7+R8)+Vth_hi

R8_pwr=Vcc^2/R8

% opamp_calc.m
% Common mode input voltages are considered
% a complementary consideration on top of the differential-gain-only
% design in opamp_gain.m

format long

% protection circuit parameters
R1=499e3;
R2=15e3;
R3=121e3;
R4=150e3;
Vin_neg=-308;
Vin_pos=25;

R_pos=R2*(R3+R4)/(R2+R3+R4) % R2/(R3+R4)

V_pos=Vin_pos*R_pos/(R1+R_pos)

V_opamp_pos=V_pos*R4/(R3+R4)

V_opamp_neg=V_opamp_pos % virtual short

V_neg=(R1*R2*V_opamp_neg+R2*R3*Vin_neg)/(R1*R2+R2*R3+R3*R1)

Vout_calcA=(V_opamp_neg-V_neg)*R4/R3+V_opamp_neg

V_diff=V_pos-V_neg

gain_diff=R4/R3;
Vout_calcB=V_diff*gain_diff

gain=Vout_calcA/(Vin_pos-Vin_neg)

```

CHAPTER 7

ELECTRONIC FILES

Electronic files attached to this report include:

Simulink models of the three-phase four-wire ac-dc-ac system control on passive load and power flow of three-phase three-wire grid-connected inverter system plus associated initialization Matlab M-files.

TI TMS320LF2407(A) DSP source code for three-phase four-wire ac-dc-ac system control. The source code for three-phase three-wire front-end rectifier control.

CHAPTER 8

CONCLUSIONS

8.1 Summary of Report

In this report, control problems in three major aspects of DG unit operation, including the single inverter unit voltage and current control in island mode, single unit power flow control in grid-connected mode, and front-end PFC rectifier control under unbalanced inverter load, have been discussed. In each topic addressed in the report, the background, the problem, and existing solutions are always presented and discussed followed by proposing a new approach which yields better performance or solves the problem. Theoretical derivations, analysis, computer simulations, and experimental tests have been practiced in the covered research to generate the results serving the purpose of the research. The entire report can be summarized as follows.

In the research on the control of three-phase four-wire inverter unit with a split dc bus topology for island applications, a new control technique has been proposed. This technique is a combination of discrete-time sliding mode control (DSMC) and robust servomechanism control (RSC). The development of the control algorithm have been presented based on a one dimensional equivalent circuit model of the system in stationary $\alpha\beta 0$ reference frame and per-unit values.

A modified space vector PWM technique, i.e., the MSVPWM, has been proposed to perform three dimensional control on an $\alpha\beta 0$ basis. The pulse duration algorithm yielding higher priority on the non-zero-axis dimensions, i.e., α and β , under limited dc bus voltage has been presented. Simulation comparison has shown the advantage of this approach over the conventional sine wave PWM in the ABC reference frame. A series of analysis and studies have been performed on the proposed control technique, including the $L-C$ filter design issue, closed-current-loop and closed-voltage-loop responses, and time domain simulations and experiments under various load scenarios. All these analysis, simulations, and experiments have demonstrated the effectiveness of the proposed control solution.

The robust stability of the proposed solution in existence of linear load disturbances and parametric uncertainty has been verified structured singular value based method. It has been shown that the weight adjustment in the optimal control performance index provides a way of tuning the transient performance of the controller while maintaining stability robustness of the system under perturbations.

In the research on power flow control of a DG unit in grid-connected mode, a power flow control approach has been presented for a three-phase three-wire topology with isolation transformer while connected to utility grid with a local load. The proposed control technique is based on a robust servomechanism voltage controller and a discrete-time sliding mode current controller. In order to obtain the parameters of the utility grid and use the information to generate feedforward control of power flow, a Newton-Raphson Method based parameter estimation and feedforward control

technique have been developed and combined with traditional integral power control. The stability of the power control loop has been proved using Lyapunov direct method. A harmonic power control technique based on PLL have been proposed to handle harmonic distorted utility grid voltage and yield harmonic free line current. Both simulation and experimental results under various scenarios have demonstrated the effectiveness of the proposed technique in power regulation and line current conditioning.

In the research of the front-end PFC rectifier control, a new control technique has been proposed for the PWM rectifier in standard three-wire rectifier-inverter systems to achieve decoupling between the converters with the capacitive dc link under unbalanced three-phase inverter load. Analytical work has been conducted to disclose the mechanism how the inverter load unbalancing affects the control of the front-end rectifier. On basis of the analysis, a notch filter is then designed and utilized in the voltage loop to suppress the undesired 2nd harmonic component in the dc link voltage feedback, which implements the power decoupling between the rectifier and the inverter and yields balanced input current and does not undermine the dynamic response of dc bus voltage regulation. The effectiveness of the proposed control technique has been demonstrated by both simulations and experimental tests.

The supporting materials associated to the research are included in Chapter 5-7.

The major contributions of this report research include

1. Have successfully applied the RSC plus DSMC technique to a three-phase four-wire topology with split dc bus. Have proposed the MSVPWM technique in the four-wire inverter control and demonstrated its advantage over the conventional sine wave PWM.
2. Have proposed and successfully implemented Newton-Raphson power system parameter identifying and feedforward control technique in real-time operation. Have developed a harmonic power controller to handle the harmonic distorted utility grid voltage.
3. For better PFC performance, a front-end rectifier control philosophy has been proposed and practiced that the instantaneous power unbalance between the front-end rectifier and the output inverter can be buffered out by the dc bus capacitor. Instantaneous power balance cannot be practiced in this case from the PFC point of view. A mathematical analysis have been performed to disclose the relation of load unbalancing and dc bus pulsating voltage.

8.2 Future Work

Based on the studies reported in this report, some interesting closely related topics warrant further investigation. They are suggested as follows:

1. To improve the experimental control performance of the three-phase four-wire split dc bus inverter by increasing the switching frequency and decreasing the filter inductance while maintaining stability. Suggested measures include using faster DSP, optimizing the control code, and improving control instrumentation.
2. To study control of three-phase four-leg inverters and take advantage of its property of rejecting 0-axis current.
3. To study power flow control of DG unit in grid-connected mode via single-loop current mode control, which differs from the three-loop approach discussed in this report.
4. To study parallel operation of multiple DG units. To study front-end PFC rectifier control using a Vienner rectifier topology.
5. To study Z-source inverters.
6. To use more advanced methods in the studies. Beyond typically used time-domain simulation and experimental test, more analytical tools can be applied in studying systems, e.g., large and small signal analysis in frequency domain, robust stability as well as robust performance, loop shaping techniques, system identification theory, etc.

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