EE682
Fuel Cell Energy Processing Systems
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Class Notes: Single-Phase Inverter Design

Fuel Cells

DC/DC Converters

Inverters

Mechatronics Laboratory

Department of Electrical Engineering

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CHAPTER 6 Single Phase Inverter Design Example

In this chapter, basic inverter architectures and waveforms will be introduced as an overview. Detailed design procedures will be described through a practical inverter design example assuming typical laboratory conditions.

6.1 Inverter architectures

When designing an inverter there are three basic schemes to convert the fuel cell plus boost module's DC energy into AC. For example, this AC may then be fed into the grid or can be used for stand-alone operation of 230V appliances. (The European wall outlets give 230V, but there is no principle difference for the USA at 120V.) In this section, these basic architectures will be introduced in an abstract level or overview level before detailed circuit design is involved.

6.1.1 First type inverter: step-up and chop

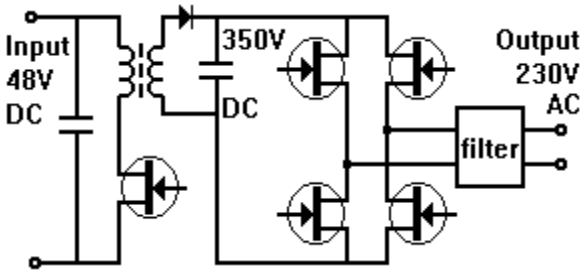


Figure 6-1 Circuit topology of a step-up and chop inverter

This type converts the low voltage into a high voltage first with a square-wave step-up converter and then converts the high-voltage DC into the wanted AC waveform. (for waveforms: see Section 6.2)

Advantage of this architecture: insulation between input and output, easy dimensioning of the input converter, therefore it is often used in small and cheap square-wave inverters. Efficiency may be up to 95% for square-wave, slightly lower for sine-wave inverters.

6.1.2 Second type inverter: High voltage in, only chop

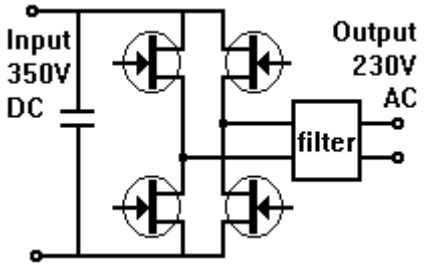


Figure 6-2 Circuit topology of a high voltage in and chop only inverter

This type requires the input voltage to be higher than the output voltage and converts it directly into the wanted AC waveform. (for waveforms: see Section 6.2) The advantage of this is the high efficiency of the inverter, typical 96%. The main disadvantage is the lack of insulation between the Solar modules and the grid voltages. Also the input voltages always require a large number of modules.

6.1.3 Third type inverter: chop and transform

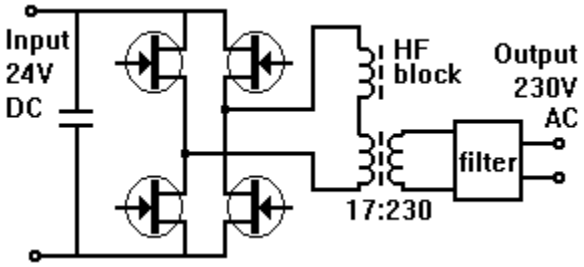
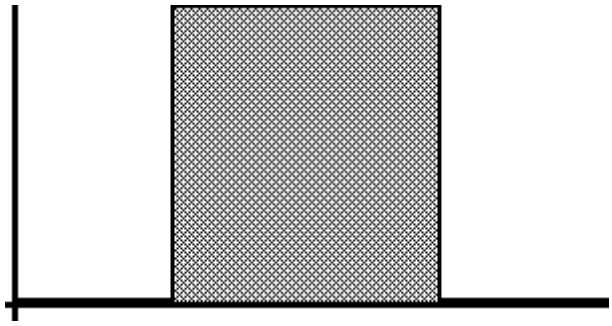


Figure 6-3 Circuit topology of a chop and transform inverter

This type converts the low voltage DC into a low voltage AC first and then converts the low-voltage AC into the wanted AC voltage. This is the architecture I chose for my inverter. The advantages are the low-voltage (=safe) operation, the insulation from the grid after the inverter, the ease with which it makes sine-wave which feeds into the transformer and the most important in many aspects: reliability due to the low number of semiconductors in the power path. Disadvantage is the slightly lower efficiency of the inverter, typically 92%. Also some hum can be generated by the transformer under load.

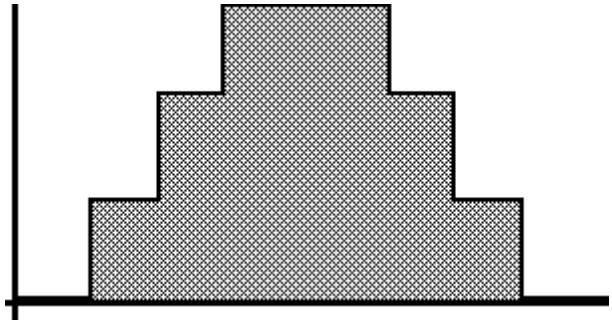
6.2 Output Waveforms

6.2.1 First waveform: square wave



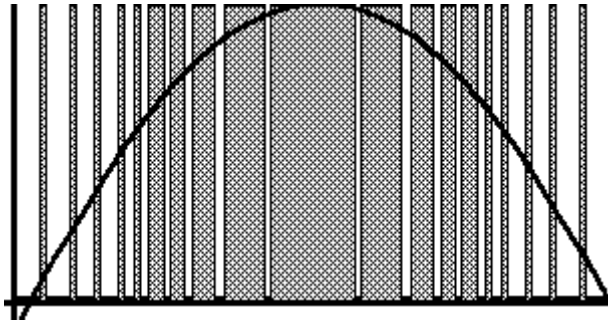
This is the form of the output voltage from a cheap inverter. Basically it switches its output on and off. This is no problem for heaters and light bulbs, but electronic equipment always has a power supply with a capacitor for energy storage. During the steep rise of voltage in a square-wave, the input current to charge the capacitor will destroy the power supply components.

6.2.2 Second waveform: modified square wave



To combat the problems with square wave there have been several changes, one is depicted here: the voltage rises in smaller steps, keeping the current more within rated limits and more closely approximating the sine wave form. Other approaches have added filters to square wave outputs, to make the rising and falling edge less steep (more trapezium-shape). Still electronic equipment will not work properly or get too hot on these types of signals.

6.2.3 Third waveform: sine wave



The waveform shown here is a good approximation of a sine wave, all type of equipment will run on this signal. The sine wave is approximated by a high-frequency chopping plus filtering (note that the chopping frequency is much higher than depicted here for readability: typically 10kHz). This chopping is also known as PWM (Pulse Width Modulation). This is the only waveform allowed to be grid-connected, when the inverter is capable of synchronization to the grid.

6.3 Inverter design example

In this section, a complete design process will be illustrated through a practical design example. This example is designed for implementation under laboratory conditions.

6.3.1 Design requirement

Design a PWM inverter with a rectified DC bus to output 6-volt (RMS) 6-watt 60Hz single phase AC power under resistive load. The input should be regular 120V AC grid power. The PWM should be implemented using Texas Instruments TMS320F240 Evaluation Module (EVM).

The design procedures will be discussed in the following subsections.

6.3.2 Circuit topologies

According to the system requirement, i.e., 120V input and 6V output, the main circuit can consist of a step-down transformer, a DC bus, and a chop-only (6.1.2) inverter. For a chop-only inverter, one circuit topology is shown in Figure 6-2. An alternative topology is shown in Figure 6-4.

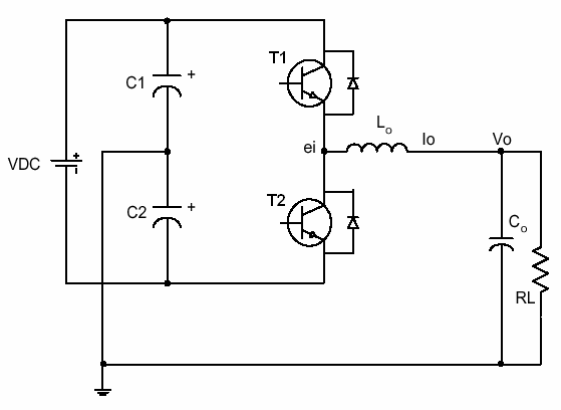


Figure 6-4 Alternative topology for a single phase inverter

The differences between the two are: the former has 4 controlled switches and the latter has only 2; the DC bus of the latter must be twice as much as that of the former; the voltage rating of the power switches in the latter circuit must be twice as much as that in the former circuit. Due to the low output voltage and power, the voltage rating of a power switch does not affect its cost and volume significantly, while less number of power switches leads to simpler control, higher reliability, and lower overall cost (not true for high voltage applications). Therefore, the latter topology (Figure 6-4) is chosen as the solution.

The overall system is shown in Figure 6-5.

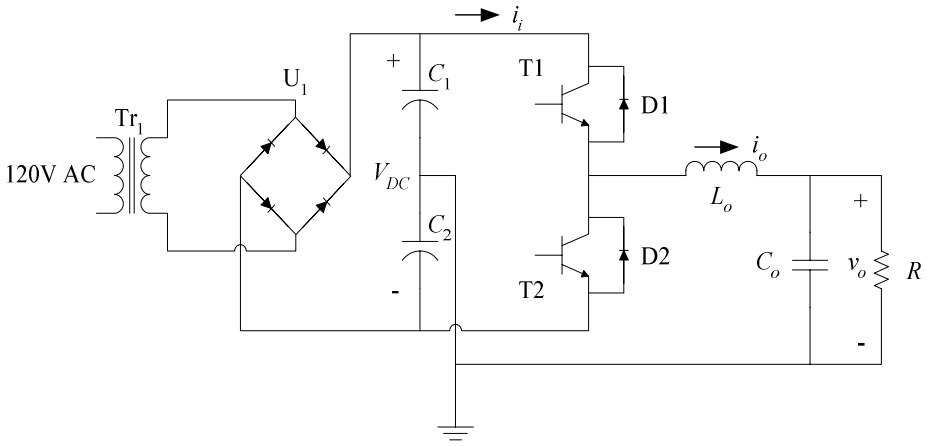


Figure 6-5 Single phase inverter topology

6.3.3 Power switch selection

Current and voltage ratings of T1 and T2 are the first factors to be determined. The system output current requirement is 1A. Considering some safety margin, switching devices rated at 1.5~3A would be proper selections for current rating. As for voltage rating, the DC bus voltage has to be determined first.

Assuming sine-triangle PWM and linear modulation (refer to Chapter 3), and considering the different circuit architecture in this design (double DC bus voltage), the DC bus voltage in this design should be

$$V_{DC} \geq 2\sqrt{2}V_{1RMS} = 2 \times \sqrt{2} \times 6\text{V} = 16.97\text{V}$$

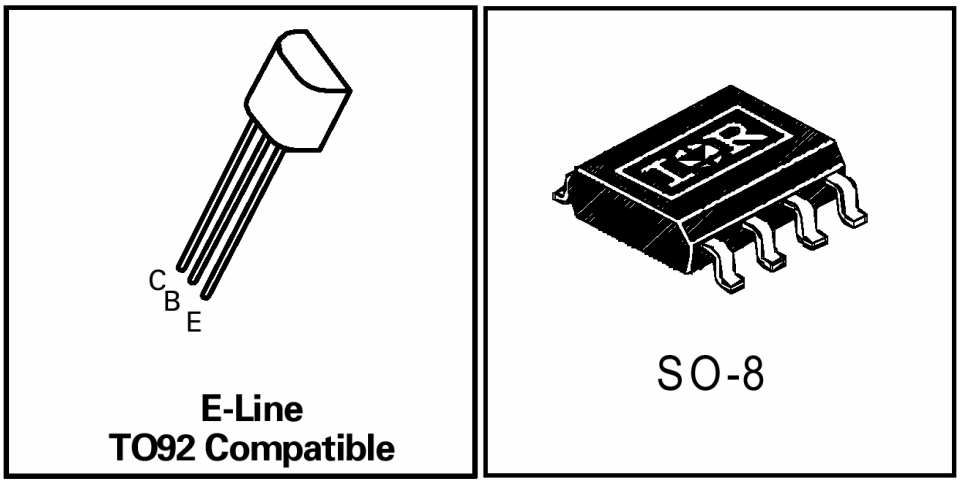
Similarly, the DC bus voltage can be chosen to be 20~30V with some safety margin considered. Due to the switching operation, the single switching device should be able to block voltage as high as V_{DC}.

From the control point of view, higher DC bus voltage provides more control force and faster transients although the inverter design itself does not involve any control. Therefore, 30V is chosen as the DC bus voltage and the switching devices must be able to block 30V at OFF state.

One BJT and one power MOSFET are picked up as candidates. There characteristics are listed below:

The BJT, ZTX1053A from ZETEX, costs $1.14 each from Digikey.com. Its maximum collector-emitter voltage at OFF state is $V_{CEO(max)}$=75V; its maximum collector current is $I_{C(max)}$=3A; and its required base drive current is at lease 10mA at $I_{C(max)}$=1A and its saturated collector-emitter voltage is 150mV. Its package is TO92 as shown in Figure 6-6(A). Its turn-on time is 90ns and turn-off time is 750ns.

The MOSFET, IRF7103 from International Rectifier, costs $1.04 for each chip (dual channel) from Digikey.com. Its maximum drain-source voltage is $V_{DSS(max)}$=50V; its maximum drain current is $I_{D(max)}$=3A; and its threshold gate drive voltage is $V_{GS(th)}$=3.0V. Its drain-to-source ON voltage is about 100mV at V_{GS}=10V and I_D=1A. Its package is SO-8 (surface mount) as shown in Figure 6-6(B). Its rise time is 20ns and fall time is 50ns.



(A) ZTX1503A (B) IRF7103

Figure 6-6 Packages of the power switches

According to the above data, the power MOSFET is better than the BJT although the surface mounting is more difficult for laboratory implementation (still doable). Therefore, the power MOSFET IRF7103 is chosen to be the power switch.

The following is the loss and thermal calculation for IRF7103.

Assuming 10kHz switching frequency, the switching loss can be calculated as follows:

$$P_{loss} = \frac{W_{loss}}{T} = \frac{1}{T}\left(W_{loss\_ON} + W_{loss\_OFF}\right) = \frac{V_{ds} I_d}{2T}\left(t_{ON} + t_{OFF}\right)$$
$$= \frac{30 \times 1}{2 \times \frac{1}{10 \times 10^3}}\left(20 + 50\right) \times 10^{-9} = 0.0105\text{W}$$

Assuming average 50% duty ratio at full (1A) load, the ON-state loss can be calculated as follows:

$$P_{ON\_loss} = \frac{W_{ON\_loss}}{T} = \frac{1}{T}\left(V_{DS(ON)} I_D \frac{T}{2}\right) = \frac{1}{2} \times 0.1 \times 1 = 0.05\text{W}$$

Therefore the overall loss P_{loss}= P_{SW_loss} + P_{ON_loss} =0.0605W<P_D=2.0W, where P_D is the heat dissipation capacity of the MOSFET. From the data sheet, the maximum thermal resistance from junction-to-sink is 3.3°C/W. Therefore, the maximum junction-to-ambient temperature different is

$$\Delta T_{ja} = R_{\theta ja} \times P_{loss} = 62.5^\circ \text{C/W} \times 0.0605\text{W} = 3.78^\circ \text{C}$$

According to the data sheet, the maximum operating temperature is T_{jmax}=150°C. Therefore, the MOSFET will be safe. Assuming 50% duty ratio, the transient thermal behavior can be calculated based on the normalized maximum transient thermal impedance in Figure 6-7 (the top curve):

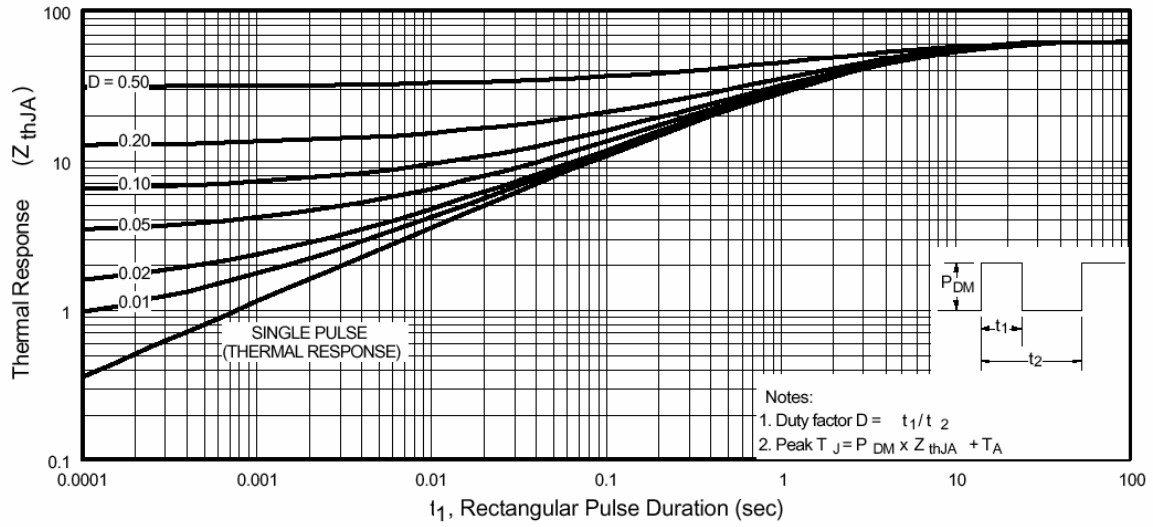


Figure 6-7 Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

$$\Delta T_{JC}(t) = P_{loss} Z_{\theta JC(50\%)}(t)$$

$$\Delta T_{JC}(100\mu s) = P_{loss} Z_{\theta JC(50\%)}(100\mu s) = 0.0605\text{W} \times 30^\circ \text{C/W} = 1.815^\circ \text{C}$$

$$\Delta T_{JC}(1ms) = P_{loss} Z_{\theta JC(50\%)}(1ms) = 0.0605\text{W} \times 31^\circ \text{C/W} = 1.8755^\circ \text{C}$$

$$\Delta T_{JC}(10ms) = P_{loss} Z_{\theta JC(50\%)}(10ms) = 0.0605\text{W} \times 32^\circ \text{C/W} = 1.936^\circ \text{C}$$

$$\Delta T_{JC}(100ms) = P_{loss} Z_{\theta JC(50\%)}(100ms) = 0.0605\text{W} \times 37^\circ \text{C/W} = 2.2385^\circ \text{C}$$

$$\Delta T_{JC}(1s) = P_{loss} Z_{\theta JC(50\%)}(1s) = 0.0605\text{W} \times 46^\circ \text{C/W} = 2.783^\circ \text{C}$$

$$\Delta T_{JC}(10s) = P_{loss} Z_{\theta JC(50\%)}(10s) = 0.0605\text{W} \times 62.5^\circ \text{C/W} = 3.78^\circ \text{C} = \Delta T_{JC}(\infty)$$

Two free wheeling diodes are needed to be used together with the power MOSFETs. It should meet the 3A current and 30V voltage requirements too. Therefore, a

General Semiconductor product 1N5400, which costs $0.32 each from Digikey.com can be used. It is rated at 3A and 50V which meet the requirements.

6.3.4 Filter design

A second order L-C passive filter is used at the output stage. The cut-off frequency should be a little higher than 60Hz. The cut-off frequency of a second order L-C filter is determined by

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

Since there are enough number of GE capacitors rated at 120μF, 220VAC, and 60Hz available in the lab, only the inductor needs to be selected. If an AC reactor of 33.6mH is chosen, the cut-off frequency f_c will be 79.3Hz, which is good for this system. A product of MTE corporation, RL-01203, which costs $136.03 each, is rated at 4.2mH and 12A. It is designed for 3-phase but can be used for single phase. 8 coils connected in series make the total inductance to be 33.6mH.

6.3.5 Input stage design

The input stage in Figure 6-5 contains a step-down transformer, a full wave rectifier, and two identical filter capacitors C_1 and C_2. Redraw this part in Figure 6-8 below, where $C= C_1C_2/(C_1+C_2)$ and R is the equivalent load resistance.

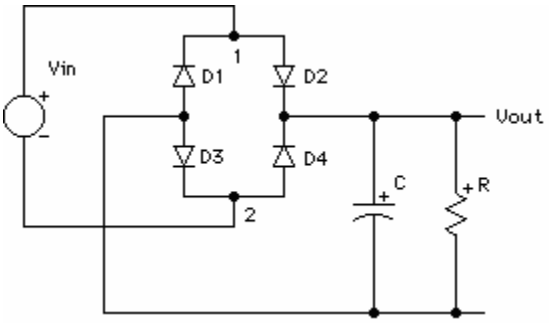


Figure 6-8 Full wave rectifier with equivalent load R

The DC bus voltage (V_{out}) and the voltage ripple are mainly dependent on the capacitors and the equivalent load resistance. To describe the source of the voltage ripple, consider the performance of the filtered full wave rectifier. The input to the rectifier is a sine wave of frequency *f*. Let V_i be the full wave rectified signal input to the filter stage of the rectifier and V_o be the output. V_i can be approximated as the absolute value of the rectifier input, with frequency 2*f*.

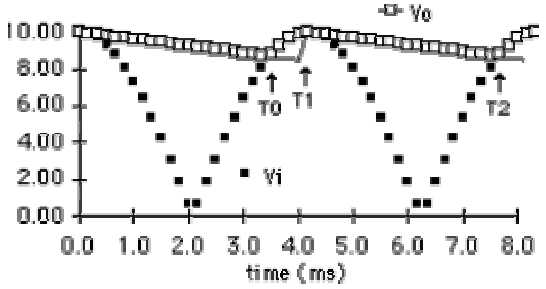


Figure 6-9 DC bus voltage V_o of a filtered full wave rectifier

In the time period from T_0 to T_1, the diode D1+D4 (or D2+D3, depending on the phase of the signal) are forward biased since $V_i > V_{out}$ (approximate the forward biased diode as a short circuit). The capacitor C charges and the voltage across the load R increases. From T_1 to T_2, the diodes are reverse biased (open circuit) because $V_{out} > Vi$, and the capacitor discharges through the load R with a time constant of RC seconds.

The voltages between times T_1 and T_2 lie along a capacitor discharge curve. Along this line,

$$V_{out} = V_{in(peak)} e^{-\frac{T-T_1}{RC}}$$

Since the desired DC bus voltage is 30V. Assuming small T_1, the average output DC voltage

$$V_{out} \approx V_{in(peak)} e^{-\frac{T}{RC}} = \sqrt{2} V_{in(RMS)} e^{-\frac{T}{RC}}$$

For a 6-watt and 30-volt DC link, the equivalent load resistance is $R= V^2/P=30^2/6=150\Omega$. As for the DC link filter capacitors C1 and C2 in Figure 6-5, there are used capacitors available in the lab – electrolytic capacitors 250V 1800μF. Please notice that if two of

them are connected in series, the overall capacitance C (in Figure 6-8) will be reduced to half - 900μF. Since the frequency is doubled to 2*f*, the period T=1/2*f*=0.008333s. With V_{out}=30V, it can be calculated that

$$V_{in(RMS)} \approx \frac{30}{\sqrt{2}\times 0.94}\text{V} = 22.6\text{V}$$

A Tamura product, 3FD-548, rated at 115V/24V at 0.5A, therefore can be used. It costs $10.76 from Digikey.com.

With above design, the peak-to-peak voltage ripple on the DC bus can be calculated:

$$V_{r(p-p)} \approx \frac{V}{2fRC} = \frac{30}{2\times 60\times 150\times 900\times 10^{-6}}\text{V} = 1.85\text{V}$$

which is acceptable.

For the full wave rectifier bridge, a General Semiconductor product, 3N253, rated at 50V and 2A, can be used.

6.3.6 Gate drive design

A TI TMS320F240 EVM is used to drive the power switches T1 and T2. Two PWM signals need to be generated by the DSP. However, the DSP output signal cannot directly used to drive the gates because of the limited voltage/current capability of the DSP output pins and the safety concerns. It is desired to isolate the low power circuit from the high power circuit electrically. Therefore, an optocoupler must be used.

If an HP HCPL-2232 optocoupler is chosen, the interface circuit can be designed as shown in Figure 6-10.

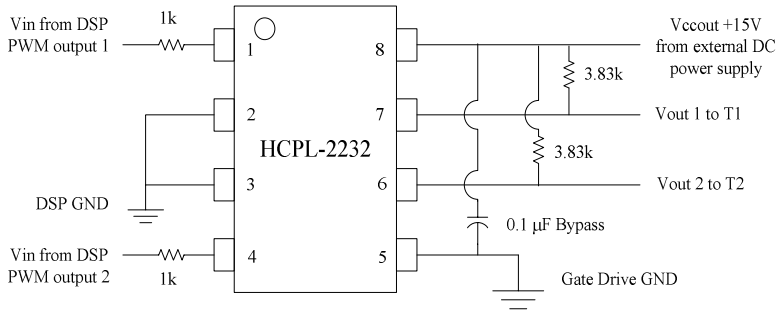


Figure 6-10 Gate drive circuit for T1 and T2

Select input resistor R_{in}=1kΩ, such that the optocoupler input stage forward current I_F=(5-1.5)/1k=3.5mA<23mA, where 23mA is the maximum output current capability of F240 DSP PWM1-6 pins. Also, 1.8mA<3.5mA<5mA, Optocoupler's I_{Fon} requirement satisfied. Select R_L=3.83k for V_{cc}=15V, recommended by manufacturer.

6.3.7 Load resistance selection

For purely resistive load, a high power resistor needs to be selected. For laboratory debugging, an 8.7Ω 12A rheostat is available in the lab. Or the students need to order a properly rated power resistor for their system, which is very easy to find at Digikey.com.

6.4 Bibliography

Datasheets:

ZTX1053A, IRF7103, 1N5400, C-2685, TMS320F240, HCPL-2232

Websites:

http://www.digikey.com/

http://www.newark.com/

http://www.ti.com/

http://vandewater.freeyellow.com/basics.html