EE682 – Group Project Design

Lecture #1 Power Switch Design

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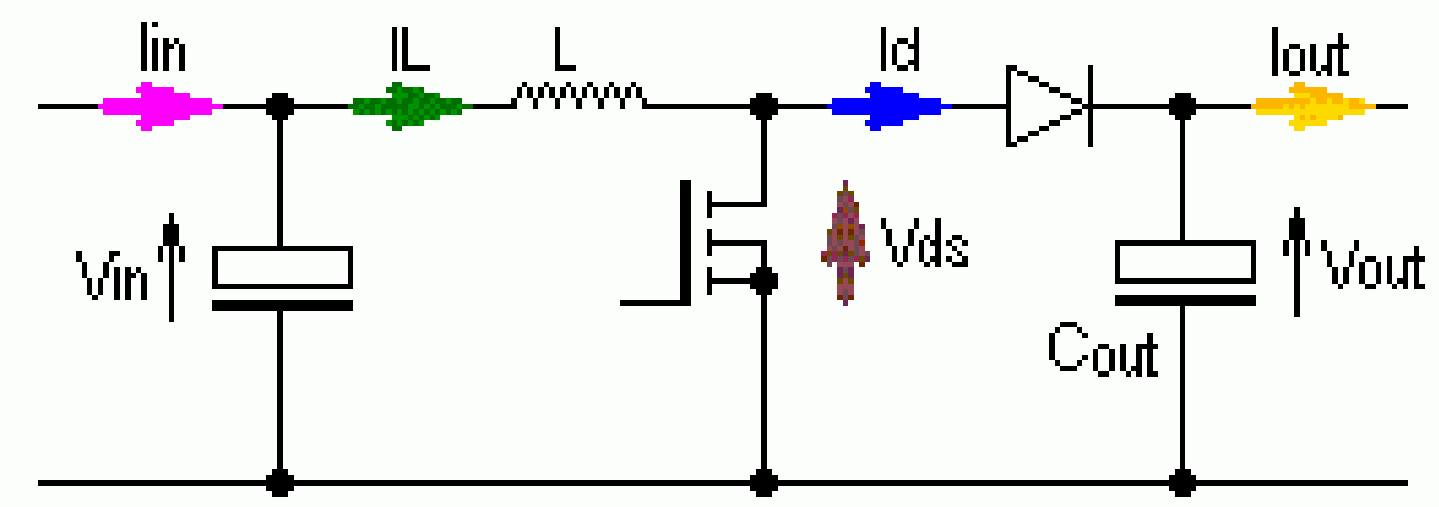
Boost DC/DC Converter Design

Boost Converter Review

1. Circuit topology

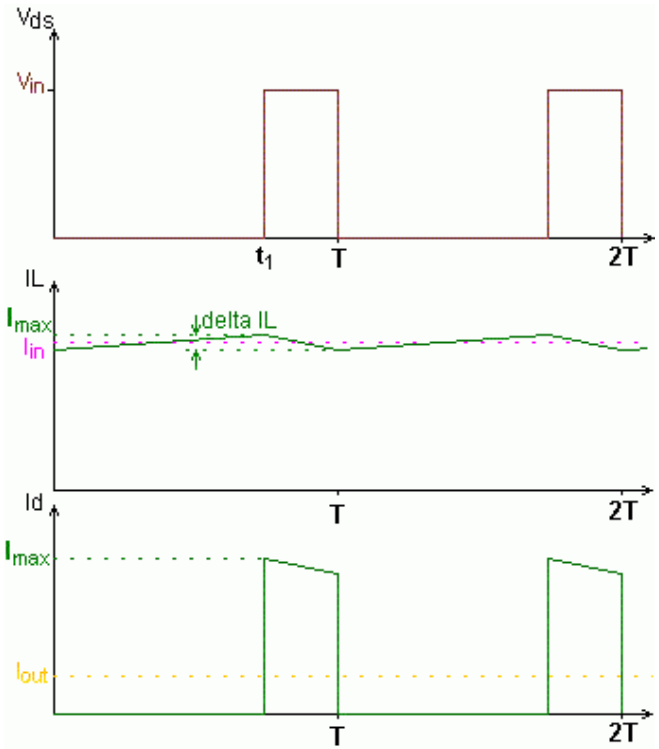


Boost Converter Review

2. Continuous conducting mode (CCM)

$$V_{out} = V_{in} \cdot \frac{T}{(T - t_1)}$$

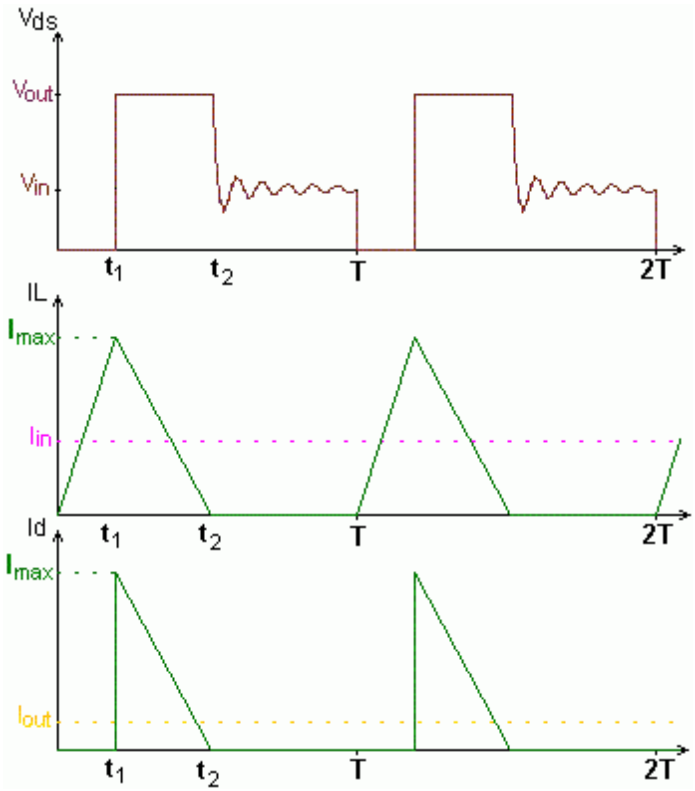
Current slope: V_L/L
Where V_L is inductor voltage



Boost Converter Review

3. Discontinuous conducting mode (DCM)

Inductor current is not continuous



Design Tasks

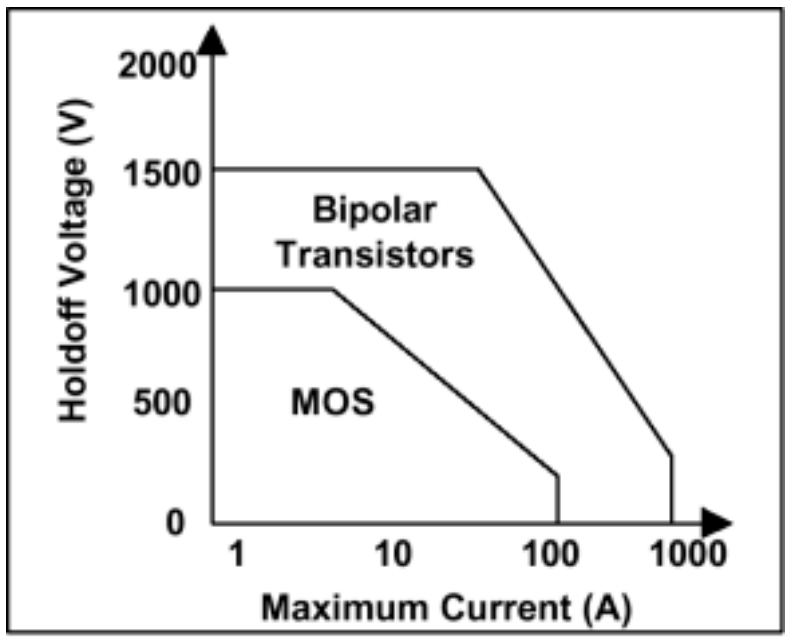
1. Power switch design
2. Inductor design
3. Capacitor design
4. Drive circuit

Design Specifications

1. Input voltage: 24 V
2. Output voltage: 48 V
3. Output power: 240 W
4. Inductor current ripple: 15 %
5. Capacitor voltage ripple: 0.1 %

Power Switch Design

1. Power BJTs, Power MOSFETs, and IGBTs
    1. BJTs – greater capacity, low ON state loss
    2. MOSFETs – fast switching, voltage driven
    3. IGBTs – combined modules, powerful and expensive



Power Switch Design

Illustrate the design procedures with a design example:

Design requirement:

A 240-watt DC/DC boost converter with V_{in}=24V and V_{out}=48V.

Power Switch Design

1. Current and voltage rating requirements

Design:

Peak transistor current equals to

$I_{in}=P/V_{in}=240W/24V=10A$

Voltage rating requirements

$V_{Tmax}=V_{out}+V_{F(diode)}=48+0.7V=48.7V$

Power Switch Design

2. Device selection based on the requirements

Design:

Candidate I: BJT 2N6547

I_C=15A>10A and V_{CE}=400V>48V

Candidate II: power MOSFET HUFA75307D3

I_D=15A>10A and V_{DS}=55V>48V

Power Switch Design

Datesheet 2N6547

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector–Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	9.0	Vdc
Collector Current — Continuous — Peak (2)	I_C I_{CM}	15 30	Adc
Base Current — Continuous — Peak (2)	I_B I_{BM}	10 20	Adc
Emitter Current — Continuous — Peak (2)	I_E I_{EM}	25 35	Adc
Total Power Dissipation @ T_C = 25_C @ T_C = 100_C Derate above 25_C	P_D	 175 100 1.0	Watts W/_C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	_C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	_C

Power Switch Design

Datesheet HUFA75307D3

HUFA75307P3, HUFA75307D3, HUFA75307D3S

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	15	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15	
Power Dissipation	P_D	45	W
Derate Above 25^oC		0.3	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Power Switch Design

3. Base/Gate drive requirements

2N6547: For I_C=15A, must have I_B>=3A, not desirable

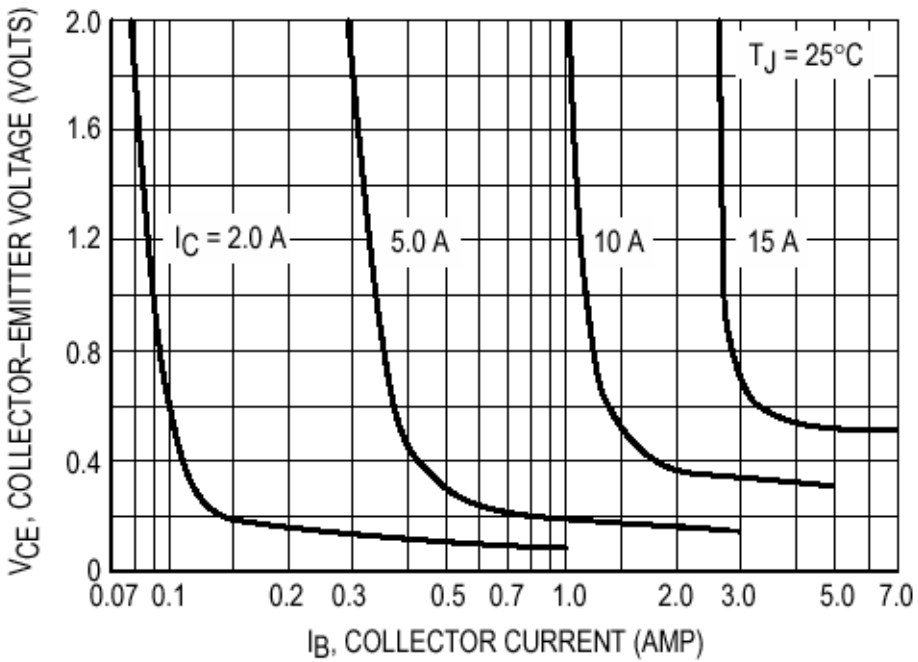


Figure 2. Collector Saturation Region

Power Switch Design

3. Base/Gate drive requirements (cont'd)

HUFA75307D3 is voltage driven:

Threshold (mininum ON) gate-source voltage V_{GSth} =4V

Maximum gate-source voltage V_{GSmax}=20V

Can be driven by TTL (+5V) or CMOS logic +15V digital circuits

Power Switch Design

4. Transient performances

2N6547

Rise time: t_r=1.0μs

Fall time: t_f=1.5μs

HUFA75307D3

Rise time: t_r=40ns

Fall time: t_f=45ns

Power Switch Design

5. Selection

Power MOSFET HUFA75307D3

6. Switching loss

$$P_{SW\_loss} = \frac{W_{loss}}{T} = \frac{1}{T}\left(W_{loss\_ON} + W_{loss\_OFF}\right) = \frac{V_{ds} I_d}{2T}\left(t_{ON} + t_{OFF}\right)$$

$$= \frac{48\times 10}{2\times \frac{1}{20\times 10^3}}\left(60+100\right)\times 10^{-9} = 0.768\text{W}$$

Power Switch Design

7. ON state loss
   1. ON state time

$$t_1 = \frac{1}{f}\left(\frac{V_{out}+V_F-V_{in}}{V_{out}}\right) = \frac{1}{20\times10^3}\left(\frac{48+0.7-24}{48}\right)\text{sec} = 25.73\,\mu\text{s}$$

   2. ON state loss

$$P_{ON\_loss} = \frac{W_{ON\_loss}}{T} = \frac{1}{T}\left(I_D^2 r_{DS(ON)} t_1\right)$$

$$= \frac{1}{\frac{1}{20\times10^3}}\left(15^2\times0.075\times25.73\times10^{-6}\right) = 8.684\text{W}$$

Power Switch Design

8. Overall loss

$$P_{loss} = P_{SW\_loss} + P_{ON\_loss} = 9.452\text{W} < \text{P}_\text{D} = 45\ \text{W}$$

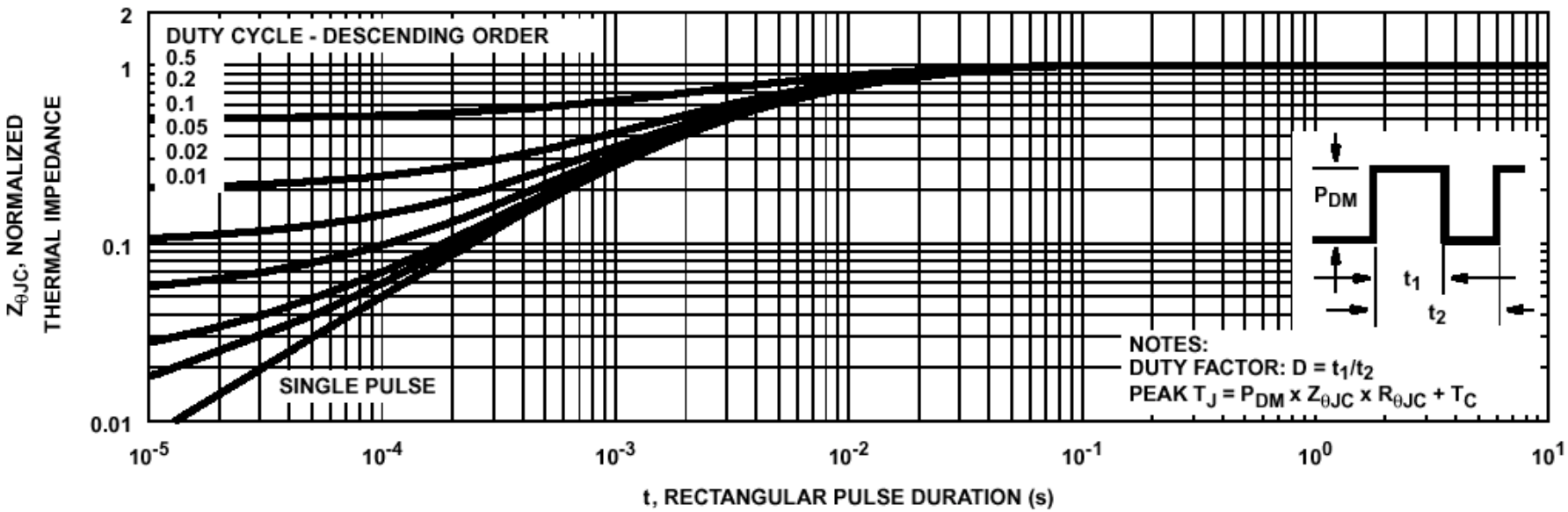
(see the datasheet of HUFA75307D3)

Power Switch Design

Calculation of junction to sink temperature difference

$$\Delta T_{JC}(t) = P_{loss} Z_{\theta JC\,(50\,\%)}(t) R_{\theta JC}$$

$$\therefore \Delta T_{js} = R_{\theta js} \times P_{loss} = 3.3^{\circ}\mathrm{C/W} \times 9.452\mathrm{W} = 31.2^{\circ}\mathrm{C} < \mathrm{T_{jmax}} = 175^{\circ}\mathrm{C}$$



Power Switch Design

HUFA75307D3 ON-resistance and turn-on and turn-off time

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		55	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 45V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 10)		2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 15A, V_{GS} = 10V (Figure 9)		-	0.075	0.090	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	3.3	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220AB		-	-	62	$^oC/W$
		TO-251AA, TO-252AA		-	-	100	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 30V, $I_D \cong$ 15A, R_L = 2.0Ω, V_{GS} = 10V, R_{GS} = 100Ω		-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$			-	7	-	ns
Rise Time	t_r			-	40	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	35	-	ns
Fall Time	t_f			-	45	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 30V, $I_D \cong$ 15A, R_L = 2.0Ω $I_{g(REF)}$ = 1.0mA (Figure13)	-	16	20	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	9	11	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	0.6	0.8	nC
Gate to Source Gate Charge	Q_{gs}			-	1.2	-	nC
Reverse Transfer Capacitance	Q_{gd}			-	4	-	nC