Modeling of Distributed Parasitics in Power FETs

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Abstract—A distributed circuit analysis of power FETs accounting for the lateral source parasitic impedance in addition to the lateral drain and gate parasitic impedances is presented. Both a numerical solution and an exact analytic solution are derived. Using the exact analytic solution, approximate equivalent circuits are derived for FETs of short gate width for two common types of boundary conditions. When the gate and drain terminals are located on opposite sides of the distributed FET, the lateral source parasitic impedance can be represented for short gate width FETs by an equivalent circuit with a negative series impedance in series with the source terminal. The practical consequences on parameter extraction for device modeling are discussed. The availability of an exact analytic solution for the distributed FET should also assist with the synthesis of traveling wave FETs.

Index Terms—Distributed parasitics, LDMOSFET, lossy substrate, power FET, traveling-wave FET.

I. INTRODUCTION

THE GROWTH in the wireless communication industry is fostering the development of new power radio-frequency (RF) transistors with higher performances in terms of cost, linearity, gain, and operating frequencies. Simultaneously, accurate models are demanded by microwave circuit designers for the design of power RF amplifiers for frequency-division multiple access (FDMA), time-division multiple access (TDMA), and code-division multiple access (CDMA) applications. Among the new power RF transistors the LDMOSFETs, which is growing in popularity will be used as an example. A common feature of power FETs is the very large effective gate width which is required to deliver the targeted power. In view of the gigahertz frequencies of operation and the large gate width used in these transistors, it is necessary to address the modeling of distributed effects in these devices. Such a study is of importance for both FET modeling purpose as well as for FET design purpose, as the lateral parasitics greatly impact the gain performances of power FETs.

A rich body of literature (see [1]–[11] and references therein) is available on the analysis of distributed parasitics in power FETs. The pioneer work of Wolf [1] established the well-known result that the gate/base parasitic in a transistor can be represented for short width by a resistance equal to one-third of the gate or base total resistance. This result was stated to also hold for the source and drain parasitic impedances in [6], although no proof was provided. We shall see in this paper that this result is valid for only one of the two commonly used

boundary conditions. An exact analytic solution was derived by Kuvas [2] for the case of a distributed parasitic gate impedance. Kretschmer *et al.* [3] and Chang *et al.* [7] demonstrated how to extend the analysis to distributed gate and drain parasitics but no analytic solution was reported. Several papers rely on sliced models [8], [9], [11] to implement the distributed FET, using synthetic transmission lines realized with multiple cascaded elemental lumped FET circuits. Such models can then be conveniently implemented and analyzed using a circuit simulator and can be used to design traveling wave FETs. A full wave analysis of the propagation in a MESFET has also been reported by Heinritsch and Hartnagel [4], [5]. In this paper we rely instead on coupled-mode theory which assumes a quasi-TEM propagation.

Most of the papers [1]–[3], and [7] focus only on the lateral gate and drain parasitics and do not consider the effect of the lateral source parasitics. However, a few references [6], [9]–[11] do show a more general equivalent circuit model including a lateral source resistance or impedance in the analysis of the distributed effects. However no analytic solution is obtained for the distributed FET and no equivalent circuit is derived in the limits of short gate width (except for [6], see comment above).

Reference [6] gives the most general three-terminal distributed network which can be used to model the distributed parasitic network. This distributed network will be adopted here with a single modification: the distributed device is not assumed to be directly connected to the input ground except through the source distributed ground line. The removal of this unphysical ground constraint is quite beneficial as this reduces the analysis from a six-port device with three modes and three propagation constants to a four-port device with two modes and two propagation constants. In [6], the analysis method used is briefly outlined but the effect of the location of the gate and drain excitations, which greatly affects the final characteristic of the distributed FET is not discussed. The importance of the location of the boundary condition was reported in Chang *et al.* [7] and Abdipour *et al.* [11] but no analytic solution or approximate equivalent circuit for gate width FETs is provided.

In this paper, we report an analysis of the FET parasitics which accounts for the distributed effects contributed by the lateral source, drain and gate resistances/inductance/mutual-inductance in power FETs. Both an exact numerical and analytic solution are derived and are verified to be in agreement. The analytic solution is then used to generate a convenient approximate equivalent circuit for the case of FETs with small gate width. The exact solution and approximate equivalent circuits are then compared for the case of a power LDMOSFET. Of particular interest is the analysis of a distributed FET for which the gate and drain terminals are excited on opposite sides of the distributed FET. A new type of equivalent circuit is found to be required for

Manuscript received January 1, 2002; revised May 28, 2002. This work was supported by Agere Systems. The review of this paper was arranged by Editor M. A. Shibib.

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Publisher Item Identifier 10.1109/TED.2002.803647.

Fig. 1. Possible layout for a power FET.

modeling this common configuration. The paper concludes with a discussion on the practical consequences and applications of the theoretical results obtained.

II. DISTRIBUTED SOURCE, DRAIN, AND GATE EFFECTS

A typical layout for a power transistor cell is shown in Fig. 1. This cell is terminated on each side by the gate and drain wire-bond pads respectively. Multiple such cells can then be placed in parallel (above and below the cell shown) as is suggested by the black dots to form the complete transistor. The cell shown laterally integrates 40 vertically aligned subtransistors. The distributed model developed in this paper can strictly only be applied to each of the 20 vertically aligned subtransistors.

The analysis of the lateral discrete distributed network connecting the 40 transistors can be performed using regular circuit analysis. Note that at the frequencies considered the short lateral interconnect wires between the transistor fingers can be approximated by an inductor and resistances in series (see Fig. 2). The overall circuit can then be expressed as the product of 20 four-port $ABCD$ matrices. However in view of the large number of individual transistor fingers used (40 here) it can be advantageous to approximate this lumped-circuit by a distributed network. In such a case, the analytical results for the distributed network we derive in this paper are also applicable to the laterally distributed network.

Note however, that in the interest of simplicity of presentation the lateral distributed effects will be neglected in the example selected to demonstrate the application of the theory.

The equivalent circuit for the analysis of the distributed effects is shown in Fig. 3. Note that the distributed circuit is not connected to the arbitrary ground reference terminal as was assumed in [6]. Instead, the source contacts on both sides of the FET will be used as the local reference ground for this distributed FET. It is indeed one of the goal of this paper to account for the effect of a nonideal source line.

Fig. 2. Equivalent circuit for the lateral FET network.

As is shown in Fig. 3, the matrices Z'_p and $Y'_d = Z'^{-1}_d$ are the parasitic impedance per-unit-length and the FET device admittance per-unit-length, respectively

$$Z'_p = \begin{bmatrix} Z'_{go} & M'_{12} & M'_{13} \\ M'_{12} & Z'_{do} & M'_{23} \\ M'_{13} & M'_{23} & Z'_{so} \end{bmatrix}$$

$$Z'_d = Y'^{-1}_d = \begin{bmatrix} Z'_{11} & Z'_{12} & Z'_{13} \\ Z'_{21} & Z'_{22} & Z'_{23} \\ Z'_{31} & Z'_{32} & Z'_{33} \end{bmatrix}$$

using

$$Z'_{go} = \frac{Z_g}{W}, \quad Z'_{do} = \frac{Z_d}{W}, \quad Z'_{so} = \frac{Z_s}{W}, \quad M'_{ij} = M'_{ji} = \frac{M_{ij}}{W}$$

and

$$Z'_{ij} = W Z_{ij}.$$

Z'_{go} , Z'_{so} , Z'_{do} are the lateral gate, source and drain impedances per unit length, M'_{ij} the lateral mutual impedances per

Fig. 3. Equivalent circuit network for the vertical distributed FET.

unit length. Note that the inductance matrix component L_p (inductances and mutual inductances) of $Z'_p = j\omega L'_p + R'_p$ can be evaluated within the TEM approximation [12] using

$$L'_p = \frac{1}{c^2} C_0'^{-1}$$

where C_0' is the capacitance matrix per-unit-length of the FET lines when all dielectrics are removed and c the speed of light in free space.

The voltage and current along the distributed FET satisfy the following:

$$\begin{bmatrix} \frac{dV_1}{dx} \\ \frac{dV_2}{dx} \\ \frac{dV_3}{dx} \end{bmatrix} = Z'_p \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = Z'_d \begin{bmatrix} \frac{di_1}{dx} \\ \frac{di_2}{dx} \\ \frac{di_3}{dx} \end{bmatrix}. \quad (1)$$

From the current continuity equation we have the following identities:

$$i_1 + i_2 + i_3 = 0 \quad \frac{di_1}{dx} + \frac{di_2}{dx} + \frac{di_3}{dx} = 0. \quad (2)$$

We also find useful to introduce the spatially varying gate-to-source V_{gs} and drain-to-source V_{ds} voltages for which we can write the following equations:

$$\begin{aligned} V_{gs} &= V_1 - V_3, & \frac{dV_{gs}}{dx} &= \frac{dV_1}{dx} - \frac{dV_3}{dx} \\ V_{ds} &= V_2 - V_3, & \frac{dV_{ds}}{dx} &= \frac{dV_2}{dx} - \frac{dV_3}{dx}. \end{aligned} \quad (3)$$

Using (2) and (3), we can reduce the system of (1) to

$$\begin{bmatrix} \frac{dV_{gs}}{dx} \\ \frac{dV_{ds}}{dx} \end{bmatrix} = Z''_p \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} V_{gs} \\ V_{ds} \end{bmatrix} = Z''_d \begin{bmatrix} \frac{di_1}{dx} \\ \frac{di_2}{dx} \end{bmatrix} \quad (4)$$

where we have introduced the 2×2 device impedance matrix Z''_d and the 2×2 parasitic matrix Z''_p defined in the following as:

$$\begin{aligned} Z''_d &= \begin{bmatrix} Z''_{11} & Z''_{12} \\ Z''_{21} & Z''_{22} \end{bmatrix} \\ &= \begin{bmatrix} Z'_{11} - Z'_{31} - Z'_{13} + Z'_{33} & Z'_{12} - Z'_{32} - Z'_{13} + Z'_{33} \\ Z'_{21} - Z'_{31} - Z'_{23} + Z'_{33} & Z'_{22} - Z'_{32} - Z'_{23} + Z'_{33} \end{bmatrix} \\ Z''_p &= \begin{bmatrix} Z'_g + Z'_s & Z'_s \\ Z'_s & Z'_d + Z'_s \end{bmatrix}. \end{aligned}$$

Note that we have expressed Z''_p in terms of the following generalized impedances

$$Z'_g = Z'_{go} - M'_{12} - M'_{13} + M'_{23} \quad (5)$$

$$Z'_d = Z'_{do} - M'_{12} + M'_{13} - M'_{23} \quad (6)$$

$$Z'_s = Z'_{so} + M'_{12} - M'_{13} - M'_{23}. \quad (7)$$

This generalized impedance notation shows how the mutual impedances can be conveniently absorbed in the gate, drain and source lateral impedances during the extraction process.

From the System of (4) we obtain the following second-order system of differential equations:

$$\begin{bmatrix} \frac{d^2 i_1}{dx^2} \\ \frac{d^2 i_2}{dx^2} \end{bmatrix} = N \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (8)$$

where we have defined $N = Y''_d Z''_p$ as

$$\begin{aligned} N &= \begin{bmatrix} N_{11} & N_{12} \\ N_{21} & N_{22} \end{bmatrix} \\ &= \begin{bmatrix} (Z'_g + Z'_s) Y''_{11} + Z'_s Y''_{12} & Z'_s Y''_{11} + (Z'_d + Z'_s) Y''_{12} \\ (Z'_g + Z'_s) Y''_{21} + Z'_s Y''_{22} & Z'_s Y''_{21} + (Z'_d + Z'_s) Y''_{22} \end{bmatrix} \end{aligned}$$

with Y''_d the inverse of Z''_d

$$Y''_d = \begin{bmatrix} Y''_{11} & Y''_{12} \\ Y''_{21} & Y''_{22} \end{bmatrix} = \begin{bmatrix} Z''_{11} & Z''_{12} \\ Z''_{21} & Z''_{22} \end{bmatrix}^{-1}.$$

The propagation constants which can then be obtained from the eigenvalues of the matrix N [6] ($\det |N - \lambda I| = 0$) are given by

$$\lambda = \gamma_{1/2}^2 = \frac{1}{2} \left[N_{11} + N_{22} \pm \sqrt{(N_{11} - N_{22})^2 + 4N_{12}N_{21}} \right].$$

Equation (8) admits a solution of the following form:

$$i_1(x) = Ae^{\gamma_1 x} + Be^{-\gamma_1 x} + Ce^{\gamma_2 x} + De^{-\gamma_2 x} \quad (9)$$

$$i_2(x) = J_1 (Ae^{\gamma_1 x} + Be^{-\gamma_1 x}) + J_2 (Ce^{\gamma_2 x} + De^{-\gamma_2 x}) \quad (10)$$

where J_1 and J_2 are the ratios i_2/i_1 obtained from the eigenvectors of N

$$J_1 = \frac{\gamma_1^2 - N_{11}}{N_{12}} \quad \text{and} \quad J_2 = \frac{\gamma_2^2 - N_{11}}{N_{12}}.$$

Using (8), we can write the boundary conditions at $x = 0$ and $x = L$ in the following four-dimensional (4-D) matrix equation

$$I'' = \begin{bmatrix} \frac{d^2 i_1(0)}{dx^2} \\ \frac{d^2 i_2(0)}{dx^2} \\ \frac{d^2 i_1(W)}{dx^2} \\ \frac{d^2 i_2(W)}{dx^2} \end{bmatrix} = \begin{bmatrix} N_{11} & N_{12} & 0 & 0 \\ N_{21} & N_{22} & 0 & 0 \\ 0 & 0 & N_{11} & N_{12} \\ 0 & 0 & N_{21} & N_{22} \end{bmatrix} \begin{bmatrix} i_1(0) \\ i_2(0) \\ i_1(W) \\ i_2(W) \end{bmatrix} = N_2 I \quad (11)$$

where I is the 4×1 vector of the line current at $x = 0$ and $x = L$.

Using (9) and (10), we can write the following two identities which relate the current and its derivatives at the boundaries to the unknown current coefficients A, B, C , and D (vector P):

$$I = \begin{bmatrix} 1 & 1 & 1 & 1 \\ J_1 & J_1 & J_2 & J_2 \\ e^{\gamma_1 W} & e^{-\gamma_1 W} & e^{\gamma_2 W} & e^{-\gamma_2 W} \\ J_1 e^{\gamma_1 W} & J_1 e^{-\gamma_1 W} & J_2 e^{\gamma_2 W} & J_2 e^{-\gamma_2 W} \end{bmatrix} \begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix} = D_1 P \quad (12)$$

$$I' = \begin{bmatrix} \gamma_1 & -\gamma_1 & \gamma_2 & -\gamma_2 \\ J_1 \gamma_1 & -J_1 \gamma_1 & J_2 \gamma_2 & -J_2 \gamma_2 \\ \gamma_1 e^{\gamma_1 W} & -\gamma_1 e^{-\gamma_1 W} & \gamma_2 e^{\gamma_2 W} & -\gamma_2 e^{-\gamma_2 W} \\ J_1 \gamma_1 e^{\gamma_1 W} & -J_1 \gamma_1 e^{-\gamma_1 W} & J_2 \gamma_2 e^{\gamma_2 W} & -J_2 \gamma_2 e^{-\gamma_2 W} \end{bmatrix} \cdot \begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix} = D_2 P. \quad (13)$$

From (4), we can also write the following 4-D equation:

$$V = \begin{bmatrix} V_{gs}(0) \\ V_{ds}(0) \\ V_{gs}(W) \\ V_{ds}(W) \end{bmatrix} = \begin{bmatrix} Z_{11}'' & Z_{12}'' & 0 & 0 \\ Z_{21}'' & Z_{22}'' & 0 & 0 \\ 0 & 0 & Z_{11}'' & Z_{12}'' \\ 0 & 0 & Z_{21}'' & Z_{22}'' \end{bmatrix} \begin{bmatrix} \frac{di_1(0)}{dx} \\ \frac{di_2(0)}{dx} \\ \frac{di_1(W)}{dx} \\ \frac{di_2(W)}{dx} \end{bmatrix} = Z_2'' I'. \quad (14)$$

Then using (11)–(13) the following relation between V and I can be obtained:

$$V = Z_2'' D_2 D_1^{-1} I. \quad (15)$$

As a result, the four-port Z parameter matrix of the distributed FET is simply given by the following equations [note the direction of the currents $i_k(x)$ at $x = 0$]

$$Z = Z_2'' D_2 D_1^{-1}. \quad (16)$$

This final result provides the mean to numerically calculate the impedance matrix of the distributed FET. In our case these equations were implemented in MATLAB. We defer an analysis of this result to Section V.

III. ANALYTIC SOLUTIONS

The solution developed in the previous section leads to a simple numerical solution. A direct analytic solution can however also be obtained by analytically evaluating the matrix $Z = Z_2'' D_2 D_1^{-1}$. This was done with the help of Maple, although this leads to an extremely long solution. After many simple but tedious simplifications, the following compact exact results can be obtained for the FET impedance matrix:

$$\begin{aligned} Z_{11} &= Z_{33} \\ &= \frac{Z_{11}''}{\gamma_1^2 - \gamma_2^2} [\gamma_1^2 \gamma_2 \coth(\gamma_2 W) - \gamma_1 \gamma_2^2 \coth(\gamma_1 W)] \\ &\quad + \frac{Z_g' + Z_s'}{\gamma_1^2 - \gamma_2^2} [\gamma_1 \coth(\gamma_1 W) - \gamma_2 \coth(\gamma_2 W)] \\ Z_{12} &= Z_{34} \\ &= -\frac{Z_{12}''}{\gamma_1^2 - \gamma_2^2} [\gamma_2^3 \coth(\gamma_2 W) - \gamma_1^3 \coth(\gamma_1 W)] \\ &\quad - \frac{Z_{12}'' N_{11} - Z_{11}'' N_{12}}{\gamma_1^2 - \gamma_2^2} [\gamma_1 \coth(\gamma_1 W) - \gamma_2 \coth(\gamma_2 W)] \\ Z_{13} &= Z_{31} \\ &= \frac{Z_{11}''}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_1^2 \gamma_2}{\sinh(\gamma_2 W)} - \frac{\gamma_1 \gamma_2^2}{\sinh(\gamma_1 W)} \right] \\ &\quad + \frac{Z_g' + Z_s'}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_1}{\sinh(\gamma_1 W)} - \frac{\gamma_2}{\sinh(\gamma_2 W)} \right] \\ Z_{14} &= Z_{32} \\ &= -\frac{Z_{12}''}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_2^3}{\sinh(\gamma_2 W)} - \frac{\gamma_1^3}{\sinh(\gamma_1 W)} \right] \\ &\quad - \frac{Z_{12}'' N_{11} - Z_{11}'' N_{12}}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_1}{\sinh(\gamma_1 W)} - \frac{\gamma_2}{\sinh(\gamma_2 W)} \right] \\ Z_{21} &= Z_{43} \\ &= \frac{Z_{21}''}{\gamma_1^2 - \gamma_2^2} [\gamma_1^2 \gamma_2 \coth(\gamma_2 W) - \gamma_1 \gamma_2^2 \coth(\gamma_1 W)] \\ &\quad + \frac{Z_s'}{\gamma_1^2 - \gamma_2^2} [\gamma_1 \coth(\gamma_1 W) - \gamma_2 \coth(\gamma_2 W)] \\ Z_{22} &= Z_{44} \\ &= -\frac{Z_{22}''}{\gamma_1^2 - \gamma_2^2} [\gamma_2^3 \coth(\gamma_2 W) - \gamma_1^3 \coth(\gamma_1 W)] \\ &\quad - \frac{Z_{22}'' N_{11} - Z_{21}'' N_{12}}{\gamma_1^2 - \gamma_2^2} [\gamma_1 \coth(\gamma_1 W) - \gamma_2 \coth(\gamma_2 W)] \end{aligned}$$

$$\begin{aligned}
Z_{23} &= Z_{41} \\
&= \frac{Z_{21}''}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_1^2 \gamma_2}{\sinh(\gamma_2 W)} - \frac{\gamma_1 \gamma_2^2}{\sinh(\gamma_1 W)} \right] \\
&\quad + \frac{Z_s'}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_1}{\sinh(\gamma_1 W)} - \frac{\gamma_2}{\sinh(\gamma_2 W)} \right] \\
Z_{24} &= Z_{42} \\
&= -\frac{Z_{22}''}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_2^3}{\sinh(\gamma_2 W)} - \frac{\gamma_1^3}{\sinh(\gamma_1 W)} \right] \\
&\quad - \frac{Z_{22}'' N_{11} - Z_{21}'' N_{12}}{\gamma_1^2 - \gamma_2^2} \left[\frac{\gamma_1}{\sinh(\gamma_1 W)} - \frac{\gamma_2}{\sinh(\gamma_2 W)} \right].
\end{aligned}$$

Note that in these results, we have expressed the matrix elements Z_{ij} using the usual current definition shown in Fig. 4 so that we have

$$\begin{bmatrix} v_{ds1} \\ v_{gs1} \\ v_{ds2} \\ v_{gs2} \end{bmatrix} = Z \begin{bmatrix} -i_1(0) \\ -i_2(0) \\ i_1(W) \\ i_2(W) \end{bmatrix} = Z \begin{bmatrix} i_{d1} \\ i_{g1} \\ i_{d2} \\ i_{g2} \end{bmatrix}.$$

For small gate widths W , a simpler approximate solution for the impedance matrix of the distributed FET can be obtained using power series expansions. When γW is small we can indeed approximate the $\coth(\gamma W)$ and $1/\sinh(\gamma W)$ function as

$$\coth(\gamma_{1/2} W) \approx \frac{1}{\gamma_{1/2} W} + \frac{\gamma_{1/2} W}{3} \quad (17)$$

$$\frac{1}{\sinh(\gamma_{1/2} W)} \approx \frac{1}{\gamma_{1/2} W} - \frac{\gamma_{1/2} W}{6}. \quad (18)$$

Substituting these power-series expansions in the 16 elements of the exact analytic solution presented earlier, the impedance matrix Z is found to simplify to the equation as shown at the bottom of the page. The Z matrix derived above presents an approximate 4×4 impedance matrix of the four-port distributed FET which is valid for short gate-width (the usual case).

IV. BOUNDARY CONDITIONS

A distributed FET is in its most general form a four-port device since the gate-to-source and drain-to-source voltages can be applied on both sides of the distributed FET. However in conventional device layouts the gate-to-source contact and drain-to-source voltages are usually applied on a single side at a time and

Fig. 4. Four-port network representation of distributed FET.

we can reduce for such case the 4×4 impedance to a final 2×2 impedance matrix Z_f .

Due to the symmetry of the device only two different boundary conditions need to be considered. These two different boundary conditions, referred to as case A and case B, are shown in Fig. 5. Electrically, the boundary conditions consist of:

- case A

$$\begin{aligned}
i_1(0) &= -I_1, \quad i_2(0) = -I_2, \quad i_1(W) = 0, \quad i_2(W) = 0 \\
V_{gs} &= V_{gs}(0) \quad \text{and} \quad V_{ds} = V_{ds}(0).
\end{aligned}$$

- case B

$$\begin{aligned}
i_1(0) &= -I_1, \quad i_2(0) = 0, \quad i_1(W) = 0, \quad i_2(W) = I_2, \\
V_{gs} &= V_{gs}(0) \quad \text{and} \quad V_{ds} = V_{ds}(W).
\end{aligned}$$

Applying these two boundary conditions to the exact 4×4 impedance matrix Z , we obtain the following 2×2 matrices Z_f :

$$Z_{f,1} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}, \quad Z_{f,2} = \begin{bmatrix} Z_{11} & Z_{14} \\ Z_{41} & Z_{44} \end{bmatrix}$$

for the exact distributed solution. The input and output impedance elements are the same, since we have $Z_{44} = Z_{22}$ but the trans-impedance element are found to be different.

Applying the two previous boundary conditions to the approximate 4×4 impedance matrix Z we obtain the following two different 2×2 matrices Z_f :

$$\begin{aligned}
Z_{f,1a} &= \begin{bmatrix} Z_{11}'' + \frac{Z_g' + Z_s'}{3} & Z_{12}'' + \frac{Z_s'}{3} \\ Z_{21}'' + \frac{Z_s'}{3} & Z_{22}'' + \frac{Z_d' + Z_s'}{3} \end{bmatrix} \\
Z_{f,2a} &= \begin{bmatrix} Z_{11}'' + \frac{Z_g' + Z_s'}{3} & Z_{12}'' - \frac{Z_s'}{6} \\ Z_{21}'' - \frac{Z_s'}{6} & Z_{22}'' + \frac{Z_d' + Z_s'}{3} \end{bmatrix}
\end{aligned}$$

for FETs of short gate width ($\gamma_1 W, \gamma_2 W \ll 1$).

$$Z = \begin{bmatrix} Z_{11}'' + \frac{Z_g' + Z_s'}{3} & Z_{12}'' + \frac{Z_s'}{3} & Z_{11}'' - \frac{Z_g' + Z_s'}{6} & Z_{12}'' - \frac{Z_s'}{6} \\ Z_{21}'' + \frac{Z_s'}{3} & Z_{22}'' + \frac{Z_d' + Z_s'}{3} & Z_{21}'' - \frac{Z_s'}{6} & Z_{22}'' - \frac{Z_d' + Z_s'}{6} \\ Z_{11}'' - \frac{Z_g' + Z_s'}{6} & Z_{12}'' - \frac{Z_s'}{6} & Z_{11}'' + \frac{Z_g' + Z_s'}{3} & Z_{12}'' + \frac{Z_s'}{3} \\ Z_{21}'' - \frac{Z_s'}{6} & Z_{22}'' - \frac{Z_d' + Z_s'}{6} & Z_{21}'' + \frac{Z_s'}{3} & Z_{22}'' + \frac{Z_d' + Z_s'}{3} \end{bmatrix}$$

Fig. 5. Two commonly used boundary conditions with the associated location of the drain and gate excitations.

Like for the exact analytic solution, the diagonal impedance elements are the same and off-diagonal element are different. Closer inspection reveals, however, that the gate and drain parasitic impedance give the same contribution to the input and output impedance such that in the limits of zero lateral source impedance, both boundary conditions admit the same impedance matrix and each are equivalent to the addition of a series resistance $Z_g/3$ and $Z_d/3$ to the gate and drain contacts respectively. This is a well-known result that has been reported in many papers [1], [2], [6].

The situation is, however, different if we have a nonzero lateral source impedance. In such a case, different impedance matrices are obtained for each boundary condition as a result of the distributed nature of the device.

V. NUMERICAL RESULTS

To explore the impact of the source impedance in further detail, let us consider the example of a power LDMOSFET [13] with $N_f = 224$ fingers each of gate width $W = 90 \mu\text{m}$, for a total lateral source resistance $R_s = R'_s W / (3N_f) = 1.3 \Omega$. In Fig. 6, we have plotted the MAG/MSG and $|S_{21}|^2$ versus gate width W at 1 GHz, for both boundary conditions. The LDMOSFET gain is plotted for a gate width exceeding the practical usefulness of the power LDMOSFETs to show the range of validity of the linear approximation.

Fig. 6(a) corresponds to the case of boundary condition A and Fig. 6(b) corresponds to the case of boundary condition B. In each graph (a) and (b), we compare the numerical solution (circle) obtained from (16) and the analytic solution (plus) given by (17) (see Section III). In each graph (a) and (b), both traces A and B give the same result, demonstrating the validity of the analytic solution obtained for the FET impedance matrix Z . In each graph (a) and (b), the trace C (cross) gives the results obtained with the approximate impedance matrix obtained in the limits of short gate width. The approximate solution is seen to equal the exact solution for gate width smaller than $40 \mu\text{m}$, but deviates for larger gate widths, leading to errors as large as 5 dB for $180\text{-}\mu\text{m}$ gate width.

VI. EQUIVALENT CIRCUIT

In the limits of distributed FETs of short gate width, we can implement the distributed effects using an equivalent circuit. In the case of boundary condition A, the equivalent circuit can be obtained easily by adding a third of the total lateral gate, drain and source parasitic impedances in series with each of these

(a)

(b)

Fig. 6. $|S_{21}|^2$ and MAG/MSG versus gate width W for the boundary conditions of (a) case A and (b) case B at 1 GHz.

terminals respectively. This is shown in the left-hand side of Fig. 7.

However, in the case of boundary condition B, the parameters of gate and drain side obtained are a somewhat more complex form than in the case of boundary condition A, and a negative series source impedance is required.

The use of a negative series impedance is not really an issue since the overall input ($Z_{f,11}$) and output ($Z_{f,22}$) impedances remains positive and only the trans-impedances are negative.

Fig. 7. Equivalent circuits for boundary conditions A and B.

Fig. 8. Comparison of the performance of the equivalent circuit I and II applied to the boundary condition B in the small gate width approximation. $|S_{21}|^2$ and MSG/MAG at 1 GHz are plotted versus gate width W .

The negative trans-impedance is nonetheless a sign of the fundamental impact of using gate-to-source and drain-to-source excitations located at opposite sides of the distributed FET.

To illustrate the importance of using the correct equivalent circuit topology we compare in Fig. 8, the results obtained when the equivalent circuit I (circle) and II (cross) are both used for modeling the boundary condition B. A substantial error is introduced by the equivalent circuit I at gate widths as small as 45 μm , for which the equivalent circuit II was seen to be a valid approximation when compared to the exact solution.

VII. CONCLUSION

In this paper, we have presented a coupled-mode circuit-analysis of the lateral source, drain, and gate-lateral parasitic impedances in distributed FETs. An exact analytic formula that accounts for the source impedances in addition to the drain and gate impedances was given for the first time. This exact solution was used to establish equivalent-circuit approximations for FETs of short gate width for various types of boundary conditions. A new type of equivalent circuit was found to be required when the gate and drain terminals are located on opposite sides of the distributed FET.

An important consequence of this work is that an effective reduction of the series source impedance can be expected to be

induced by the lateral distributed source impedance when the gate and drain are on opposite sides. It is possible to conceive that in the limits of large lateral source resistance $R_s(\text{lat})$, the negative resistance induced by the boundary condition of case B could actually offset the intrinsic vertical source resistance $R_s(\text{int})$ of the FET and that a total effective negative $R_s(\text{eff})$ would result

$$R_s(\text{eff}) = R_s(\text{int}) - \frac{R_s(\text{lat})}{6}. \quad (19)$$

A similar result holds also for the source inductance. Note that the example considered in this paper assumes that the substrate inductance is negligible. For perfect conductor and dielectric this is fully justified as the substrate ground plane creates as an image of the microstrip which does not contribute any inductance. For LDMOSFET, the substrate usually includes both a low and high conductivity silicon layer beside the metallization at the bottom of the substrate. Although several references have noted that a lossy substrate contributes a longitudinal inductance [14] or impedance [15] per unit length resulting from the magnetic field penetration in the substrate, the authors are not aware of any report in the literature giving the fraction of this longitudinal impedance per length which is contributed to the longitudinal self-inductance per unit length of the return current in the substrate. Further work along this line is therefore of great interest particularly for high-frequency applications.

The result expressed by (19) is obviously of importance for the parameter extraction of power FETs. For example in the analytic parameter extraction reported in [16] for a two-time constant nonquasi-static FET model, the requirement for positive R_s and L_s should be relaxed. The exact physical conditions under which a net negative $R_s(\text{effective})$ can be observed remains, however, to be determined. At the very least, the lateral resistance contributes in the reduction of the value of the effective source contact resistance, which is usually smaller than the drain resistance R_d (about six times smaller in [16]). To conclude, recall that even though in the common boundary condition of case B, the contribution of the lateral source impedance is subtractive ($-Z_s/6$) for the device trans-impedances (Z_{12} , Z_{21}), its contribution is always additive ($+Z_s/3$) for the transistor input and output impedances (Z_{11} , Z_{22}), under both types of boundary conditions.

It is also useful to mention that the availability of the exact analytic solution derived in this paper should also assist with the synthesis of traveling wave FETs. Note that previous analyses

[8], [9], [11] relied on sliced models. The analysis of complex distributed FET layouts with gate and drain electrodes connected at multiple locations, can now be directly analyzed, using the exact 4×4 Z matrix reported for the distributed FET model.

ACKNOWLEDGMENT

The authors would like to thank the anonymous reviewers for their suggestions.

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