

Project Assignment #4**DUE: Friday, April 18th.**

In this assignment you will be writing an alternative architecture for the 8 bit ALU.

DO NOT Change the Entity Description for the 8 bit ALU.

The testbench is in file ~degroat/ee762_assign/pr_step4.vhdl. Note that this is the same testbench as in step 3. Also note that you do not have to recompile the ENTITY as the ENTITY for the 8-bit ALU does not change for this assignment.

The alternative architecture that you are to write will use a PROCESS statement to describe the operation of the ALU on a slice-by-slice basis. You will write a process that will iteratively (use a loop) compute the Cout, and Result for each slice of the 8 bits of the ALU. The Cin will be the Cout of the previous iteration. Your architecture should have a different name than the architectures of step 3. It will contain one and only one process and no other concurrent statements. You should use a process with a sensitivity list. The sensitivity list will contain all signals that are on the right hand side of statements within the process.

You are to use a loop to iterate the function of the ALU slice from the LSB to the MSB. In each iteration use the value of A_i , B_i , Cin_i , Pct_i , Kct_i , and Rct_i to compute the $Cout_i$ and $Result_i$ for that slice. In an iteration use $A(i)$, $B(i)$, $Pctl$, $Kctl$, $Rctl$ and Cin to the slice to do the same computations that are done in the bit slice architecture, passing the Cout of iteration i as the Cin input to iteration $i+1$.

Use variables as appropriate and remember the difference in variables and signals.

Compile and simulate this description. You will need to simulate for 17 us.

You can do this by using the command >run 17 us

.do files will be created for both the waveform and the listing.

Don't forget to put your COMPONENT declaration, configuration and instantiation in the testbench architecture. The configuration needs to specify this new architecture.

TURN IN: (use the pr4_list.do and ps4_wave.do files to set up listing and waveform)

- a) Listing of the VHDL code.
- b) Simulation results listing. (remember - NO LINE WRAP!!!)
- c) Waveform of the complete simulation (use Zoom->FullSize) plus the region 7300 to 9800 ns.