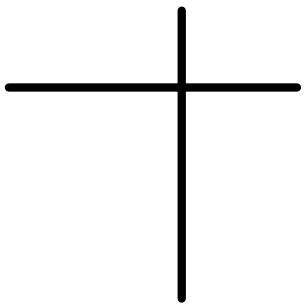
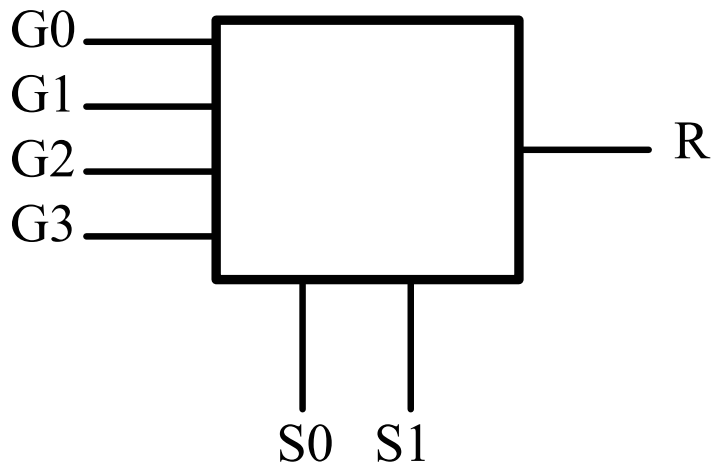
Project Step 1
Due Friday Apr 4th

A 4-to-1 mux.

The Unit to Model – A 4-to-1 Mux

- Truth Table





This Unit Can perform any of the logic functions of 2 inputs

Project Step 1

- Objective – **Model the unit. Connect the data inputs, A and B to the Select inputs, the G inputs to the corresponding data lines.**
- **You will then have a "generic" logic unit that can perform any of the functions of two inputs.**

The 16 functions

The 16 functions are: **(note that the G values are Hex)**

G3 G2 G1 G0	Function
0	zero
1	NOR
2	A'B
3	A'
4	AB'
5	B'
6	XOR
7	NAND
8	AND
9	XNOR
A	B
B	A' + B
C	A
D	A + B'
E	OR
F	one

How to model

- Model using a dataflow style
  - Concurrent signal assignment statement
    - Y <= (A AND B OR C) NOR D;
  - Conditional signal assignment statement (pp 207-209)
    - Y <= ‘1’ WHEN Q = “000” ELSE
    - A AND C WHEN Q = “001” ELSE …
  - Selected signal assignment statement (pp 272-275)
    - WITH bit_vector_signal SELECT
    - Y <= ‘0’ WHEN “0000”
    - ‘1’ WHEN “0010” | “0011”
    - A WHEN OTHERS;
- Note that all three of these are concurrent statements of the language.

The testbench

- In this assignment you are given the testbench which will stimulate your model by applying exhaustive testing.
- Copy the file pr_step1.vhdl
  - FROM the web page or from ~degroat/ee762_assign
- The ENTITY is provided for you. Enter the architecture.

Simulate and get results

- Compile the file
- Simulate the design – generate both waveform and a listing of the results.
- Turn in
  - Copy of the code
  - Copy of the listing file
  - Copy of the waveform. BE SURE TO GET THE ENTIRE SIMULATION. Use zoom as appropriate. You will need to simulate for 5200 ns to run all the test cases.