Homework Assignment #1 **DUE: Monday March 31st**

This assigment is intended as a run through the Quick VHDL system.
The commands relevant to this VHDL system are:

vlib *library_name* this command creates a library for the analyzed designs.
(you will need a library called "work")

vcom *design_file.vhdl* the VHDL compile command
vcom -source *design_file.vhdl* will print the source line and then the error message

vdel *design_unit* deletes the design unit from the library

vsim no arguments - starts up simulator - allows you to select library and design unit. The control window also allows you to compile **You can do everything from this window** or use the specific Commands. You can even bring up a text editor to enter your VHDL.

vdir [-lib <library_name>] [<entity_name>] lists contents of a library

vmap [<logical_name>] [<path>] defines a mapping between a logical library and a library directory
qhmap work ~/ee762/pr_step2_lib

STEP 1) In a terminal window on the Red Hat Systems do the following:
(--Bring up a terminal window.)

Insure that you have a path set to access the mentor tools. Execute
>echo $PATH
In response to this command you should get
PATH=/opt • • • with /opt/local/mentormaster/modeltech/bin
some where in the path

>printenv | grep MGC
In response to this command you should get an appropriate response for your account.

If you do not get these (you may get more but that is ok), then add the following to your *.login* file (at a point after the "setenv PATH ...")

source /opt/local/mentormaster/SETUP.MODELSIM

STEP 2) Create a directory for you work in this class and possibly even subdirectories for home-work and one for the project. Possibly ece762 and hw as the subdirectory. Change directory to that directory and create a file with the following contents: (the remainder of this handout assumes you name the file, hw1.vhdl)

```
ENTITY  first_test  IS
END  first_test;
ARCHITECTURE  one  OF  first_test  IS
SIGNAL  phi1, phi2 :  BIT;
BEGIN
   PROCESS
   BEGIN
       WAIT FOR 10 NS;
       phi1 <=  '0';     phi2 <= '1';
       WAIT FOR 10 NS;
       phi1 <=  '1';     phi2 <= '0';
   END PROCESS;
END one;
```

This file can be created with a standard text editor or through the editor in the Modeltech GUI. The editor is under FILE- -> NEW - -> Source - ->VHDL

STEP 3) In the directory for your work and contianing the file you just entered, you need to create a VHDL library. To do this execute

-- start up the system
>vsim&
Under the file pulldown choose NEW→Library
A popup will ask for the Library name and the physical name – by default they are both "work"

Or from the command line you could have issued the command

>vlib work

Then you can compile your design (this can also be done from the simulator window when you start it but try the command from the command line)

>vcom hw1.vhdl

In the GUI choose COMPILE- -> COMPILE

A popup will allow you to choose hw1.vhdl for compilation.

NOTE: If you compile the unit from the command line it will not appear in library work until you (re)state the simulator.

STEP 4) Now we want to simulate the design for 200 ns.

Using the "Simulate" pulldown, choose "Start Simulation"
Expand the + for "work" and choose the **entity** first_test

Change the "Resolution" to ns (BE SURE TO DO THIS)
Unclick the optimization box.
Now click **OK.**

The VIEW or ADD pulldowns in the main window is used to activate the other windows. The available windows are Source, Structure, Variables, Processes, Signals, Wave, List
To see a waveform (or listing) for a signal, activate the Objects window by clicking on "Objects" and then create a wave window.

View --> Wave . . .

You can add all the signals to the waveform (or list) using the Add pulldowns and the Wave and List in the choices (With the "Objects" window highlighted)

Add → Wave → Signals in design

You will see the names of the signals added to the wave display.
(Within the Wave and List windows you can explicitly add a signal using the "Prop" pulldown.)

STEP 5) You run the simulation using the RUN option of the Simulation pulldown. You can change the value for how long the RUN selection is for in the Runtime Options. You can also enter a command RUN *200 ns* at the command prompt in the transcript window of the GUI.

Run for 200 ns. You should see the waveform generated in the Wave window.

STEP 6) Open a list window View --> List . . . in main window
Add the signals List --> Signals in design in Signals Window
Save the listing to a file File --> Write to File in List window

STEP 7) To print your listing results: Highlight the list window – Under File choose "EXPORT→TABULAR LIST" Name the file hw1.lst for example.
For the waveform use the "PRINT POSTSCRIPT" and print the results to a file which you can view and then print.

STEP 8) Printouts. Print out the Listing and Wave results you created. Also printout the VHDL source that you entered.
Turn in a copy of the VHDL source, the waveform, and the simulation listing file.

NOTE: You can accomplish everything from the GUI window.
To create a new library the menu selection is on File→New→Library…
(Note that you do want a library called work)
To create and edit a new source file of VHDL code it is File→New→VHDL
(Note the simulator also works with Verilog and System C)
(This is actually a very nice editor for entering VHDL code)