PE Refresher Course

Digital Systems and Computers
Part 2 – example problems

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594

594

Figure 594 shows a synchronous digital circuit. The synchronous circuit will sequence through a loop of valid states, with several invalid states outside the loop. The input clock is a symmetric square wave.

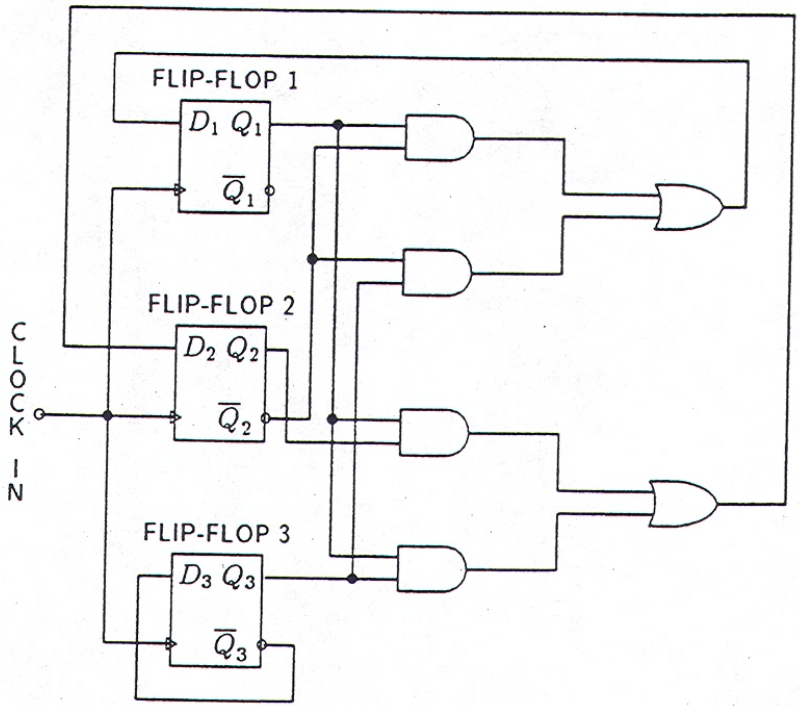

FIGURE 594

Problem specification continued

The rising edge-triggered D-type flip-flops have the following characteristic: (a) Set-up time: $T_{su} = 4\ ns$, (b) hold time: $T_h = 2\ ns$ and (c) clock-to-Q propagation time: $T_{p,min} = 3\ ns \leq T_p \leq 7\ ns = T_{p,max}$

The individual logic gates have the following characteristics: Input-to-output propagation time: $T_{p,min} = 2\ ns \leq T_p \leq 5\ ns = T_{p,max}$

1. Assuming worst-case design, the maximum allowable clock frequency (MHz) that will ensure proper operation is most nearly:

(A) 45.5

(B) 47.6

(C) 58.8

(D) 83.3

(E) 90.9

More problem specification

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(C) 58.8

(D) 83.3

(E) 90.9

1. Worst case loop delay is equal to the minimum allowable clock period.

$$T = T_{FF\ max} + 2(T_{gate\ max}) + T_{su}$$

$$T = 7 \times 10^{-9} + 2(5 \times 10^{-9}) + 4 \times 10^{-9} = 21 \times 10^{-9}$$

$$Freq.max. = \frac{1}{T} = \frac{1}{T_{worst\ case}} = \frac{1}{21 \times 10^{-9}} = 47.6MHz$$

- **THE CORRECT ANSWER IS (B) 47.6 MHz**

Q 2 and 3

2. Assuming worst-case design, the minimum allowable clock frequency (MHz) that will ensure proper operations is most nearly:

(A) There is no minimum.

(B) 45.5

(C) 58.8

(D) 83.3

(E) 90.9

There is none so A

3. The logic circuit has the following number of valid states:

(A) 4

(B) 5

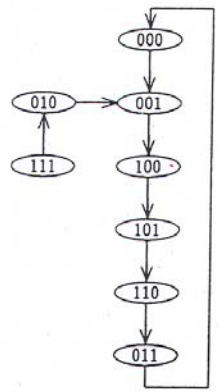
(C) 6

(D) 7

(E) none of the above

3. The Karnaugh map and the state diagram for the circuit is as shown.

PS			$D_A = A\overline{B} + \overline{B}C$	$D_B = AB + BC$	$D_C = \overline{C}$
A	B	C			
0	0	0	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	1	0



• THE CORRECT ANSWER IS (C) Divide-by-6 counter with 6 valid states.

Q 4

4. The logic equation for the D-input of flip-flop 1 is:

(A) $D_1 = Q_1\, Q_2 + Q_2\, Q_3$

(B) $D_1 = Q_1\, (Q_2 + Q_3)$

(C) $D_1 = \overline{Q_1}\, Q_2 + \overline{Q_2}\, Q_3$

(D) $D_1 = Q_1\, \overline{Q_2} + \overline{Q_2}\, Q_3$

(E) $D_1 = \overline{Q_1}\, Q_2 + \overline{Q_2}\, \overline{Q_3}$

4. By inspection of circuit

$$D_1 = Q_1\, \overline{Q_2} + \overline{Q_2}\, Q_3$$

- **THE CORRECT ANSWER IS (D)** $D_1 = Q_1\, \overline{Q_2} + \overline{Q_2}\, Q_3$

Q5

5. If at power up, the circuit comes up in state 111, it will then:

(A) begin normal operation in a valid state, making it a robust self-starting design.

(B) transition between invalid states and never begin proper operation.

(C) transition through invalid states before reaching a valid state, making it a robust self-starting design.

(D) remain in state 111, making it a poor design.

(E) none of the above.

5. See Question 3 solution. The counter transitions through two invalid states before reaching a valid state, making it a robust, self-starting design.

• **THE CORRECT ANSWER IS (C) transitions through invalid states before reaching a valid state, making it a robust, self-starting design.**

Q6

6. A two-input AND gate (with its output called Z) is connected to the Q-output of flip-flop 2 and the Q-output of flip-flop 3 (i.e., $Z = Q_2Q_3$). The new output Z is to be used as a clock input for other logic outside of this problem. In addition, the clock-in signal also may be used as a clock input to other logic. Which of the following statements is true for this configuration?

(A) There will not be skew between clock-in and Z.

(B) Z will not glitch at unwanted times and will not cause extra clock pulses.

(C) The maximum clock frequency of the circuit will increase.

(D) There will be a skew between clock-in and Z and Z may glitch at unwanted times causing extra clock pulses.

(E) There will be a skew between clock-in and Z and the maximum clock frequency of the circuit will increase.

6. The following characteristics hold:

Skew is flip-flop propagation plus gate propagation delay for a max of $7 + 5 = 12\ ns$. As 'BC' passes from '01' in state '101' to '10' in state '110', 'BC' may pass through state '11'. This would create a glitch output. There is skew between clock-in and Z and Z may glitch at unwanted times causing extra clock pulses.

- **THE CORRECT ANSWER IS (D) Skew between clock- in and Z as well as Z may glitch.**

7. Decreases T_{su} and decreases $T_{c-q\,max}$ of the gates and flip-flops

Q 7

(E) There will be a skew between clock-in and Z and the maximum clock frequency of the circuit will increase.

7. Assuming worst-case design, which of the following changes will increase the maximum allowable clock frequency?

(A) Decrease T_{su} and decrease $T_{p,max}$ of the gates and flip-flops.

(B) Decrease T_h and decrease $T_{p,min}$ of the gates and flip-flops.

(C) Decrease T_h and increase $T_{p,min}$ of the gates and flip-flops.

(D) Decrease $T_{p,min}$ and increase $T_{p,max}$ of the gates and flip-flops.

(E) Increase $T_{p,min}$ and increase $T_{p,max}$ of the gates and flip-flops.

7. Decreases T_{su} and decreases $T_{p,max}$ of the gates and flip-flops.

- **THE CORRECT ANSWER IS (A) Decreases T_{su} and $T_{p,max}$.**

8. If the 3-OR circuit has inputs $\overline{Q_1}$, Q_2 and $\overline{Q_3}$, the output when Q_1 is low, Q_2 is high and Q_3 is low will be

$$Y_{low} = \overline{Q_1} + Q_2 + \overline{Q_3} = (Q_1 \cdot \overline{Q_2} \cdot Q_3)_{low}$$

thus Y is low when $Q_1\, Q_2\, Q_3 = 101$.

- **THE CORRECT ANSWER IS (C) $Q_1Q_2Q_3 = 101$.**

Q 8

8. A 3-input OR gate is connected to the three flip-flops. The inputs to the 3-input OR gate are $\overline{Q_1}$, Q_2 and $\overline{Q_3}$ respectively and the output of the 3-input OR gate is Y. During which of the following states will Y be low?

(A) $Q_1Q_2Q_3 = 000$.

(B) $Q_1Q_2Q_3 = 010$.

(C) $Q_1Q_2Q_3 = 101$.

(D) $Q_1Q_2Q_3 = 000$, $Q_1Q_2Q_3 = 010$, and $Q_1Q_2Q_3 = 111$.

(E) $Q_1Q_2Q_3 = 010$, $Q_1Q_2Q_3 = 101$, and $Q_1Q_2Q_3 = 111$.

If any of the inputs are high Y will be high. For Y to Be low all the input need to be low. So the Combination needs to be 101 or C.

Q 9

9. An output Z (as a function of Q_1, Q_2 and Q_3) is high during states $Q_1Q_2Q_3 = 011$, 100, and 110 and low during other valid states of the counter in Figure 594. Which of the following equations will implement output Z with a minimum number of gates?

(A) $Z = \overline{Q_1}\,\overline{Q_2} + \overline{Q_2}\,Q_3$

(B) $Z = \overline{Q_1}\,Q_2Q_3 + Q_1\,\overline{Q_3}$

(C) $Z = Q_1\,Q_2Q_3 + Q_1\,\overline{Q_3}$

(D) $Z = Q_2 + Q_1\,\overline{Q_3}$

(E) $Z = \overline{Q_1}\,Q_2\,Q_3 + Q_1\overline{Q_2}\,\overline{Q_3} + Q_1\,Q_2\,\overline{Q_3}$

9. If the output Z is high during states $Q_1\,Q_2\,Q_3 = 011$, 100, and 110 and low for other states of the counter shown in Figure 594, determine the equation for the output Z. The Karnaugh map is as shown in the figure below where x is a 'don't care' state.

KARNAUGH MAP

Q_1 \ $Q_2\,Q_3$	00	01	11	10
0	0	0	1	x
1	1	0	x	1

The equation for the output Z is then

$$Z = Q_2 + Q_1\,\overline{Q_3}$$

- **THE CORRECT ANSWER IS (D)** $Z = Q_2 + Q_1\,\overline{Q_3}$.

Q 10

10. Using idealized conditions, a major advantage of using Gray-code to assign states in a synchronous state machine is that:

(A) output skew is reduced.

(B) several bits are guaranteed to change simultaneously at some state transition.

(C) more states are available than in an arbitrary state assignment.

(D) output coding is easier than other state assignments.

(E) only one bit at a time changes so that the states can be decoded without glitches.

10. Since all transitions are between squares which are adjacent on the Karnaugh map, all output=1 to output=1. Changes can be covered by a group so that no $1 \rightarrow 0 \rightarrow 1$ glitches can occur.

• **THE CORRECT ANSWER IS (E) Only one bit at a time changes so it is possible to decode without glitches.**

Question 595

A counter consisting of integrated electronic circuits is shown in Figure 595.

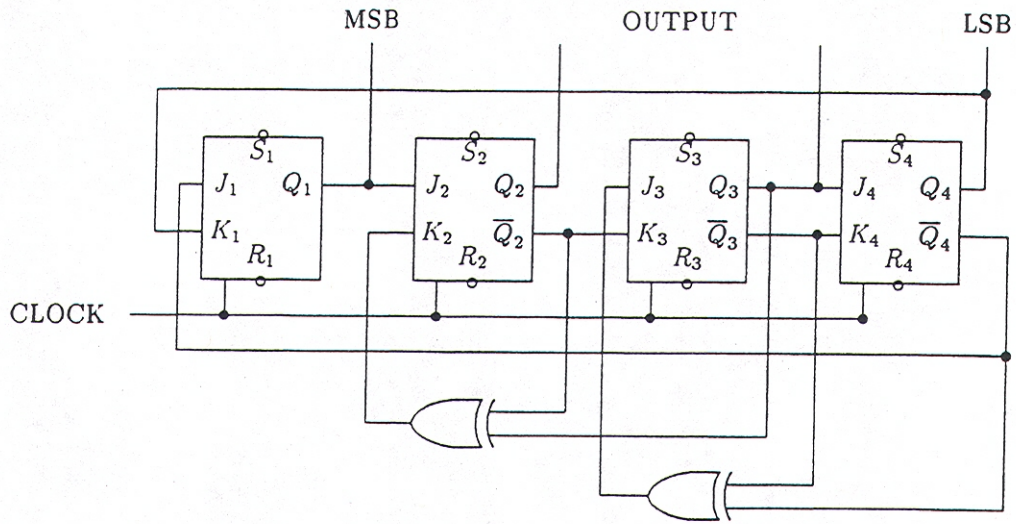


FIGURE 595

DATA LIST:

(a) Clock frequency	1.00 MHz	(d) Clock voltage	logic 0 to logic 1
(b) Clock duty cycle	55%	(e) Inputs to S and R	logic 0 to logic 1
(c) Clock waveshape	pulse	(f) Outputs of Q and $\overline{Q}$	logic 0 or logic 1

Exam questions on 595 – 1 and 2

1. If $S_1 = 0$, $R_1 = 1$, $S_2 = 0$, $R_2 = 1$ $S_3 = 1$, $R_3 = 0$, $S_4 = 0$, $R_4 = 1$, what is the output of the counter in hexadecimal?

(A) 2

(B) 4

(C) B

(D) D

(E) F

2. If S and R are allowed to take on all values, how many combinations of Qs and the next state of Q, $\overline{Q}s$ are available?

(A) 8

(B) 16

(C) 64

(D) 128

(E) 256

SOLUTION:

1. If $S_1 = 0$, $R_1 = 1$, $S_2 = 0$, $R_2 = 1$, $S_3 = 1$, $R_3 = 0$, $S_4 = 0$, and $R_4 = 1$ the binary number is 1101 or decimal 13. Decimal 13 equals D in the hexidecimal numbering system.

- THE CORRECT ANSWER IS (D) D

2. The possible number of combinations of Q and $\overline{Q}$ must be 4×4 or 16.

- THE CORRECT ANSWER IS (B) 16

Exam questions on 595 – 3 & 4

3. What is the maximum frequency of the LSB in the count?

(A) 2 MHz

(B) 1 MHz

(C) 550 kHz

(D) 500 kHz

(E) 256 kHz

4. For each step of the count, the output is available for most nearly which of the following times?

(A) 0.275μs

(B) 0.5μs

(C) 1.0μs

(D) 1.1μs

(E) 2.0μs

3. The maximum frequency of the LSB is

$$\text{LSB} = (1/2) \times \text{clock rate} = (1/2)\ \text{MHz} = 500\ \text{kHZ}$$

- **THE CORRECT ANSWER IS (D) 500 kHz**

4. If the LSB digit changes at a rate of 500 kHz, the counter steps every cycle or an output every 1 μs.

- **THE CORRECT ANSWER IS (C)** 1 μs

Exam questions on 595 – 5 & 6

5. The memory elements in the circuits are:

(A) exclusive OR gates

(B) T flip-flops

(C) D flip-flops

(D) S-R flip-flops

(E) J-K flip-flops

6. Which of the data from the DATA LIST are necessary and sufficient to calculate the next state outputs from the counter?

(A) (e) and (f) only

(B) (c) and (f) only

(C) (a), (b), and (c) only

(D) (a), (c), and (e) only

(E) (a), (b), (c), (d), and (e) only

Answers 5, 6, 7, 8

5. The memory elements are J-K flip-flops.

- **THE CORRECT ANSWER IS (E) J-K flip-flops**

6. The output og Q and $\overline{Q}$ as well as S-R inputs are required, (e) and (f).

- **THE CORRECT ANSWER IS (A) (e) and (f) only.**

7. From Figure 595, the state equation for $Q_2(t+1)$ is

$$Q_2(t+1) = J_2\overline{Q}_2 + \overline{K}_2 Q_2$$

where from Figure 595

$$J_2 = Q_1, \text{ and } \overline{K}_2 = \overline{\overline{Q}_2 \oplus Q_3}$$

By reduction or mapping

$$\overline{K}_2 Q_2 = [\overline{\overline{Q}_2 \oplus Q_3}]Q_2 \Rightarrow Q_2\overline{Q_3}.$$

- **THE CORRECT ANSWER IS (B)** $Q_2(t+1) = Q_1 \cdot \overline{Q_2} + Q_2 \cdot \overline{Q_3}$

8. Using the state equation

$$Q_3(t+1) = \overline{Q}_3 \cdot Q_4 + Q_2 \cdot Q_3$$

it can be shown that the correct states are given by column (a) of the truth table.

- **THE CORRECT ANSWER IS (A) (a)**

Exam questions on 595 – 7 & 8

7. The state equation for $Q_2(t+1)$ is:

(A) $Q_2(t+1) = \overline{Q}_1 \cdot Q_2 + \overline{Q}_2 \cdot Q_3$

(B) $Q_2(t+1) = Q_1 \cdot \overline{Q}_2 + Q_2 \cdot \overline{Q}_3$

(C) $Q_2(t+1) = Q_1 \cdot Q_2 + \overline{Q}_2 \cdot \overline{Q}_3$

(D) $Q_2(t+1) = \overline{Q}_1 \cdot \overline{Q}_2 + Q_2 \cdot Q_3$

(E) $Q_2(t+1) = Q_1 \cdot \overline{Q}_2 + Q_2 \cdot Q_3$

8. The state equation for $Q_3(t+1)$ is

$$Q_3(t+1) = \overline{Q}_3 \cdot Q_4 + Q_2 \cdot Q_3$$

Which of the following truth tables represents $Q_3(t+1)$ after one clock pulse?

Q_2	Q_3	Q_4	(a)	(b)	(c)	(d)	(e)
0	0	0	0	0	0	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	1	0	0
0	1	1	0	0	0	0	0
1	0	0	0	0	0	1	0
1	0	1	1	1	1	1	1
1	1	0	1	0	1	1	1
1	1	1	1	1	1	1	0

(A) (a)

(B) (b)

(C) (c)

(D) (d)

(E) (e)

Exam questions on 595 – 9 & 10

9. The counter is set to start with a count of hex number C. Which of the following hex numbers will be displayed after the next clock pulse? NOTE: Assume S and R are in an appropriate state for counting.

(A) 4

(B) 5

(C) C

(D) D

(E) It cannot be determined from the information given.

10. The inputs to S and R while counting should be:

(A) tied to ground only

(B) tied to logic 0

(C) tied to logic 1

(D) left floating or tied to ground

(E) left floating or tied to the clock.

9. If the counter is set to hexidecimal C, binary 1100 and decimal 12, with $Q_1 = 1$, $Q_2 = 1$, $Q_3 = 0$, and $Q_4 = 0$, the values of $Q_i(t+1)$ are

$$Q_1(t+1) = 1 \quad Q_2(t+1) = 1 \quad Q_3(t+1) = 0 \quad \text{and} \quad Q_4(t+1) = 0.$$

The counter remains in the state 1100 or C.

- **THE CORRECT ANSWER IS (C) hexidecimal C**

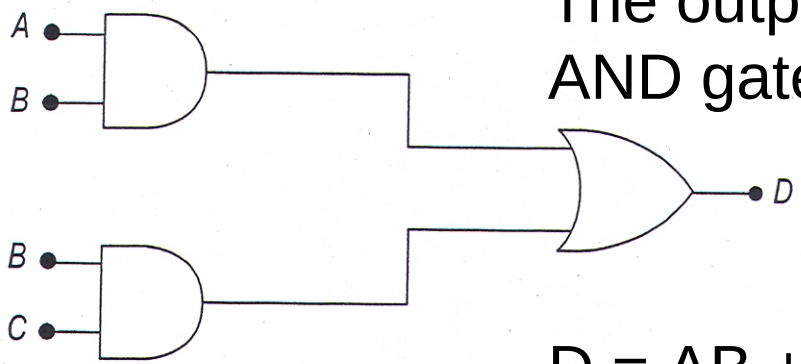
10. S and R should be tied to logic 1.

- **THE CORRECT ANSWER IS (C) tied to logic 1.**

Afternoon exam questions

117. The output D in the circuit is:

(A) $B(A + C)$
(B) $(A + B)(B + C)$
(C) $\overline{A}\overline{B} + \overline{B}\overline{C}$
(D) $(\overline{A} + \overline{B})CB$



Simply look at the gate Structure and by inspection
The output of the top AND Gate is AB

The output of the lower AND gate is BC

D = AB + BC = B(A + C)

ANOTHER

118. The function $F = (\overline{A} + B)(\overline{B} + \overline{C})(A + C)$ can be expressed as the following sum of products:

(A) $F = ABC + A\overline{B}C$
(B) $F = ABC + \overline{A}\,\overline{B}C$
(C) $F = AB\overline{C} + A\overline{B}C$
(D) $F = AB\overline{C} + \overline{A}\,\overline{B}C$

Sum of products is taking all the literal of the equation And writing them as an OR of ANDed terms.

A problem like this can best be solved by expanding out
= (A'B' + A'C' + BB' + BC') (A + C)
= (A'B' + A'C' + BC') (A + C)
= (A'B'A + A'C'A + BC'A + A'B'C + A'C'C + BC'C
= ABC' + A'B'C

CONTINUED

- If the expansion does not show the answer map them onto a Karnaugh Map and then simplify.
- Truth table can also be used but are somewhat time consuming.

Another afternoon example

503. A 16-bit floating point word has a format as shown in the following table.

Byte 0								Byte 1							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
S	E							M							
	MSb						LSb	MSb							LSb

In the table, S is a sign bit with S = 1 indicating a value less than zero; E is a 7-bit excess-64 exponent of a power of 2; and M is an 8-bit mantissa that is a fractional part of unity. MSb and LSb denote the most significant and least significant bits of each byte in the word. A 16-bit word corresponding to $(4000)_{16}$ represents a numeric value that is most nearly:

(A) 0.0
(B) 0.5
(C) 1.0
(D) 2.0

503 answer

- 4000 = 0100 0000 0000 0000
- S = 0
- Exp=100 0000 = 64 and in excess 64 is 0
- Mantissa is 0
- Value calculation is $-1^{s} (M * 2^{E-64})$
- Value is $0 * 2^{0} = 0.0$

- Answer is A

Question 504

504. An 8-bit microcontroller has an instruction set architecture as indicated in the table. The microcontroller uses a 3-bit instruction word with the following eight instructions:

Opcode	Mnemonic	Function	Description
000	JMP	PC⇐ACC	Jump to location in ACC
001	INC	ACC⇐ACC+1	Increment accumulator
010	ADD	ACC⇐ACC+B	Add B port data to accumulator
011	OUT	C⇐ACC	Output data to C port latch
100	CLR	ACC⇐0	Zero the accumulator
101	NOT	ACC⇐~ACC	Ones complement the accumulator
110	SHR	ACC[6:0] ⇐ACC[7:1] ACC[7] ⇐0	Shift accumulator 1 bit to the right
111	SHL	ACC[7:1] ⇐ACC[6:0] ACC[0] ⇐0	Shift accumulator 1 bit to the left

Make no assumptions concerning the initial content of the registers in this question. Assume that all data values are unsigned 8-bit numbers. Assuming that overflow does not occur, the proper code sequence to multiply the contents of the accumulator by 8 is:

(A) SHL, SHL, SHL
(B) SHR, SHR, SHR
(C) CLR, INC, SHL, SHL, SHL
(D) ADD, ADD, ADD, ADD, ADD, ADD, ADD, ADD

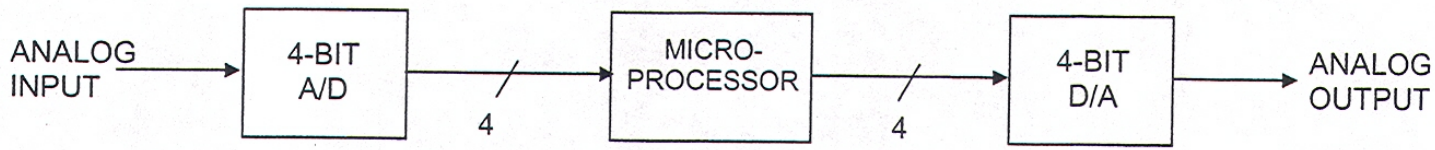
504 answer

- When you shift left it is the same a multiplying by 2 or 10 in binary
- So shl, shl, shl
- Multiply by 2, then by 2 (or x4), then by 2 (or by 8)

Question 505

505. The microprocessor-based data acquisition system shown below samples an analog signal, processes it digitally, and then converts the processed signal back to analog form. The system uses data converter circuits with the following characteristics:

A/D: 4-bit offset binary, unity gain, bipolar –5 to +5 V; –5 V corresponds to $(0000)_2$
D/A: 4-bit offset binary, unity gain, unipolar, +10 V; 0 V corresponds to $(0000)_2$



For an input voltage of +2.0 V, the A/D converter output code is most nearly:

(A) $(0011)_2$
(B) $(0100)_2$
(C) $(1011)_2$
(D) $(1101)_2$

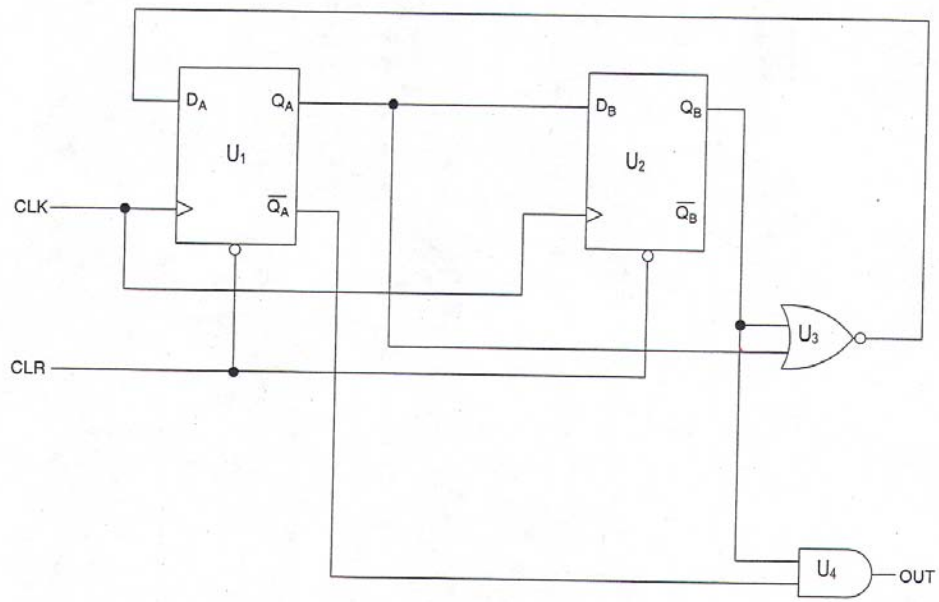
Answer 505

- The step size is 10 V/16 = 0.625 V
- Since the encoding runs from -5v to +5v and each step is 0.625
- 2V is at 70% on the scale or 7V above the base
- 7v / 0.625 v = 11.2 which is most nearly decimal 11 or binary 1011
- And answer C

Question 507

507. The propagation delay from CLK to OUT can be represented as the propagation delay through which gates?

(A) $\max(U_1, U_2) + U_4$
(B) $U_1 + U_2 + U_3 + U_4$
(C) $U_1 + U_2 + U_4$
(D) $U_1 + U_2$

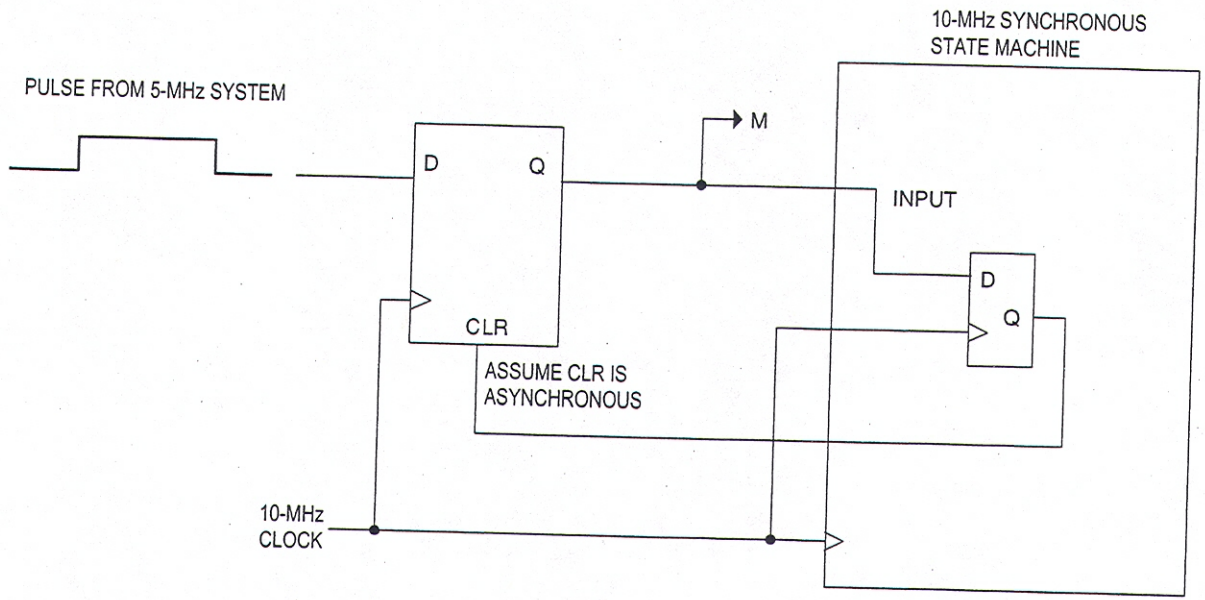


Answer 507

- For clk-to-out must consider what drives out
- First you would have the delay of U4 which drives out
- The inputs to U4 come from the flip flops, so it would be the slowest of the two flip-flop outputs plus the delay through U4
- Or the max (U1, U2) + U4
- It is the max of U1, U2 as they are parallel
- Answer A

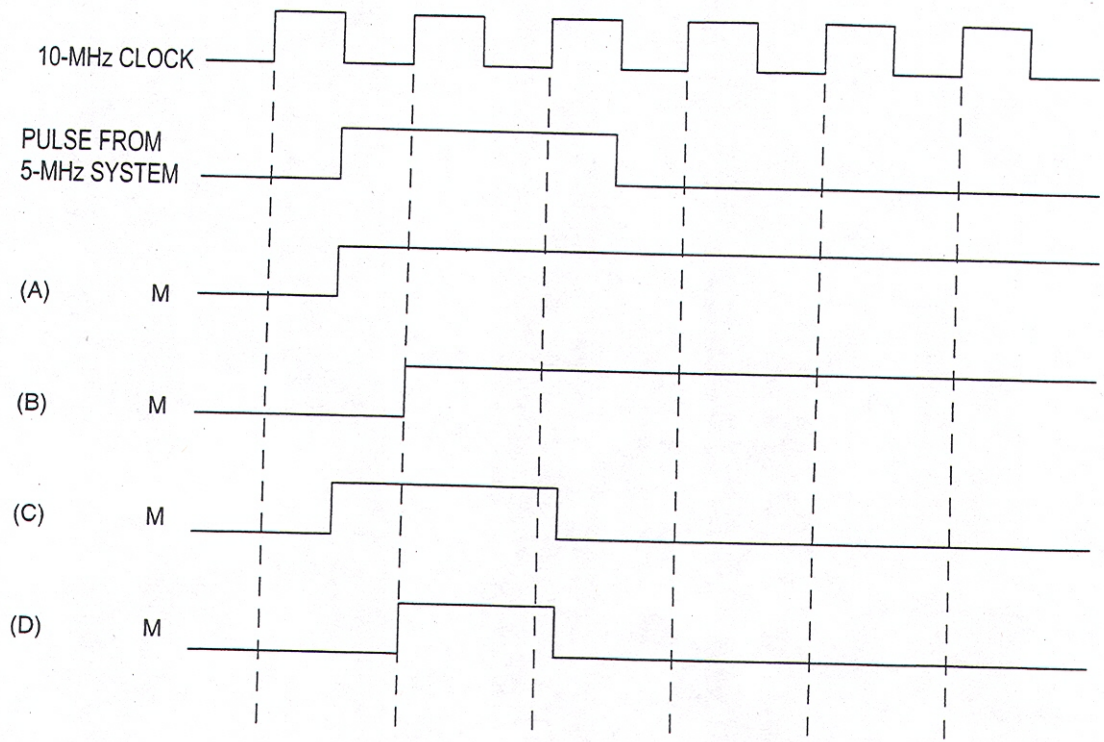
Question 513

513. The following circuit is used to synchronize an input from a slower system. Assume that the D flip-flops are positive edge triggered with zero second setup time.



513 continued

The most appropriate timing diagram describing the behavior of an input is:

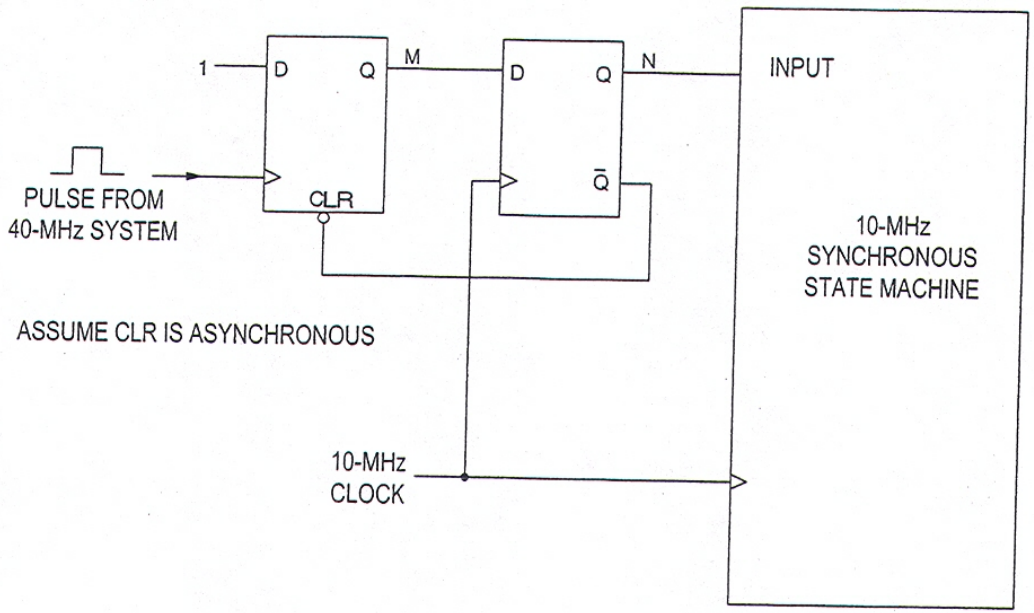


513 answer

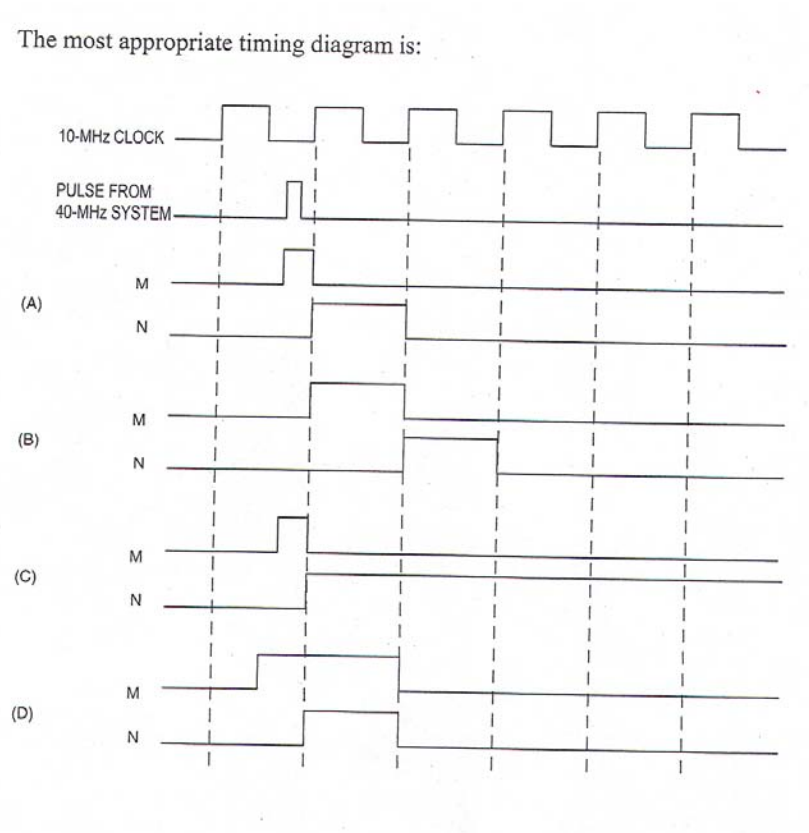
- The output M will not change until a rising edge of clock. This eliminates responses A and C as they coincide with the falling edge.
- B is not correct as the signal is also an input to the internal F/F in the state machine which feeds back to the clear input of the external F/F.
- Once M is asserted it will be clock to the output of this internal F/F will go high clearing the external F/F.
- Thus M is high (or asserted) for 1 clock period.

Question 514

514. For the system shown assume the flip-flops are positive edge triggered with a setup time of zero seconds.



Question 514 continued

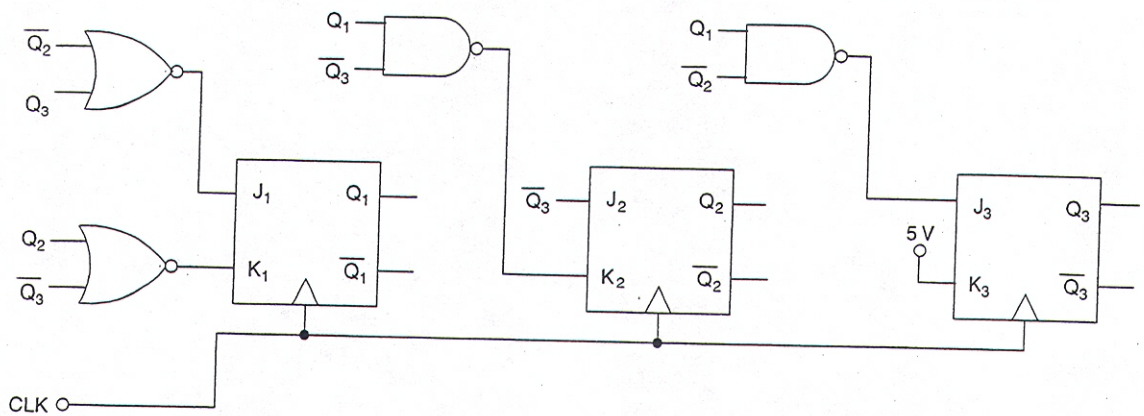


- Will latch a 1 into 1st F/F on rising edge of the pulse.
- On the rising edge of clk will propagate this through 2nd F/F to the system and clear the 1st F/F.
- This propagates to the 2nd F/F output on the subseqent clk

Question 516

516. The synchronous digital circuit below has input CLK and output Q_2. Assume positive logic. If the current state of the synchronous circuit is $Q_1Q_2Q_3 = 100$, the next state will be:

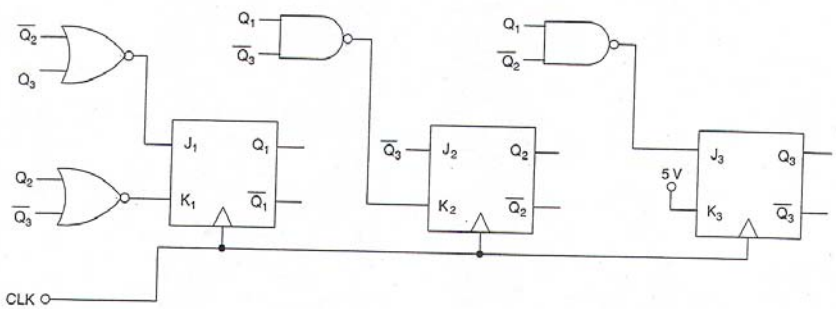
(A) 010
(B) 011
(C) 100
(D) 110



Question 516 answer

516. The synchronous digital circuit below has input CLK and output Q_2. Assume positive logic. If the current state of the synchronous circuit is $Q_1Q_2Q_3 = 100$, the next state will be:

(A) 010
(B) 011
(C) 100
(D) 110

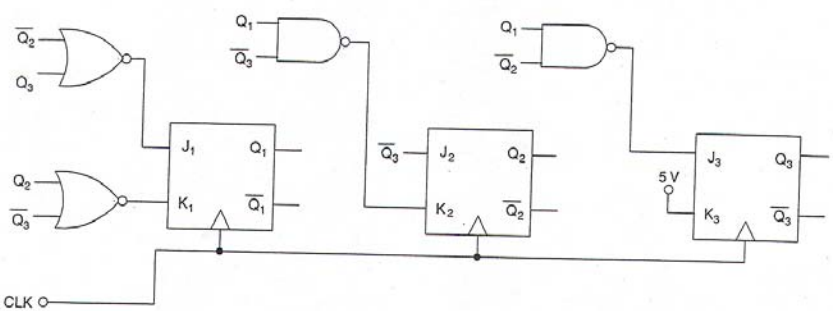


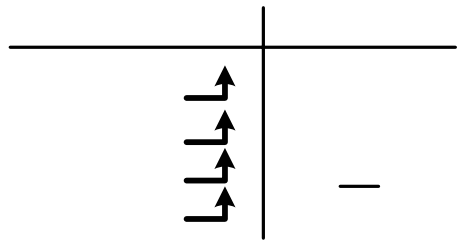
Question 516 answer

- Current state and J/K f/f transition table

516. The synchronous digital circuit below has input CLK and output Q_2. Assume positive logic. If the current state of the synchronous circuit is $Q_1Q_2Q_3 = 100$, the next state will be:

(A) 010
(B) 011
(C) 100
(D) 110





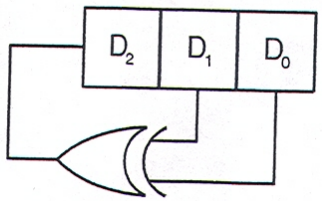
- So next state will be 1 1 0

Question 517

517. A synchronous counter circuit is implemented using a 3-bit Linear Feedback Shift Register (LFSR) as shown below. During the rising edge of each clock pulse, the LFSR shifts the register contents from the D_i position to the D_{i-1} position.

Assume that the LFSR is initialized with $D_2D_1D_0 = 001$. The number of states the circuit cycles through is most nearly:

(A) 2
(B) 3
(C) 7
(D) 8



- States: 001→ 100 → 010 → 101 → 110 → 111 → 011 and back to the beginning
- Answer is C

Question 518

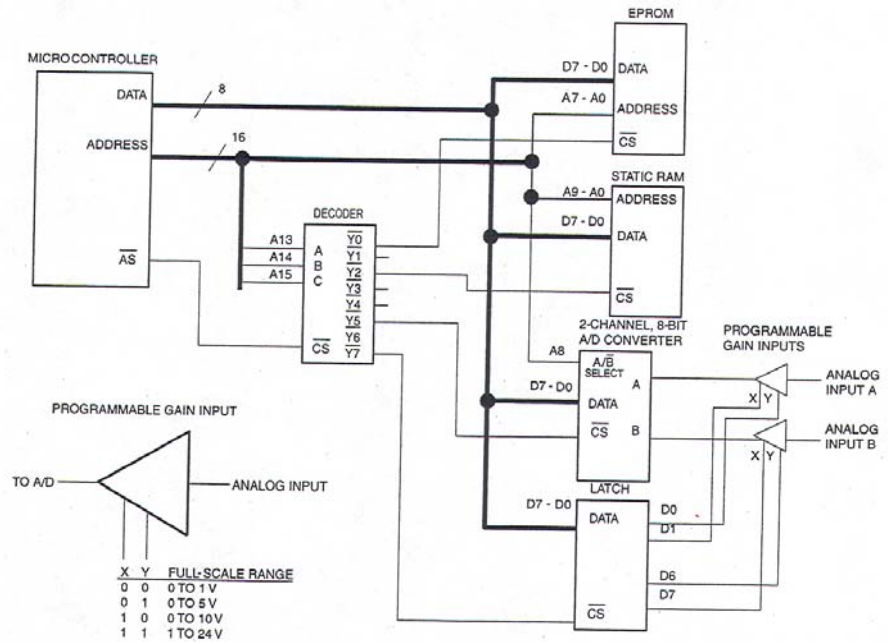
518. A CPU contains a control unit that is designed with one-hot encoding in an attempt to maximize clock speed. This synchronous circuit cycles through 16 distinct states and produces 32 control signals. If the circuit is based on D flip-flop cells, the number of cells required is most nearly:

(A) 4
(B) 5
(C) 16
(D) 32

- One hot encoding means only one state bit is at logic-1 for each state and thus uses 1 F/F for each state. 16 F/F are needed.

Question 506

)6. A microcontroller system with an A/D converter is shown in the figure below. Assume that A15 and D7 are the most significant bits of the address and data buses.



To set the programmable gain of analog input A for a full-scale input of 0 to 10 V, and input B for a full-scale input of 0 to 5 V, you must:

(A) send the data $(01)_{16}$ to address location $(C000)_{16}$
(B) send the data $(02)_{16}$ to address location $(DFFF)_{16}$
(C) send the data $(83)_{16}$ to address location $(FFFF)_{16}$
(D) send the data $(42)_{16}$ to address location $(FFFF)_{16}$

Question 506 answer

- The chip select for the latch that controls input to the programmable gain inputs is asserted when the address is 111x xxxx xxxx xxxx
- This gets us the either answer C or D
- We want full scale 0-10 for A requiring a 10 for bits D1 D0 and full scale 0-5 for B requiring a 01 on D7 D6 so data word is 01xx xx10
- Answer is D as $42 is 0100 0010