

Final Report

Inverter Simulations and Testing

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Abstract

The parallel operation of power inverters is investigated in this paper. A simulation of a single power inverter was created in PSCAD. This simulation details results experimentally derived. Matlab was also used to simulate various scenarios for the output voltage waveforms. Experimental laboratory results include the gate signals and analysis of inrush current for an induction machine. Additional information is provided on the low voltage DC system used to power an inverter. Our research has concluded that a low cost modular system of inverters would be possible with the use of a microcontroller.

Table of contents

Abstract.....	1
Table of contents.....	2
List of Figures.....	3
Introduction.....	4
Purpose.....	4
Discussion.....	5
General modular design theory.....	5
PSCAD Simulation.....	9
Simulations in MATLAB.....	13
NEC Code.....	21
Battery Charger.....	29
Results.....	32
Conclusion.....	37
Appendix A – PSCAD Data files.....	38
Appendix B – Battery Charger Schematics.....	48
Appendix C – Group Tasks.....	50
References.....	51

List of Figures

Figure 1: PSCAD Simulatuion Schematic.....	11
Figure 2: Output Voltage and Gate Signal for PSCAD Simulation.....	12
Figure 3: Input/Output Current for PSCAD Simulation.....	13
Figure 4: Two sine waves generated at the exact same time and added together.....	15
Figure 5: Phase shift of $\pi / 2$ for each inverter.....	16
Figure 6: Change in wave number from 2 to 5.....	17
Figure 7: Sine waves with a 100 volt DC offset.....	18
Figure 8: One inverter fails or is turned off.....	19
Figure 9: Daisy Chain method for power systems per <i>NEC</i>	23
Figure 10: Output voltage transients during the inrush current period for an induction machine.....	33
Figure 11: Gate signal for high voltage side transistors in inverter.....	34
Figure 12: Inverted output to drive complimentary pair of transistors.....	34
Figure 13: Bottom side of the 700W inverter.....	35
Figure 14: Top side of the 700W inverter.....	36
Figure 15: Schematic 1 of 2 (Battery Charger).....	48
Figure 16: Schematic 2 of 2 (Battery Charger).....	48
Figure 17: Setup with variable transformer.....	49

Introduction

As a continuation from ECE 582, we chose to investigate the effects of two inverters connected in a parallel configuration. All the testing was preformed in a lab designated for us in Caldwell. This laboratory provided us with the oscilloscope and workspace needed.

The inverters used in our research were the Xantrex Xpower 700 watt and 1500 watt power inverters. After disassembling the 700 watt inverter, we were able to see the switching power transistors, step up transformers, as well as the high and low voltage circuits more closely. Testing was performed for various outputs with each inverter. Theories were formulated with respect to how the inverters would react under a certain load. With the use of a vacuum cleaner and computer monitors, we were able to view the inrush current and voltage drop during the turn on transient period. Our research also included the importance of exact phase matching between inverters while in parallel and the modifications necessary for each inverter in parallel operation. A consideration of the *NEC* must also be utilized in the design of a modular inverter system. Our research performed in ECE 683 was to test the parallel operation of power inverters. We have utilized simulations and laboratory testing to aid with our research.

Purpose

The purpose of this project was to investigate the operation of the DC to AC power inverter. The concept of a modular system with multiple inverters will be considered once the basic operation of a single inverter is studied. Currently, the SW4024 inverter manufactured by Trace Engineering (Reference #4) includes the capability to connect two inverters in a series or parallel configuration for more voltage

or current respectively. This system utilizes an interconnection between the inverter modules and two digital signal processors. The Trace Engineering inverter is a relatively high cost solution for an inverter system. This cost factor is the motivation behind studying the parallel connection between inexpensive inverters for a higher power output. A better control over system cost and a more efficient system would be realized if a modular system was built. A modular inverter system design must also incorporate safety features and fault tolerance in the event of malfunction.

Discussion

General modular design theory

Every component of an inverter system must be sized correctly in order to keep costs down and efficiency high. There are a number of ways of achieving this goal. The first way would be a continuous upgrading and downgrading process. New components could be traded in for other components every time the load requirements in the system changed. While this method would keep efficiency high, it is obviously not practical from a cost or time standpoint. The second way would be to design the system with excess capacity. This excess would allow for future expansion of the system without the necessity to completely change components of the system. In this case, there would be an additional cost of purchasing larger components and efficiency would be slightly lower since the components are too large for the job. However, this is currently the most common method for DC to AC inverter systems. A third method for achieving this goal would be building a system that is sized correctly which has the ability to quickly and cost effectively change with the load. This goal can be realized with a modular power system design.

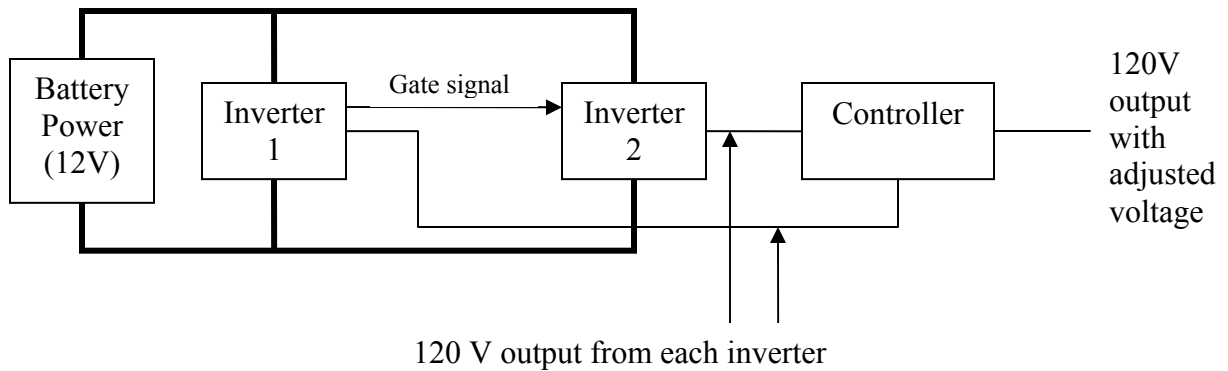
Each block of a modular power system is comprised of a battery array and DC to AC power inverter. Each block should have a total power rating between 500 and 1000 VA. A system would need many modular blocks if the power rating of each block was less. Conversely, if the power rating was greater, then efficiency would decrease from the excess capacity. Blocks of 500 to 1000 VA power rating can be connected together in parallel to obtain large power outputs while keeping efficiency high and cost down due to the modular design. There are several considerations involved in this modular approach. First, a wiring system must be designed with a sufficient overhead for safety with respect to the modular system. Both the DC bus wires from the battery array and the AC load wires must increase in size for each modular block that is added. Second, each inverter in the modular block must be operating at the same frequency and phase since the output is AC voltage sine wave. Third, the system must be designed for safety. The overall modular system must be able to detect and disconnect blocks in the event that one or more modular blocks fails, outputs the wrong voltage, wrong frequency or phase.

There are two methods to operate parallel inverters with the same frequency and phase. One method is to have a master and slave inverter. The master inverter outputs AC voltage that is 'sensed' by the slave inverter. The slave inverter then synchronizes with this AC voltage and begins inverting with the same frequency and phase. A second system would comprise of one master clock module driving every inverter. Using a single clock module would guarantee the synchronous operation of every inverter. However, both systems have their drawbacks. The first system is much more complex. It requires an analog to digital conversion of the AC wave form, then a DSP to analyze the signal and output the correct clock pulses to the inverter. This complexity adds in

cost as well as serviceability. However, this complexity adds two advantages. If one inverter were to fail, the other inverter could still operate, but the system would have a reduced capacity. Also, the inverter has the ability to operate in 'sell back' mode. In this mode, the inverter takes power from the battery array and transmits the power back to the utility grid. Since the inverter can 'sense' the AC waveform, it has can easily synchronize with the utility power. The second method of synchronizing inverters is much less complex. Every inverter is already operating together since there is a master clock module. This resolves the issue of having one inverter synchronize with the other. Since there is no synchronizing involved, the A/D - D/A converter along with the DSP can be eliminated which saves cost and adds to serviceability. However, this simplification has two drawbacks. The first drawback is a redundancy issue. The entire power system would go offline if the master clock module were to fail. One possible remedy to this problem would be a standby clock module. The second drawback is the inability of the system to operate in 'sell back' mode. The system cannot synchronize with the utility power grid since there is no provision in the inverter system to sense the AC waveform. A possible solution to this drawback would be a separate clock module with a DSP that would operate in sell back mode.

A modular wiring system can be accomplished with a central bus and taps for each block on the central bus. To have a completely modular system, both DC and AC wiring should be contained in the central bus. The majority of the central bus will be designed around system integration and safety features with the use of the *NEC*. A primary component in safety is the current handling capability; the system must have a current rating in excess of the sum of each modules output current. The central bus must

also have safety features to guard against exposed wiring when modules are added or removed and to prevent the removal of modules while the system is in operation. The central bus could also contain a simple DSP to ensure proper operation of each module connected. The output frequency, phase and magnitude will be sampled by the DSP for each of the modules. The central bus will utilize hardware to disconnect any/all modules from the system if the module is determined to be malfunctioning by the DSP. The inverter system could then also operate in sell back mode if a DSP is operating within the central bus. This will add functionality to the overall modular system and increase the desirability of the system. The following block diagram shows a theory for parallel operation of inverters.



PSCAD Simulation

PSCAD was used for the simulation of a DC to AC inverter. The PSCAD simulation was created to match as closely with our actual inverter as possible. A DC voltage source of 14.4 volts was used. The schematic for the inverter simulated in PSCAD is shown in figure 1. The switching was accomplished with an H bridge setup with four transistors. The diodes in anti parallel are necessary to protect the transistors from reverse voltage caused by an inductive load. A clock signal is generated at the frequency of 60Hz by an impulse generator. This 60Hz impulse is used to drive a monostable pulse generator. The resulting waveform is a 60Hz square wave with a duty cycle of 50 percent and it is used to drive the gates of the four transistors. Two NOT gates are used to control a complimentary pair of transistors in conduction while the other pair remains off. This sequence repeats and generates the low voltage AC waveform. The output of the transistors was fed into a step up transformer to change the output voltage to 120VAC. A simulated RL load was used to more precisely model an induction machine. See Appendix B for the PSCAD data files. Figure 2 shows the voltage output waveform and the gate signal for the transistors. There is a slight ramp up time of the voltage due to the inductance in the circuit. The ringing at the peak of the voltage also occurs from this inductance. Figure 3 shows the input DC current and the output AC current in the inverter simulation. The AC current closely follows the AC voltage with a slight lagging factor introduced from the inductance. The DC input current remains almost constant, but contains a periodic drop to zero. This drop occurs when the transistors are switching. Since no device has a rise and fall time of zero there will be a slight amount of time before the transistor is fully conducting. This PSCAD simulation

closely models the experimental results obtained from the operation of a vacuum cleaner powered by the DC to AC inverter system.

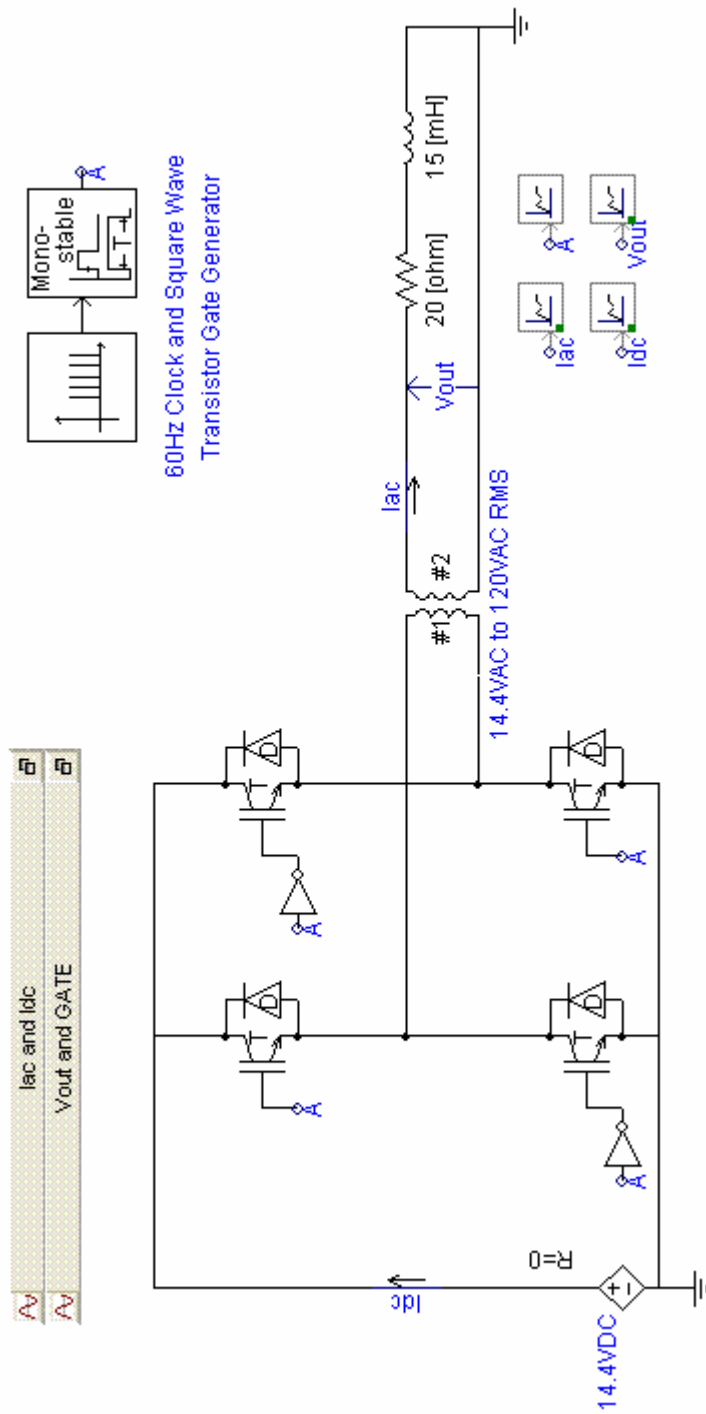


Figure 1: PSCAD Simulatuion Schematic

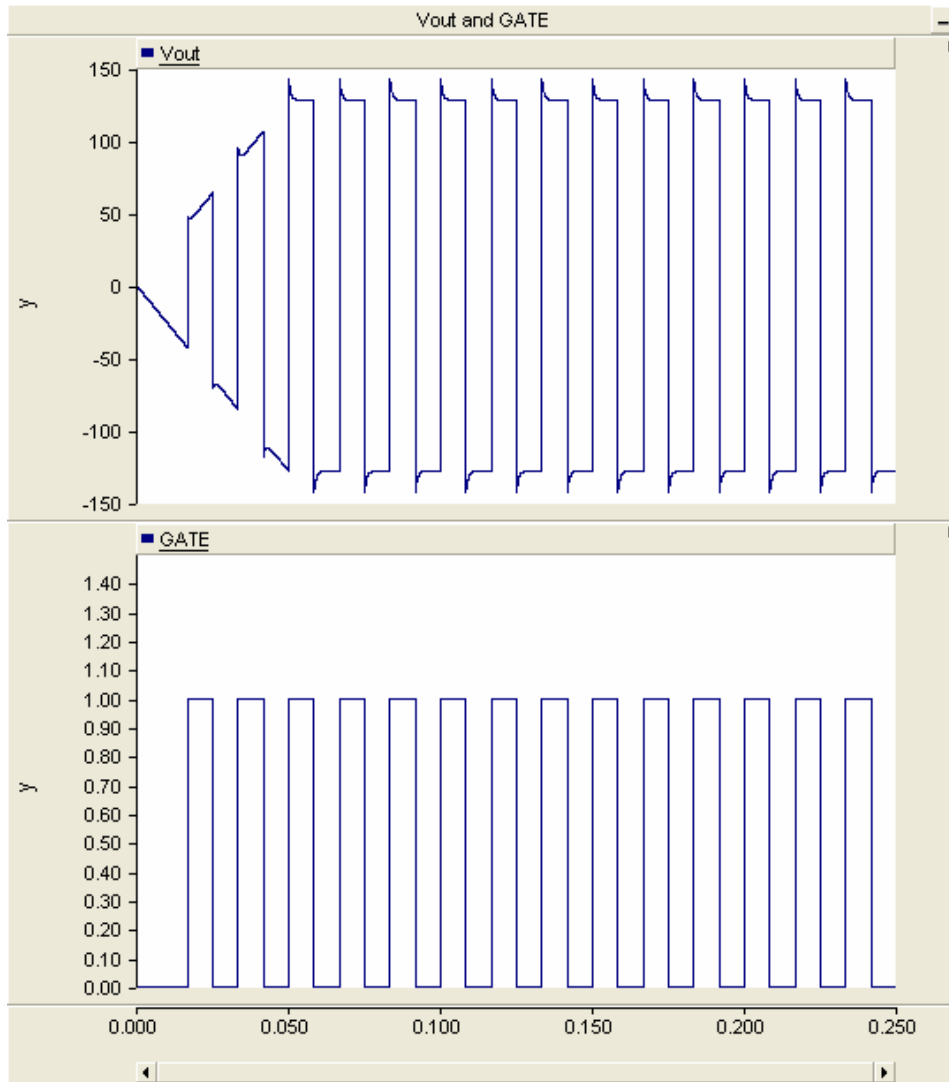


Figure 2: Output Voltage and Gate Signal for PSCAD Simulation

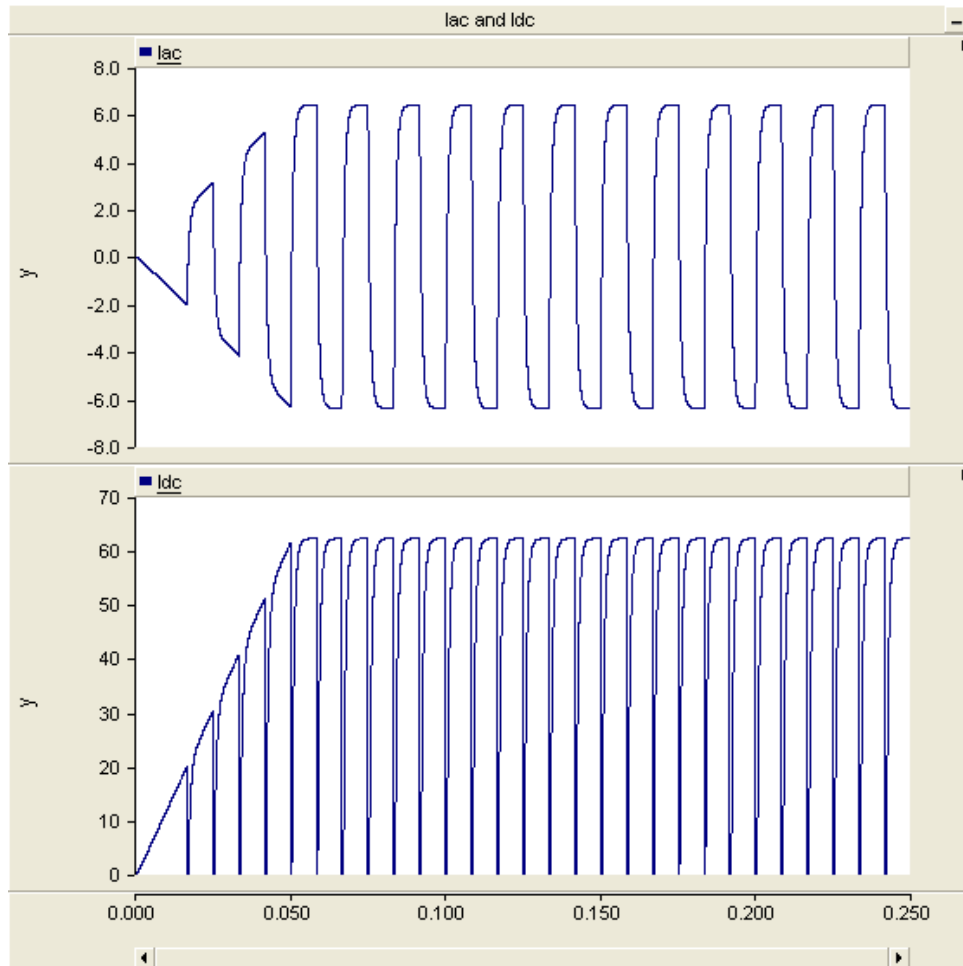


Figure 3: Input/Output Current for PSCAD Simulation

Simulations in MATLAB

In order to obtain more power from an inverter, two of them can be connected in parallel. By operating two inverters in parallel without modification, the voltage will be boosted. These simulations show what would happen to the voltage if there were no controller adjusting the voltage. In order to ensure that the correct voltage is obtained there are certain measures that must be taken into consideration. Using a controller to regulate the amount of voltage from each inverter, it will keep the total voltage output to 120 volts. This will be explained in greater detail further in the report. In order to get the maximum current output, it is essential that the two sine waves have exactly the same

phase and frequency with one another. With the use of Matlab simulation, graphs were generated using a true sine wave. The Matlab code is as follows:

```
% Inverter Phase Shifting

clear;
clc;

x = 0:pi/100:2*pi;
y1 = 120*sin(2*pi*x);
y2 = 120*sin(2*pi*x);

% % Use to simulate one inverter stop working
% for n = 150:1:201;
%     y2(1,n)=0;
% end

for z = 1:1:201;
    y1_ind = y1(1,z);
    y2_ind = y2(1,z);
    if y1_ind == 0;
        if y2_ind == 0;
            y3 = 0;
        end
    else
        y3 = y1_ind+y2_ind;
        array(1,z) = y3;
    end
end
array;
plot(x,array,x,y1,x,y2)
```

Figure 4 demonstrates two sine waves generated at the exact same time and the two inverters put in parallel. Each sine wave is generated as follows, where x is the time that the sine waves are run:

```
x = 0:pi/100:2*pi;
y1 = 120*sin(2*pi*x);
y2 = 120*sin(2*pi*x);
```

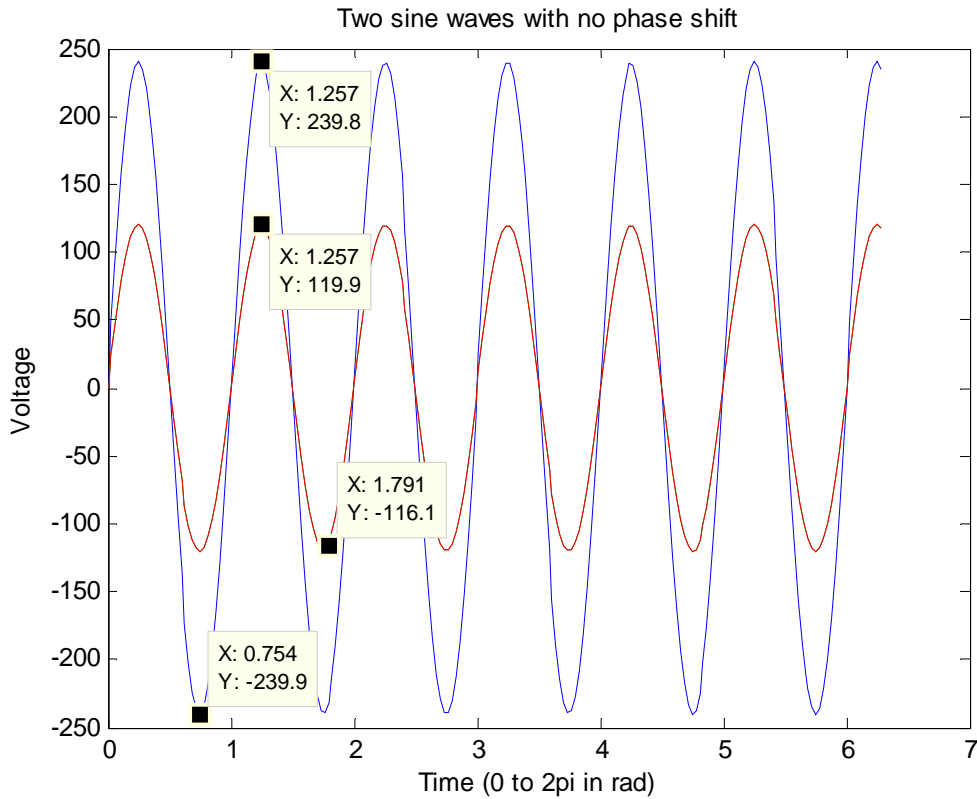


Figure 4: Two sine waves generated at the exact same time and added together.

In figure 4, markers are placed to show the voltage at each peak on the amplitude. Only two sine waves are seen because the two inverters that are generating a 120 volt wave from each inverter are generated at the same moment. Without any type of voltage control a combination of 240 volts or 480 volts peak to peak is created. Samples for each wave are taken from 0 to 2π with a step of $\pi/100$.

If the sine waves are not matched correctly in phase, it seems to be possible to still achieve a voltage jump. This will cause problems when operating equipment however. Figure 5 gives a phase shift of $\pi/2$ for the two inverters. In this graph the maximum voltage can be seen to be different than the voltage in figure 4.

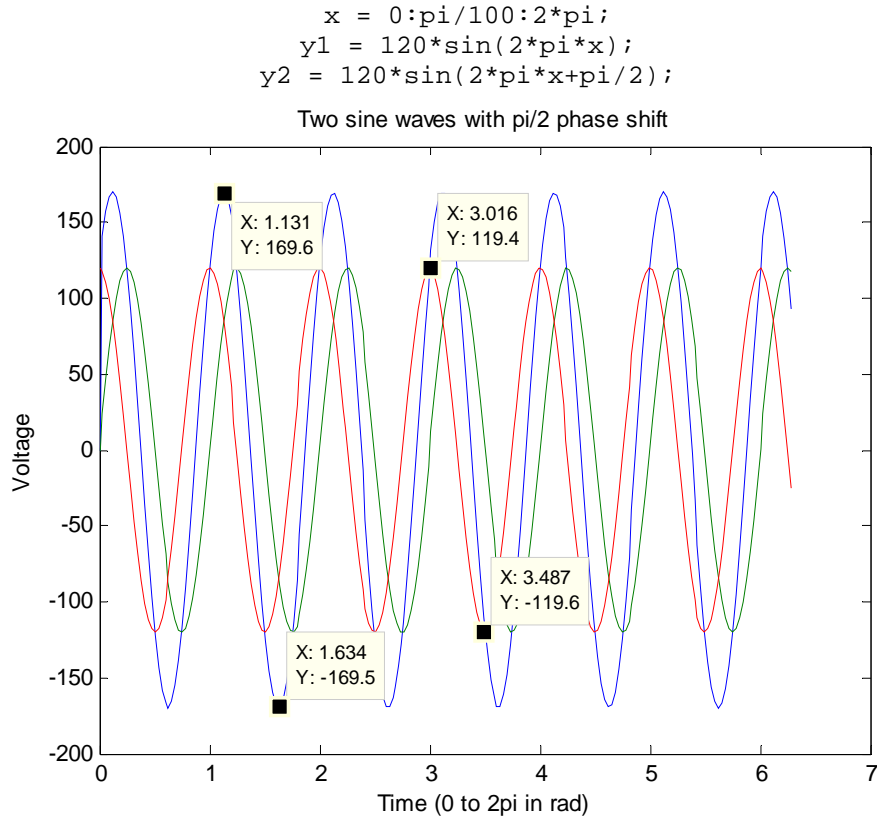


Figure 5: Phase shift of $\pi/2$ for each inverter.

The same amplitude of 120 volts AC power from each wave still applies but the combined waves only give a maximum voltage of about 170 volts. This same figure demonstrates the importance of making sure that the waves are within phase of one another.

Another important factor to obtain an accurate sine wave generated at the same phase is the consistency of the desired final wave. If the device changes the wave number of one wave or changes the DC offset, there will be a malfunction of any unit connected and probably to the inverter itself. Figure 6 shows the problems with a change in wave number from one wave to the other. The sine waves are simulated as follows:

```

x = 0:pi/100:2*pi;
y1 = 120*sin(2*pi*x);
y2 = 120*sin(5*pi*x);

```

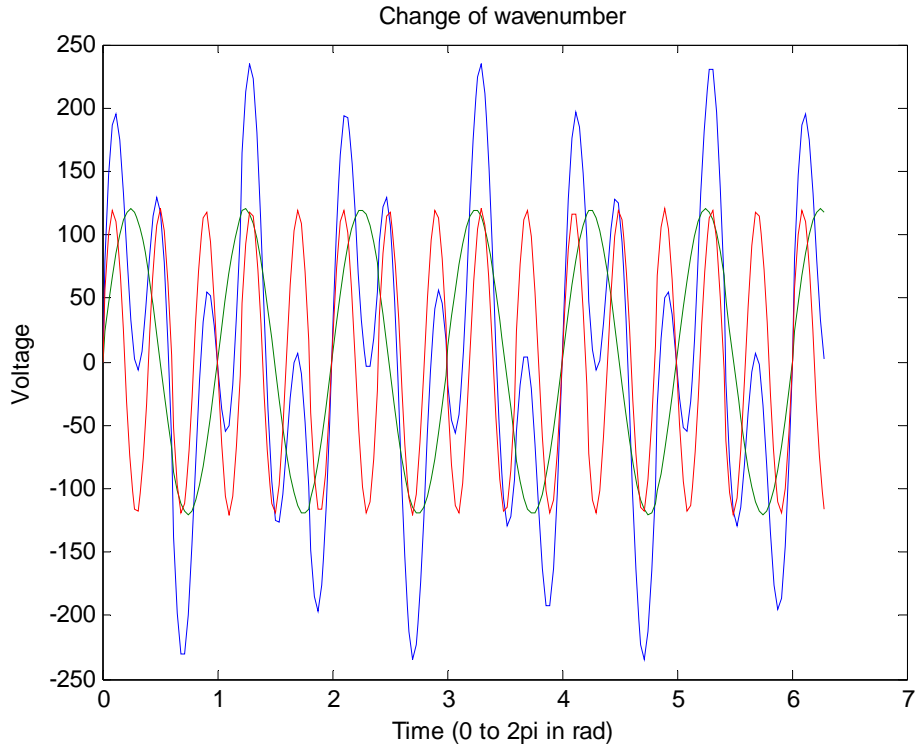


Figure 6: Change in wave number from 2 to 5.

The frequency of y_2 is much faster than that of y_1 . This allows for the two inverters to confuse each other and generate a wave with many difficult properties. Different amplitudes and sporadic frequencies are all generated. Although this has been simulated, it has not been tested first hand in the lab. Other unknown problems could also arise when trying to produce an output similar to this one.

A second problem that must be avoided is a DC offset. Figure 7 shows a large DC offset of 100 volts. This voltage is a little extreme but shows the severity of the wave change rather well. The following sine waves used are:

```
x = 0:pi/100:2*pi;
y1 = 120*sin(2*pi*x);
y2 = 120*sin(2*pi*x)+100;
```

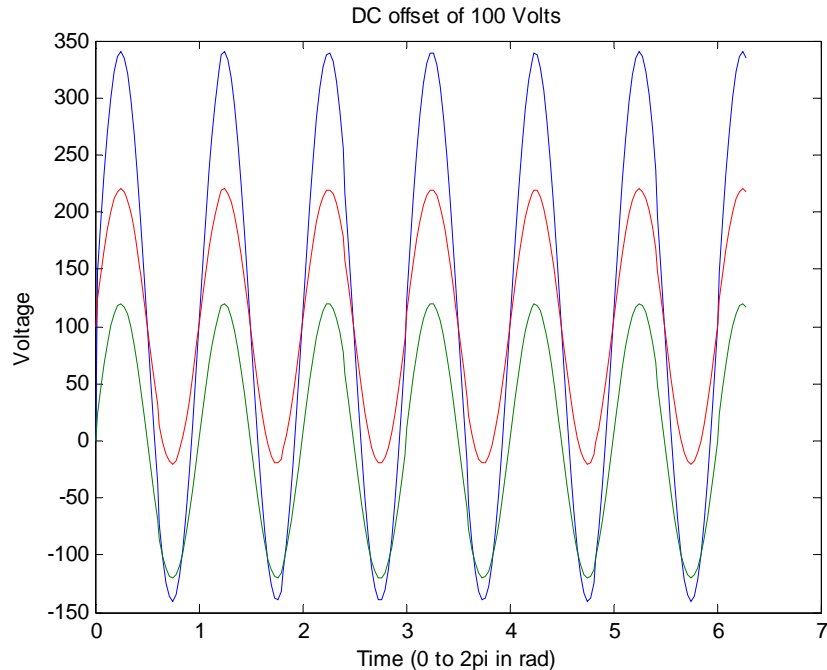


Figure 7: Sine waves with a 100 volt DC offset.

This graph shows that if two waves have a large DC offset without any phase shift, they will combine to give an interesting output. The voltage ranges from nearly 340 volts to about -140 volts. This wave still has a difference of 480 volts peak to peak but oscillates at different speeds above zero volts and below zero volts. Although it is believed that it could be a problem for any device operating from these inverters, it has not been tested out in the lab or researched further. Any device with a motor would most likely either, start and stop continuously without ever reaching its full potential, or not run at all.

Once each inverter has been designed to have the same phase another problem can be addressed. If one inverter was to fail while an appliance or device was operating, it is most likely that there would be a large jump in current and a drop in the voltage. The controller must then readjust the voltage output to meet the needs of 120 volts. Figure 8

shows what the voltage would look like if one of the inverters is suddenly turned off. The sine waves generated are the same as figure 4 and have no phase shift:

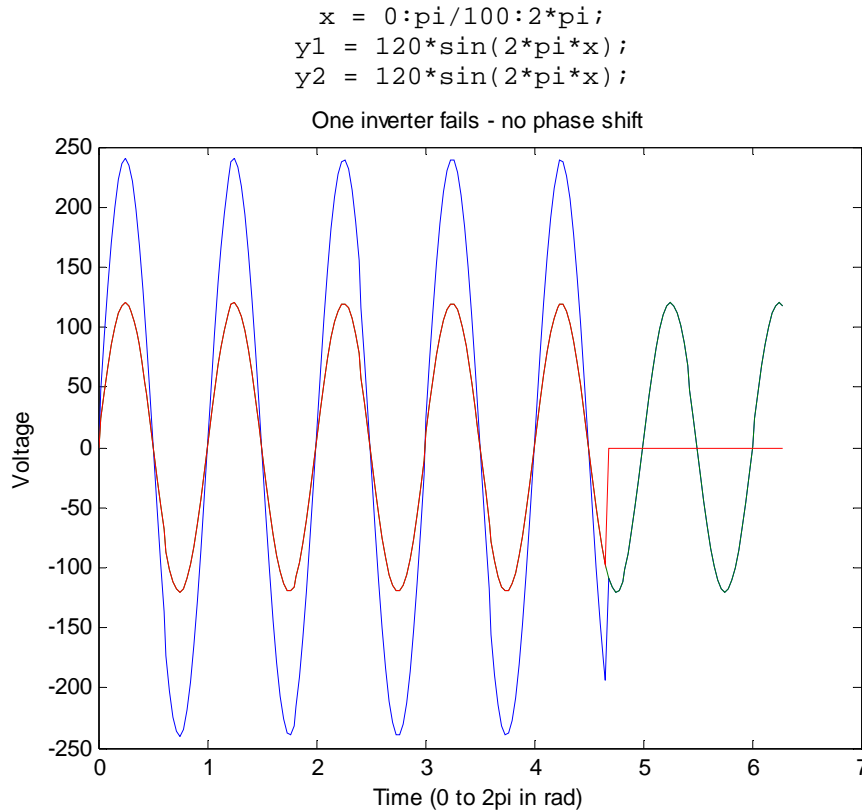


Figure 8: One inverter fails or is turned off.

The figure shows that the voltage will drop to half of the total output and will try to continue to operate the load. Depending on the load this may not be as clean of a wave. There will most likely be jumps and imperfections in the wave due to the draw of current that will be produced. The load will most likely shut off and the single inverter will fault and shut down. This has not been tested first hand in the lab but is a good topic that could be researched farther down the road.

In order to achieve a sine wave without phase shifts, the high voltage output transistors must be synchronized to allow for an identical wave. By detaching the gates

from one of the circuit boards and attaching them to the gates of the other inverter, it is possible to run off the same clock from one inverter. This could be a simple way to control the phase of each inverter without involving a microcontroller. Other more expensive inverters may control the phase by adjusting their clocks accordingly to achieve this same output. Sensors that determine the amount of current being drawn and adjusting the phases to work together could do this.

From this data we can see it is not possible to just attach two inverters in parallel. The sine waves from two inverters in parallel must be controlled in some way. Otherwise the voltages will just add together. The device must realize how many inverters are being connected and reduce the voltage in some way and allow the current to be boosted rather than the voltage. For example, if two inverters are connected, then each inverter must only put out 60 volts. This will add up to 120 volts AC. The current, however, will be doubled allowing for more things to be connected to the inverters. This seems to only be possible to do with some sort of controller. A controller will allow for the flexibility of adding and detaching inverters. If some sort of circuit was created and the voltages of the inverters were passed through that, it must be some sort of variable circuit.

However, creating a circuit would be very difficult. Taking into consideration must be each inverters individual properties. The amount of wattage supplied, current draw, and many other factors are important. Then creating the variable circuit must include a transformer that would be compatible with each inverter. This seems like a very difficult task and would be easier and better preformed by a controller.

Controlling the voltage is not only important for a sinusoidal wave. After experimenting with the inverters, we found that they do not actually put out a sine wave

or a modified sine wave as we expected. The two inverters tested produced a square wave. It is interesting to see that many devices can be powered by such a wave. Another interesting aspect was that the square wave did not carry the same duty cycle as well for the upper and lower peaks. This is important because the inverter still has the ability to power motors. After charging the batteries to the appropriate voltage and current level, the vacuum cleaner that was used ran perfectly.

Despite a square wave, phase matching and voltage boosting/reducing is still extremely important when paralleling these inverters. Generating the square waves at the same time allows for the peaks to be at the correct voltage and not disturb the input/output of the device that is being powered by the inverters in parallel. Otherwise the inverters will begin to cancel each other out. If the inverters were exactly out of phase, the voltage would be reduced to zero. A controller would need to be used as well in order to reduce the voltage peaks to the correct level and not exceed 120 volts.

NEC Code

Copper conductors are recommended for almost all photovoltaic system wiring [110-5]. Copper conductors have lower voltage drops and good resistance to corrosion. Aluminum or copper-clad aluminum wires can be used in certain applications, but the use of such cables is not recommended—particularly in dwellings. All wire sizes presented below refer to copper conductors. The *NEC* requires 12 American Wire Gage (AWG) or larger conductors to be used with systems under 50 volts [720-4]. Article 690 ampacity calculations yielding a smaller conductor size might override Article 720 considerations, but some inspectors are using the Article 720 requirement for dc circuits. The *NEC* has little information for conductor sizes smaller than 14 AWG, but Section 690-31d

provides some information. The widely available Underground Service Entrance Cable (USE-2) is suggested as the best cable to use for module interconnects, however, single-conductor, Type UF (Underground Feeder — Identified (marked) as Sunlight Resistant), Type SE (Service Entrance), or Type USE (Underground Service Entrance) cables are permitted for module interconnect wiring [690-31(b)]. When manufactured to the UL Standards, USE-2 has a 90°C temperature rating and is sunlight resistant. The “-2” marking indicates at wet-rated 90°C insulation, the preferred rating. Additional markings indicating XLP or XLPE (cross-linked polyethylene) and RHW-2 (90°C insulation when wet) ensure that the highest quality cable is being used [Tables 310-13,16, and 17]. USE-2 is acceptable to most electrical inspectors. The RHH and RHW-2 designations frequently found on USE-2 cable allow its use in conduit inside buildings. USE or USE-2 cables, without the other markings, do not have the fire-retardant additives that SE cable has and cannot be used inside buildings.

Module connectors that are concealed at the time of installation must be able to resist the environment, be polarized, and be able to handle the short-circuit current. They shall also be of a latching design with the terminals guarded. The equipment-grounding member, if used, shall make first and break last [690-32, 33]. The UL standard also requires that the connectors for positive and negative conductors should not be interchangeable. Where several modules are connected in series and parallel, a terminal block or bus bar arrangement must be used so that one source circuit can be disconnected without disconnecting the grounded (on grounded systems) conductor of other source circuits [690-4(c)]. On grounded systems, this indicates that the popular “Daisy Chain” method of connecting modules may not always be acceptable, because removing one

module in the chain may disconnect the grounded conductor for all of those modules in other parallel chains or source circuits. This becomes more critical on larger systems where paralleled sets of long series strings of modules are used. Generally, 12- and 24-volt systems can be daisy chained, but higher voltage systems should not be. Figure 8 shows the acceptable and unacceptable way to daisy chain the system.

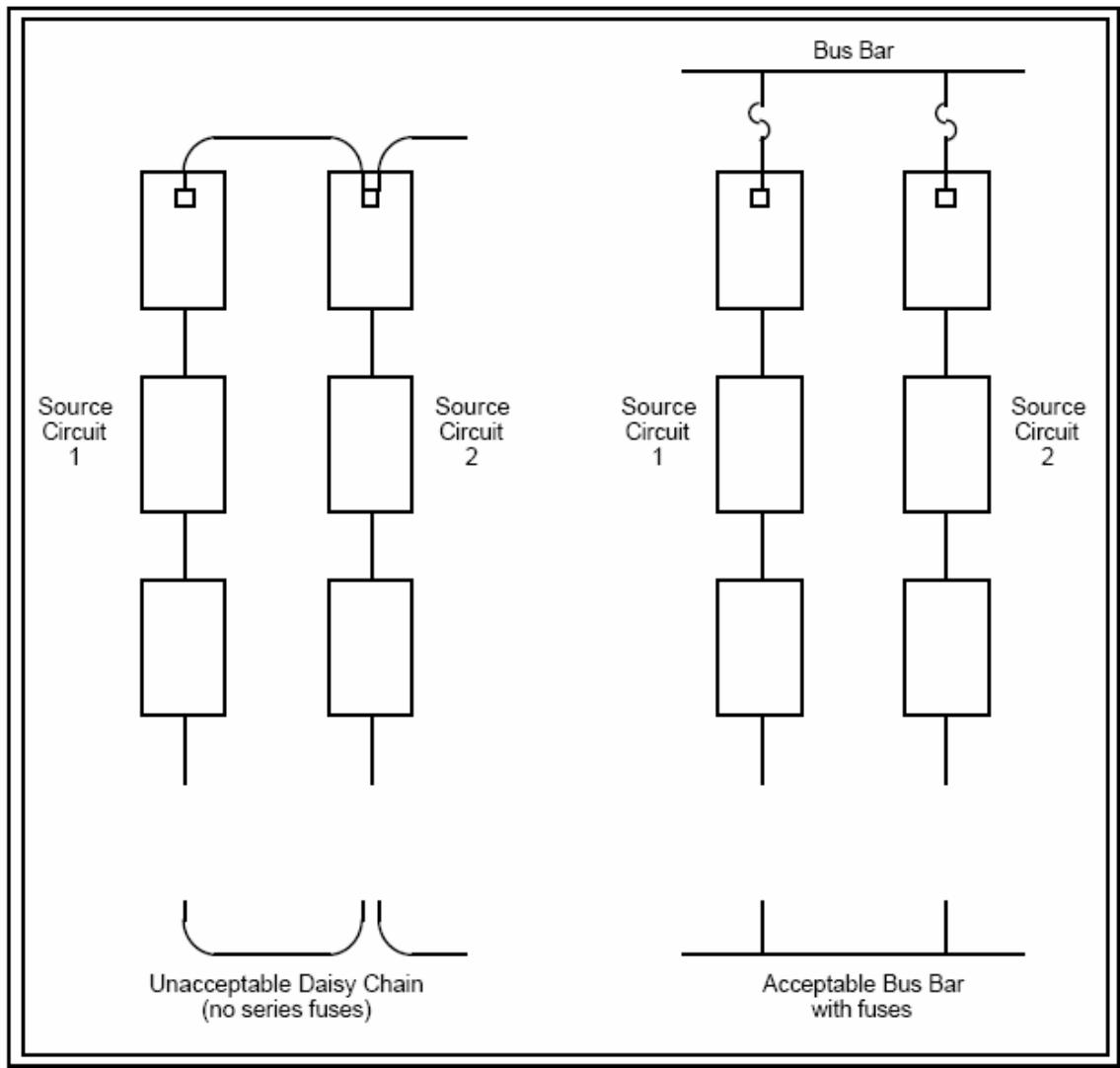


Figure 9: Daisy Chain method for power systems per NEC

The *NEC* established color coding for electrical power systems many years before either the automobile or electronics industries had standardized color codes. PV systems are being installed in an arena covered by the *NEC* and, therefore, must comply with *NEC* standards that apply to both ac and dc power systems. In a system where one conductor is grounded, the insulation on all grounded conductors must be white or natural gray or be any color except green if marked with white plastic tape or paint at each termination (marking allowed only on conductors larger than 6 AWG). Conductors used for module frame grounding and other exposed metal equipment grounding must be bare (no insulation) or have green or green with yellow-striped insulation or identification [200-6, 7; 210-5; 250-119]. The *NEC* requirements specify that the grounded conductor be white. In most PV powered systems that are grounded, the grounded conductor is the negative conductor. Telephone systems that use positive grounds require special circuits when powered by PV systems that have negative grounds. In a PV system where the array is center tapped, the center tap or neutral must be grounded [690-41], and this becomes the white conductor. There is no *NEC* requirement designating the color of the ungrounded conductor, but the convention in power wiring is that the first two ungrounded conductors are colored black and red. This suggests that in two-wire, negative-grounded PV systems, the positive conductor could be red or any color with a red marking except green or white, and the negative grounded conductor must be white. In a three-wire, center-tapped system, the positive conductor could be red, the grounded, center tap conductor must be white and the negative conductor could be black. The *NEC* allows grounded PV array conductors, such as non-white USE or SE that are smaller than 6 AWG, to be marked with a white marker [200-6] (Reference #5).

Battery cables, even though they can be 2/0 AWG and larger, must be a standard building-wire type conductor [Chapter 3]. Welding and automobile “battery” cables are not allowed. Flexible, highly-stranded, building-wire type cables (USE/RHW and THW) are available for this use. Flexible cables, identified in Section 400 of the *NEC* are allowed from the battery terminals to a nearby junction box and between battery cells. These cables shall be listed for hard service use and moisture resistance [690-74].

The inverter output (120 or 240 volts) must be connected to the ac distribution system in a manner that does not create parallel grounding paths. The *NEC* requires that both the green or bare equipment-grounding conductor and the white neutral conductor be grounded. The *NEC* also requires that current not normally flow in the equipment-grounding conductors. If the inverter has ac grounding receptacles as outputs, the grounding and neutral conductors are most likely connected to the chassis and, hence, to the chassis ground inside the inverter. This configuration allows plug-in devices to be used safely. However, if the outlets on the inverter are plug and cord connected (not recommended) to an ac load center used as a distribution device, then problems can occur. The ac load center usually has the neutral and equipment-grounding conductors connected to the same bus bar, which is connected to the case where they are grounded. Parallel current paths are created with neutral currents flowing in the equipment-grounding conductors. This problem can be avoided by using a load center with an isolated/insulated neutral bus bar, which is separated from the equipment-grounding bus bar. Inverters with hard-wired outputs may or may not have internal connections. Some inverters with ground-fault circuit interrupters (GFCIs) for outputs must be connected in a manner that allows proper functioning of the GFCI. A case-by-case analysis will be

required. A sine-wave inverter should be used to power those circuits requiring GFCI protection.

In stand-alone systems, inverters are used to change the direct current (dc) from a battery bank to 120-volt or 240-volt, 60-Hertz (Hz) alternating current (ac). The conductors between the inverter and the battery must have properly rated overcurrent protection and disconnect mechanisms [240, 690-8, 690-9]. These inverters frequently have short-duration (seconds) surge capabilities that are four to six times the rated output. For example, a 2,500-watt inverter might be required to surge to 10,000 volt-amps for 5 seconds when a motor load must be started. The *NEC* requires the ampacity of the conductors between the battery and the inverter to be sized by the rated 2,500-watt continuous output of the inverter. For example, in a 24-volt system, a 2,500-watt inverter would draw 134 amps at full load (85% efficiency at 22 volts) and 420 amps for motor-starting surges. The ampacity of the conductors between the battery must be 125% of the 134 amps or 167 amps. To minimize steady-state voltage drops, account for surge-induced voltage drops, and to increase system efficiency, some well-designed systems have conductors that are larger than required by the *NEC*. When the current-carrying conductors are oversized, the equipment-grounding conductor must also be oversized proportionately [250-122]. Oversizing the wires for the inverters would also allow the inverters to change sizes if the load was increased and a larger inverter needs to be connected to the emergency panel.

Each piece of equipment in the PV system shall have disconnect switches to disconnect it from all sources of power. The disconnects shall be circuit breakers or switches and shall comply with all of the provisions of Section 690-17. DC rated

switches are expensive; therefore, the ready availability of moderately priced dc-rated circuit breakers with ratings up to 125 volts and 110 amps would seem to encourage their use in all 12-, 24-, and 48-volt systems. When properly located and used within their approved ratings, circuit breakers can serve as both the disconnect and overcurrent device. In simple systems, one switch or circuit breaker disconnecting the PV array and another disconnecting the battery may be all that is required. A 2,000-watt inverter on a 12-volt system can draw more than 235 amps at full load. Disconnect switches must be rated to carry this load and have appropriate interrupt ratings. Again, a dc-rated, listed circuit breaker may prove less costly and more compact than a switch and fuse with the same ratings.

Inverters can have stand-alone, utility-interactive, or combined capabilities. The ac output wiring is not significantly different than the ac wiring in residential and commercial construction, and the same general requirements of the code apply. In the case of utility-interactive systems and combined systems, ac power may flow through circuits in both directions. This two-way current flow will normally require overcurrent devices at both ends of the circuit. The dc input wiring associated with stand-alone or hybrid inverters is the same as the wiring described for batteries. Most of the same rules apply; however, the calculation of the dc input current needs special consideration since the *NEC* does not take into consideration some of the finer points required to achieve the utmost in reliability. The dc input wiring associated with utility-interactive inverters is similar, in most cases, to the wiring in PV source and output circuits. Inverters with combined capabilities will have both types of dc wiring: connections to the batteries and connections to the PV modules.

The procedure presented below for cable sizing and overcurrent protection of that cable is based on *NEC* requirements in Sections 690-9, 690-8, 210-20(a), 215-2, 215-3, 220-10, 240-3(b), and 240-6(a). For circuits carrying currents from PV modules, multiply the short-circuit current by 125% and use this value for all further calculations. For PV circuits in the following examples, this is called the PV 125% calculation. In the 1999 *NEC*, this requirement has been included in Section 690-8, but may also remain in UL 1703. Do not apply this multiplier twice. For dc and ac inverter circuits in PV systems, use the rated continuous currents. AC and dc load circuits should follow the requirements of Sections 210, 220, and 215. The overcurrent device must be rated at 125% of the current determined above. This is to prevent overcurrent devices from being operated at more than 80% of rating. This calculation is called the *NEC* 125%. Cables shall have a 30°C ampacity of 125% of the current determined above to ensure proper operation of connected overcurrent devices. There are no additional deratings applied with this calculation. Based on this determination and the location of the cable (raceway or free-air), a cable size and insulation temperature rating (60, 75, or 90°C) are selected from the *NEC* Ampacity Tables 310-16 or 310-17. Use the 75°C cable ampacities to get the size, then use the ampacity from the 90°C column—if needed—for the deratings. This cable is then derated for temperature, conduit fill, and other requirements. The resulting derated ampacity must be greater than the value first calculated. If it is not greater, then a larger cable size or higher insulation temperature must be selected. The current in overcurrent device is not used at this point to preclude oversizing the cables. The derated ampacity of the cable selected must be equal to or greater than the overcurrent device rating. If the derated ampacity of the cable is less than the rating of

the overcurrent device, then a larger cable must be selected. The next larger standard size overcurrent device may be used if the derated cable ampacity falls between the standard overcurrent device sizes found in *NEC* Section 240-6. Since most overcurrent devices have terminals rated for use with 75°C (or 60°C) cables, compatibility must be verified. If a 90°C-insulated cable was selected in the above process, the 30°C ampacity of the same size cable with a 75°C (or 60°C) insulation must be less than or equal to the initial current calculated. This ensures that the cable will operate at temperatures below the temperature rating of the terminals of the overcurrent device. If the overcurrent device is located in an area with ambient temperature higher than 30°C, then the 75°C (or 60°C) ampacity must also be derated.

Battery Charger

In order to provide a constant power source for the inverters during testing it was necessary to have a 12 volt DC power source that could supply a large amount of current. During the operation of large loads it is possible to draw 60 amps from the 12 volt DC source. We have estimated the load of our vacuum cleaner to be 850W. The output voltage in a typical 12 volt nominal DC source is 14.4 and thus will be used in this calculation:

$$59A = 800W / 14.4V \quad (1)$$

The current of 59 amps is the minimum current needed from the DC source assuming 100% efficiency in the inverter. The car batteries alone would not be able to support a 59 amp current draw for any appreciable amount of time and therefore a battery charger must be used in addition to the car batteries.

The original design of the battery charger was built from a schematic obtained at (Reference #2). The two schematics can be referenced in appendix B. The basic operation of this power supply is as follows.

In schematic #1: 120VAC power flows into the transformer, which steps the voltage down to 21VAC. Two bridge rectifiers then rectify the AC voltage into DC voltage. Two current limiting resistors are used (R1 and R2) to protect the transistor base drive circuit.

In schematic #2: The base drive voltage obtained from the current limiting resistors is used to power a LM7812 12 volt regulator. The ground pin of this regulator is connected to a transistor and variable resistor to allow for some variation around the 12 volt regulator output. The output from the LM7812 is used to supply the base current to drive the main regulating transistors (Q2 – Q5). Resistors R4 – R7 are used to ensure a balanced current from each output transistor.

Many extra ‘features’ of the power supply design were not used in order to simplify the construction. In schematic #1 both indication LED’s were omitted as well as the second power switch for the DC control. In schematic #2 the current meter and resistors were left out and substituted with a current meter directly in series with the output. Presumably the power supply designer did not choose this method because a

current meter to measure large currents is expensive (there was one laying around, so it was utilized).

This DC power supply operated quite well for current ranges up to 20A. The theoretical maximum of the power supply is figured out as follows. The unregulated DC voltage from the bridge rectifiers is 21 volts. The maximum voltage drop across the current limiting resistors (R1 and R2 of schematic #1):

$$6.6 \text{ V}_{\text{drop}} = 21\text{V} - 14.4 \text{ V} \quad (2)$$

when the voltage regulator is set to provide 14.4 volts. To drop of 6.6 volts across the two series resistors R1 and R2 the current draw:

$$0.71\text{A} = 6.6\text{V} / 9.2\Omega \quad (3)$$

Therefore, 0.71A is the maximum current that can be supplied by the LM7812 before the supply voltage falls due to the current limiting resistors. Assuming the 2N3055 transistors have an average DC current gain (H_{fe}) of 30 (Reference #3) then the total output current:

$$21.3\text{A} = 0.71\text{A} * 30 \quad (4)$$

The battery charger voltage would drop once the current draw became more than 21A. A different regulation scheme had to be used since the current drawn was greater than 60 amps. The new regulation scheme used was less technically advanced but was able to provide the necessary power. The new design utilized two transformers. The first

transformer was a variable transformer and the second transformer was the main transformer of the power supply. See appendix B, schematic #3. The variable transformer was used to supply the main transformer. The main transformer was connected directly to the output of the variable transformer, and the output of the main transformer was connected to the bridge rectifiers, which provided our DC power. The variable transformer was adjusted until the output from the rectifier was 14.4 volts. This is a rather crude method of regulation because the circuit had to be manually adjusted, but it provided all of the needed current.

Results

The output gate signal needed to parallel inverters together was found by testing the high and the low voltage sides of the inverter circuitry. The gate output on the high voltage side was correct to utilize for the paralleling of inverters. This output matched the output viewed at the AC output. The output was somewhat different than what was expected originally. It was expected that the inverter would output something similar to a sine wave, since that is what is expected at a household receptacle. But instead the output was a square wave with a varying duty cycle. The frequency of the output wave was still 60Hz however. The next step was to plug a device in to the receptacle of the inverter to test the output with a load. First, a computer monitor was plugged in, resulting in the duty cycle of the output waveform to change closer to 50% while maintaining the 60Hz frequency. Next, an induction machine would need to be tested to study how the output voltage changed due to the inrush current. The theory was that the current would spike, thus lowering the voltage, and then the output would become steady and the voltage would rise back up a little. By utilizing a vacuum cleaner, the theory was tested. Figures

9 and 10 show the output right at the inrush current and the steady state output. The steady state output is also the output at the gate to which two inverters could be connected in parallel. Figure 11 shows the inverted output at the gate, which is used to drive the opposite pair of transistors. The theory was correct and the large 1500 watt inverter was able to run this vacuum cleaner and provide the necessary inrush current.

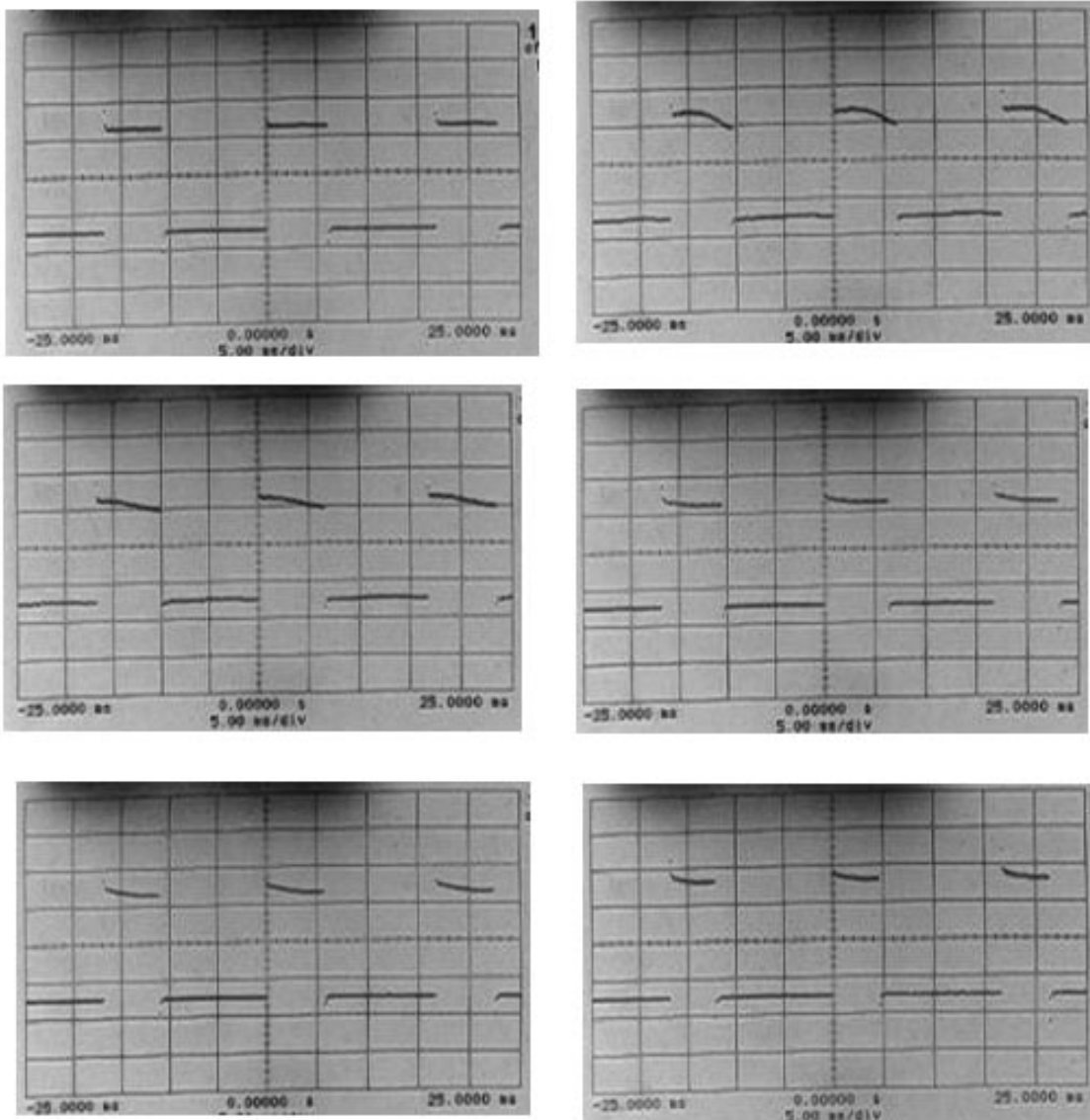


Figure 10: Output voltage transients during the inrush current period for an induction machine

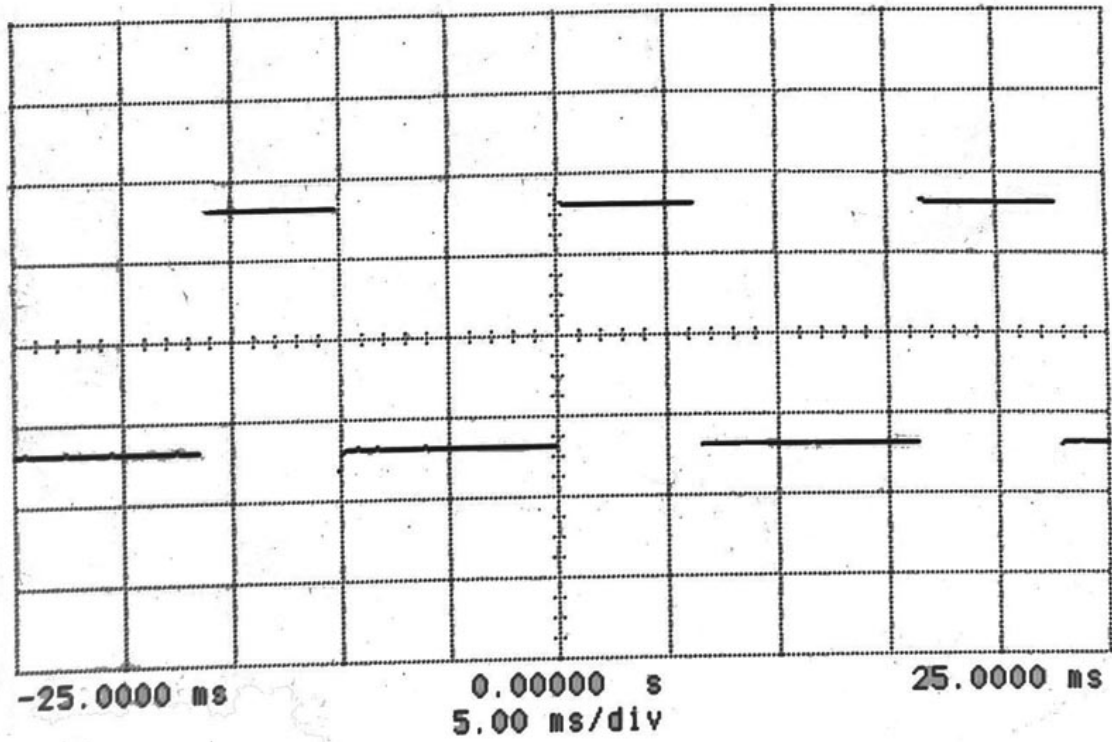


Figure 11: Gate signal for high voltage side transistors in inverter

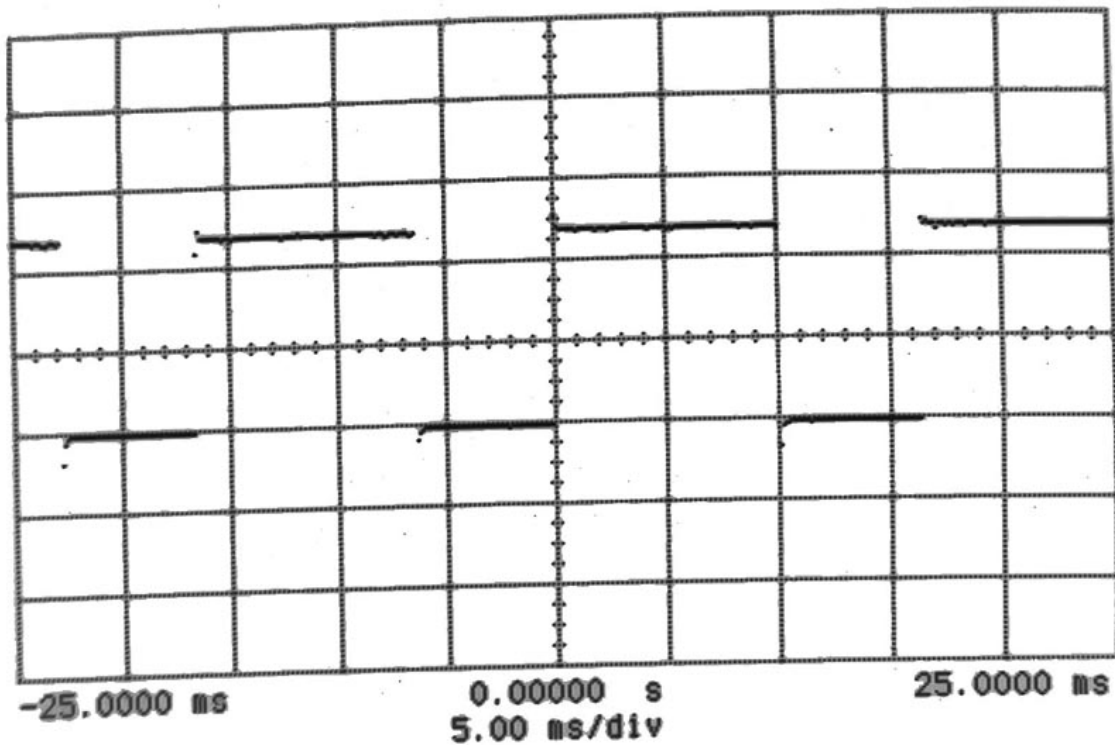


Figure 12: Inverted output to drive complimentary pair of transistors

As mentioned above, it would be possible to parallel two inverters by connecting at the gates that matched the output of the inverter on the AC side. Figure 12 shows the bottom side of the inverter where the connection would need to be made. The red circled connections are the high voltage transistor gate signals. The other inverter(s) would function slave units and have the gate signals disconnected for correct parallel operation.

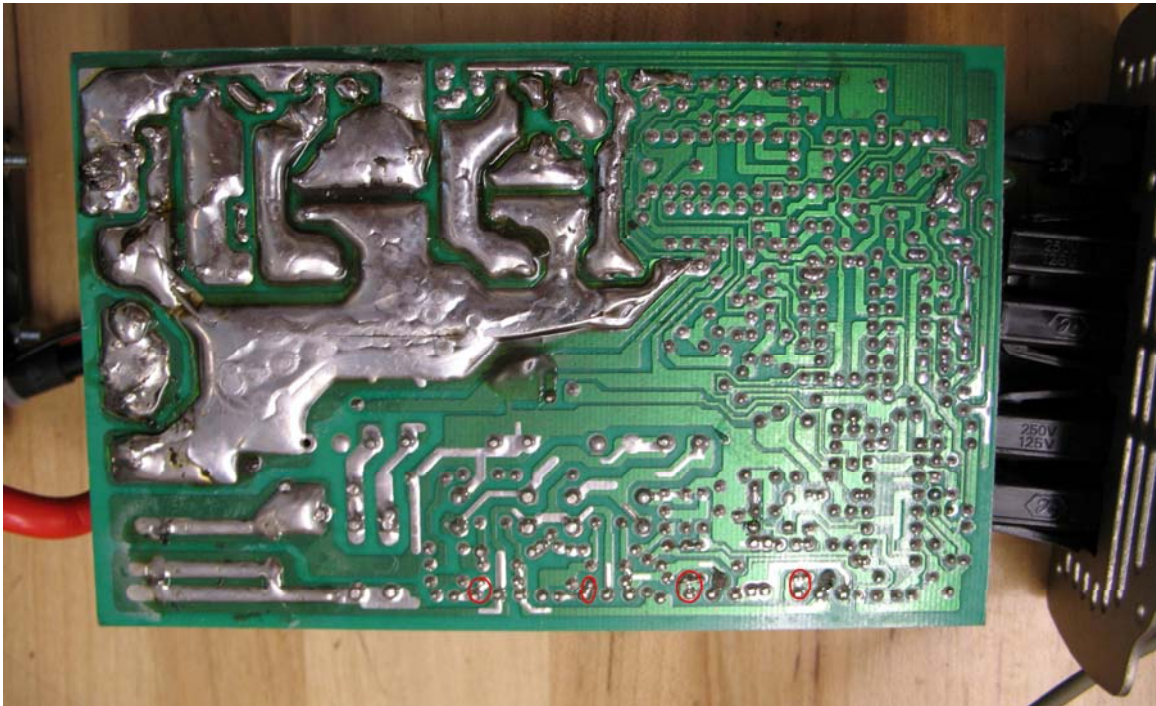


Figure 13: Bottom side of the 700W inverter

Figure 13 shows the top side of the inverter. This top view shows that there are two transformers inside the inverter. Before the inverter was disassembled, it was theorized that there would only be one, since this is a small inverter.

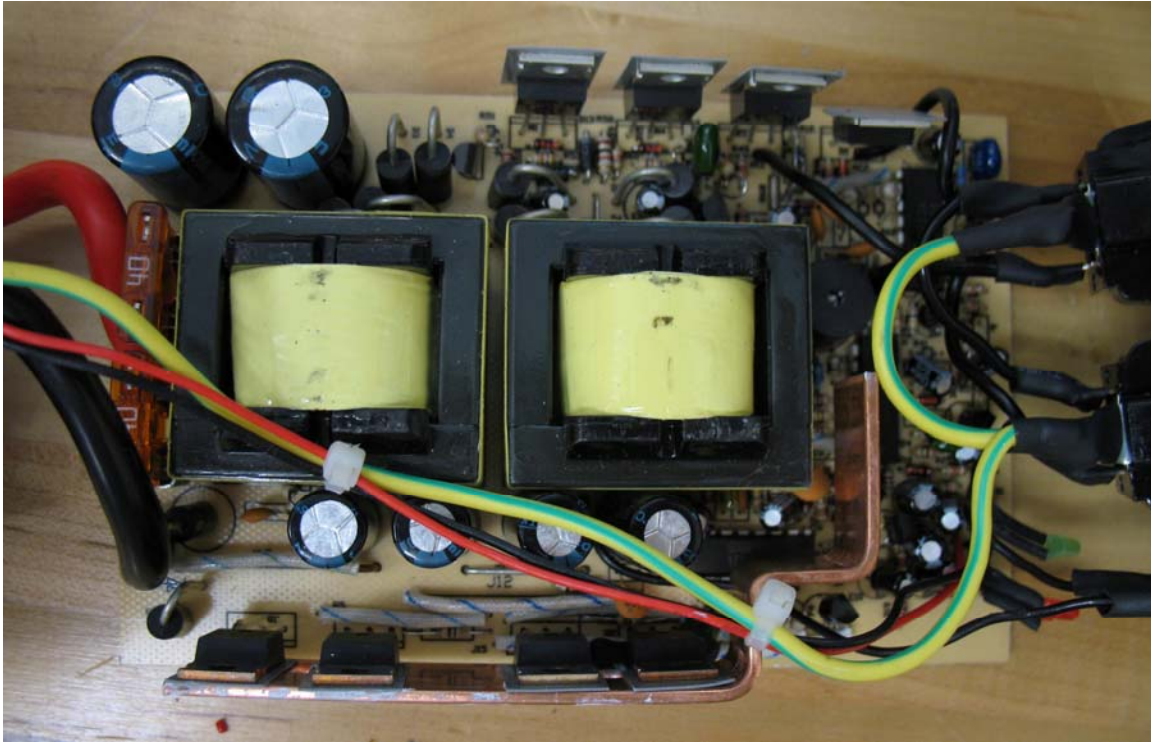


Figure 14: Top side of the 700W inverter

An RMS value of 120V is obtained for each inverter when the output waveform is used in the RMS calculation. It later theorized that paralleling two inverters together in phase would double the RMS voltage to 240V, which is not utilizable in a household receptacle. Connecting each inverter in parallel would add 120V to the system output voltage for each power inverter. For this reason, the inverters were not taken apart and soldered at the gate connections. A solution to this problem would be to put a microcontroller where all the connections were to meet and control the output voltage at a constant 120V while maintaining the current level. A system connecting each inverter in parallel would function correctly and the system power output would increase by utilizing a microcontroller. The theory of connecting the inverters in this manner is physically realized with the Trace inverters. This allows the inverter system to increase the power output, but the cost of these inverters is extremely high.

Conclusion

The research performed in ECE 683 was to test a power inverter and formulate a theory for a modular system. Parallel operation of power inverter is achievable by utilizing the gating signals on the high voltage side. Operation in this manner can be done only when a microcontroller is utilized to correct the output voltage. The microcontroller must be designed for functionality, safety but also cost to enable a modular system to be less expensive than the Trace inverters. Per NEC, the output of each inverter would daisy chain together at a bus bar then feed into the microcontroller control circuitry. Another possibility for modular units would be to place the microcontroller in the emergency panel for a household. The microcontroller would step down incoming power from the modular inverter system before it went to breakers in a household. More testing needs to be conducted before a modular inverter system could be built. We were unable to determine if the voltage output from two inverters in parallel would double or if there would just be a current sharing effect. Theoretically, the voltage output would increase by 120V for each inverter added to the system. By performing a cost analysis versus the daisy chained Trace inverters, it could be determined whether a microcontroller would be a feasible low cost alternative, since it can be seen that household units (computer monitor and vacuum cleaner) can be run off of a square wave inverter. Hopefully, by building a microcontroller and testing out problems encountered while connecting the two in parallel, more headway can be made to see if there is a more cost effective way of implementing a modular system with the less expensive square wave inverters.

Appendix A – PSCAD Data files

```
!=====
! Generated by : PSCAD v4.2.0
!
! Warning: The content of this file is automatically generated.
! Do not modify, as any changes made here will be lost!
!=====
```

```
!-----
! Local Node Voltages
!-----
```

VOLTAGES:

```
1      0.0 // NT_1
2      0.0 // NT_2
3      0.0 // NT_3
4      0.0 // NT_5
5      0.0 // NT_6
6      0.0 // NT_7
```

```
!-----
! Local Branch Data
!-----
```

BRANCHES:

```
0 4 RE 0.0 // 1 GND NT_5
1 3 RS 1000000.0 // 1 NT_1 NT_3
3 0 RS 1000000.0 // 1 NT_3 GND
1 2 RS 1000000.0 // 1 NT_1 NT_2
2 0 RS 1000000.0 // 1 NT_2 GND
5 6 A // 1 NT_6 NT_7
4 1 A // 1 NT_5 NT_1
6 0 RL 20.0 0.015 // 1 NT_7 GND
```

```
!-----
! Local Transformer Data
!-----
```

TRANSFORMERS:

```
! Single Phase Transformer: 0.01 MVA, 0.0144 kV : 0.14 kV
-2 / Number of windings...
3 2 181805.130416 /
5 0 -18699.9562714 1923.42407363 /
```

```
!
DATADSD:
DATADSO:
ENDPAGE
```

Fortran Code

```
=====
! Generated by : PSCAD v4.2.0
!
! Warning: The content of this file is automatically generated.
!         Do not modify, as any changes made here will be lost!
!-----
! Component   : Main
! Description  :
!-----
=====
```

```
      SUBROUTINE DSDyn()
```

```
!-----
! Standard includes
!-----
```

```
      INCLUDE 'nd.h'
      INCLUDE 'emtconst.h'
      INCLUDE 'emtstor.h'
      INCLUDE 's0.h'
      INCLUDE 's1.h'
      INCLUDE 's2.h'
      INCLUDE 's4.h'
      INCLUDE 'branches.h'
      INCLUDE 'pscadv3.h'
      INCLUDE 'fnames.h'
      INCLUDE 'radiolinks.h'
      INCLUDE 'matlab.h'
```

```
!-----
! Function/Subroutine Declarations
!-----
```

```
! SUBR EMTDC_XIGEN ! 'Impulse Generator /w Interpolation'
! SUBR EMTDC_XMSTAB ! 'Monostable Multivibrator /w Interpolation'
! SUBR TSAT21      ! Transformer Saturation Subroutine
! SUBR 1PVSRC      ! Single-Phase Source model
```

```
!-----
! Variable Declarations
!-----
```

```
! Subroutine Parameters
```



```

! Electrical Node Indexes
  INTEGER NT_2, NT_3

! Control Signals
  INTEGER A, IT_1, IT_2
  REAL   Vout, Iac, Idc, RT_1

! Internal Variables
  REAL   RVD2_1(2), RVD2_2(2), X_KNEE
  REAL   TURNS_V, E_MAG, F_RAD

! Indexing variables
  INTEGER ISTOI, ISTOF, IT_0           ! Storage Indexes
  INTEGER IPGB                         ! Control/Monitoring
  INTEGER ISUBS, SS(1), IBRCH(1), INODE ! SS/Node/Branch/Xfmr
  INTEGER IXFMR

!-----
! Record local indexes
!-----

! Dsdyn <-> Dsout transfer index storage
  NTXFR = NTXFR + 1
  TXFR(NTXFR,1) = NSTOL
  TXFR(NTXFR,2) = NSTOI
  TXFR(NTXFR,3) = NSTOF

! Record Offset and Increment Storage Counters
  ISTOI  = NSTOI
  NSTOI  = NSTOI + 3
  ISTOF  = NSTOF
  NSTOF  = NSTOF + 4
  IPGB   = NPGB
  NPGB   = NPGB + 4
  INODE  = NNODE + 2
  NNODE  = NNODE + 8
  IXFMR  = NXFMR
  NXFMR  = NXFMR + 1

! Initialize Subsystem Mapping

  ISUBS = NSUBS + 0
  NSUBS = NSUBS + 1

```

```

DO 100 IT_0 = 1,1
  SS(IT_0) = SUBS(ISUBS + IT_0)
100 CONTINUE

```

! Initialize Branch Mapping.

```

IBRCH(1) = NBRCH(SS(1))
NBRCH(SS(1)) = NBRCH(SS(1)) + 8

```

```

!-----
! Transfers from storage arrays
!-----

```

```

A      = STOI(ISTOI + 1)
Vout   = STOF(ISTOF + 1)
Iac    = STOF(ISTOF + 2)
Idc    = STOF(ISTOF + 3)
IT_1   = STOI(ISTOI + 2)
IT_2   = STOI(ISTOI + 3)
RT_1   = STOF(ISTOF + 4)

```

```

!-----
! Transfer from Imports
!-----

```

```

!-----
! Electrical Node Lookup
!-----

```

```

NT_2 = NODE(INODE + 2)
NT_3 = NODE(INODE + 3)

```

```

!-----
! Read Model data (if any)
!-----

```

```

IF ( TIMEZERO ) THEN
  FILENAME = 'Main.dta'
  CALL EMTDC_OPENFILE
  SECTION = 'DATADSD:'
  CALL EMTDC_GOTOSECTION
ENDIF

```

```

!-----
! Generated code from module definition

```

```

!-----
! 10:[impulse] Impulse Generator /w Interpolation
!
  CALL EMTDC_XIGEN(1,0,0.0,1.0,0.0166666666667,RVD2_1)
  RT_1 = RVD2_1(1)
!

! 20:[monostable] Interpolated Monostable MultiVibrator
!
  RVD2_1(1) = FLOAT(NINT(RT_1))
  RVD2_1(2) = 0.0
  CALL EMTDC_XMSTAB(0,0.008333333,RVD2_1,RVD2_2)
  A = NINT(RVD2_2(1))

! 30:[inv] Interpolated Logic Inverter
  IF (A .NE. 0) THEN
    IT_2 = 0
  ELSE
    IT_2 = 1
  ENDIF

! 70:[peswitch] Power electronic switch
! EMTDC_PESWITCH Power Electronic Switch Model: Transistor
  CALL EMTDC_PESWITCH2(SS(1), (IBRCH(1)+5), 0.01, 1000000.0, A, 0.0&
&, 3, 0, 100000.0, 100000.0, 0.0, 0.0)

! 80:[pgb] Output Channel 'GATE'

  PGB(IPGB+1) = REAL(A)

! 100:[inv] Interpolated Logic Inverter
  IF (A .NE. 0) THEN
    IT_1 = 0
  ELSE
    IT_1 = 1
  ENDIF

! 130:[peswitch] Power electronic switch
! EMTDC_PESWITCH Power Electronic Switch Model: Transistor
  CALL EMTDC_PESWITCH2(SS(1), (IBRCH(1)+3), 0.01, 1000000.0, IT_1, &
&&.0, 3, 0, 100000.0, 100000.0, 0.0, 0.0)

! 140:[peswitch] Power electronic switch

```

```
! EMTDC_PESWITCH Power Electronic Switch Model: Transistor
  CALL EMTDC_PESWITCH2(SS(1), (IBRCH(1)+4), 0.01, 1000000.0, IT_2, &
    &0.0, 3, 0, 100000.0, 100000.0, 0.0, 0.0)
```

```
! 150:[peswitch] Power electronic switch
! EMTDC_PESWITCH Power Electronic Switch Model: Transistor
  CALL EMTDC_PESWITCH2(SS(1), (IBRCH(1)+2), 0.01, 1000000.0, A, 0.0&
    &, 3, 0, 100000.0, 100000.0, 0.0, 0.0)
```

```
! -1:[xfmr-2w] Single Phase 2 Winding Transformer
! TRANSFORMER SATURATION SUBROUTINE
  IF (TIME.GT.0.1) THEN
    X_KNEE = 1.25
  ELSE
    X_KNEE = -1.25
  ENDIF
  TURNS_V = 0.0144
  CALL TSAT21(NT_3,NT_2, 0,0, 0,0, SS(1),0.01,TURNS_V,0.2,X_KNEE,60.&
    &0,1.0,0.004, 0.0, 0)
!
```

```
! -1:[source_1] Single Phase Voltage Source Model 2 'Source1'
! Single Phase Source: Source1 Type: Ideal
! DC source 0.0144 kV, StartUp: 0.05 sec
```

```
  E_MAG = 0.0144
  F_RAD = 0.0
  CALL EMTDC_1PVSRC(SS(1), (IBRCH(1)+1),0.05,0,E_MAG,F_RAD,0.0)
!
```

```
!-----
! Feedbacks and transfers to storage
!-----
```

```
STOI(ISTOI + 1) = A
STOF(ISTOF + 1) = Vout
STOF(ISTOF + 2) = Iac
STOF(ISTOF + 3) = Idc
STOI(ISTOI + 2) = IT_1
STOI(ISTOI + 3) = IT_2
STOF(ISTOF + 4) = RT_1
```

```
!-----
! Transfer to Exports
!-----
```

```

!-----
! Close Model Data read
!-----

      IF ( TIMEZERO ) CALL EMTDC_CLOSEFILE
      RETURN
      END

=====

      SUBROUTINE DSOOut()

!-----
! Standard includes
!-----

      INCLUDE 'nd.h'
      INCLUDE 'emtconst.h'
      INCLUDE 'emtstor.h'
      INCLUDE 's0.h'
      INCLUDE 's1.h'
      INCLUDE 's2.h'
      INCLUDE 's4.h'
      INCLUDE 'branches.h'
      INCLUDE 'pscadv3.h'
      INCLUDE 'fnames.h'
      INCLUDE 'radiolinks.h'
      INCLUDE 'matlab.h'

!-----
! Function/Subroutine Declarations
!-----

      REAL EMTDC_VVDC !
      REAL VBRANCH ! Voltage across the branch

!-----
! Variable Declarations
!-----

! Electrical Node Indexes
      INTEGER NT_7

! Control Signals

```

```
REAL  Vout, Iac, Idc
```

```
! Internal Variables
```

```
! Indexing variables
```

```
  INTEGER ISTOL, ISTOI, ISTOF, IT_0      ! Storage Indexes  
  INTEGER IPGB                          ! Control/Monitoring  
  INTEGER ISUBS, SS(1), IBRCH(1), INODE  ! SS/Node/Branch/Xfmr  
  INTEGER IXFMR
```

```
!-----  
! Record local indexes  
!-----
```

```
! Dsdyn <-> Dsout transfer index storage
```

```
  NTXFR = NTXFR + 1  
  ISTOL = TXFR(NTXFR,1)  
  ISTOI = TXFR(NTXFR,2)  
  ISTOF = TXFR(NTXFR,3)
```

```
! Record Offset and Increment Storage Counters
```

```
  IPGB   = NPGB  
  NPGB   = NPGB + 4  
  INODE  = NNODE + 2  
  NNODE  = NNODE + 8  
  IXFMR  = NXFMR  
  NXFMR  = NXFMR + 1
```

```
! Initialize Subsystem Mapping
```

```
  ISUBS = NSUBS + 0  
  NSUBS = NSUBS + 1
```

```
  DO 100 IT_0 = 1,1  
    SS(IT_0) = SUBS(ISUBS + IT_0)  
  100 CONTINUE
```

```
! Initialize Branch Mapping.
```

```
  IBRCH(1) = NBRCH(SS(1))  
  NBRCH(SS(1)) = NBRCH(SS(1)) + 8
```

```
!-----  
! Transfers from storage arrays  
!-----
```

```
Vout = STOF(ISTOF + 1)
Iac = STOF(ISTOF + 2)
Idc = STOF(ISTOF + 3)
```

```
!-----
! Electrical Node Lookup
!-----
```

```
NT_7 = NODE(INODE + 6)
```

```
!-----
! Read Model data (if any)
!-----
```

```
IF ( TIMEZERO ) THEN
  FILENAME = 'Main.dta'
  CALL EMTDC_OPENFILE
  SECTION = 'DATADSO:'
  CALL EMTDC_GOTOSECTION
ENDIF
```

```
!-----
! Generated code from module definition
!-----
```

```
! 40:[ammeter] Current Meter 'Idc'
  Idc = ( CBR((IBRCH(1)+7), SS(1)))
```

```
! 50:[ammeter] Current Meter 'Iac'
  Iac = ( CBR((IBRCH(1)+6), SS(1)))
```

```
! 60:[voltmeter] Voltmeter (Line - Line) 'Vout'
  Vout = EMTDC_VVDC(SS(1), NT_7, 0)
```

```
! 90:[pgb] Output Channel 'Iac'
```

```
  PGB(IPGB+2) = 1000.0 * Iac
```

```
! 110:[pgb] Output Channel 'Vout'
```

```
  PGB(IPGB+3) = 1000.0 * Vout
```

```
! 120:[pgb] Output Channel 'Idc'
```

PGB(IPGB+4) = 1000.0 * Idc

!-----
! Feedbacks and transfers to storage
!-----

STOF(ISTOF + 1) = Vout
STOF(ISTOF + 2) = Iac
STOF(ISTOF + 3) = Idc

!-----
! Close Model Data read
!-----

IF (TIMEZERO) CALL EMTDC_CLOSEFILE
RETURN
END

Appendix B – Battery Charger Schematics

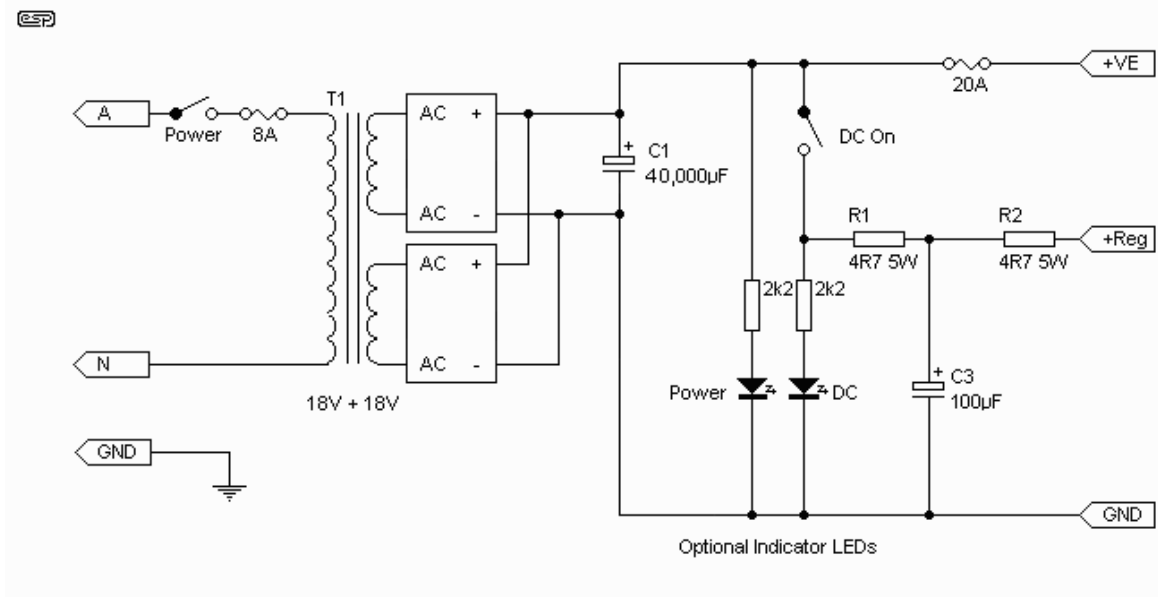


Figure 15: Schematic 1 of 2 (Battery Charger)

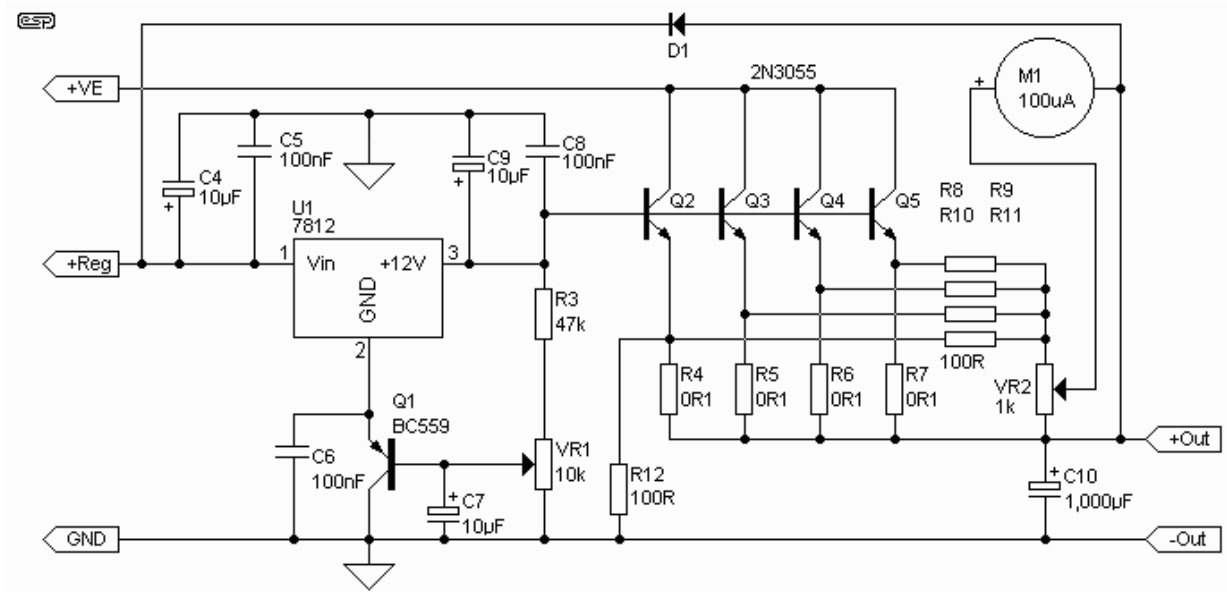


Figure 16: Schematic 2 of 2 (Battery Charger)

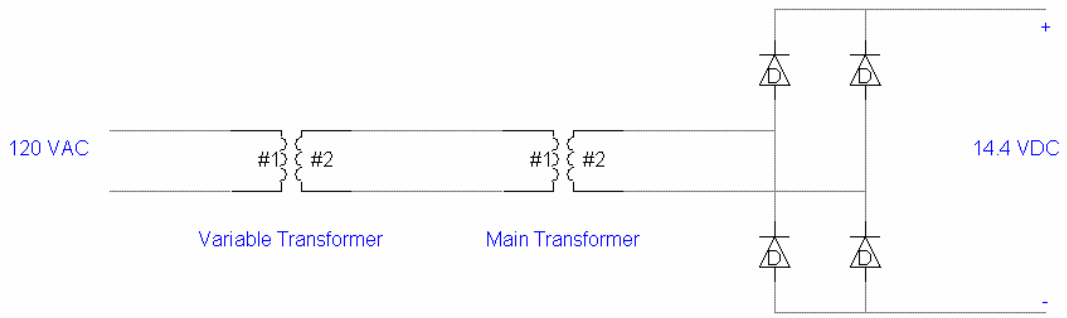


Figure 17: Setup with variable transformer

Appendix C – Group Tasks

Trevor Curry

NEC Code

Inverter research

Lab Testing

Report Compilation

Justin Richendollar

MATLAB Simulation

Inverter research

Lab Testing

Report Compilation

Tom Tweedle

PSCAD Simulation

Inverter research

Battery charger design and construction

Lab Testing

Report Compilation

References

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2. <http://www.sound.westhost.com/project77.htm>
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