Boron Delta-Doping Dependence on Si/SiGe Resonant Interband Tunneling Diodes Grown by Chemical Vapor Deposition

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***Abstract*—Si/SiGe resonant interband tunnel diodes (RITD) were fabricated using CVD on 200-mm silicon wafers. The RITD devices consist of a p^+-i-n^+ structure with δ-doped quantum wells providing resonant interband tunneling through a nominally intrinsic Si/SiGe region. The vapor-phase doping technique was used to obtain abrupt degenerate doping profiles. The boron doping in the δ-doped region was varied, and its effect on peak current density J_p and peak-to-valley current ratio (PVCR) was studied. As the flow rate is reduced, J_p was found to reduce while the PVCR initially increases and then decreases. Device simulations were performed using the ATLAS simulator developed by SILVACO to interpret the results. A maximum PVCR of 2.95 was obtained, and the highest J_p recorded was 600 A/cm^2. This is the highest reported PVCR for any CVD-grown Si/SiGe RITD.**

***Index Terms*—Band-to-band tunneling, chemical vapor deposition (CVD), Delta doping, resonant interband tunnel diodes (RITD), resonant tunneling, Si, SiGe.**

I. Introduction

As CONTINUAL scaling of the current CMOS technology approaches fundamental limitations with device dimensions, it is prudent to consider alternate device and circuit architectures that can extend functional scaling. Quantum-mechanical tunneling-based negative differential resistance (NDR) devices are high-speed devices that can be used to realize logic and memory circuits with fewer device components. Threshold logic gates based on monostable–bistable logic elements, utilizing NDR devices in conjunction with transistors, can be used to realize logic gates for Boolean and multivalue logic [1]. Dense low-power embedded memory is also perceived with a fusion of NDR devices and transistors with significantly lower voltage operation, i.e., below 0.5 V [2], [3]. In addition, the possibility of reconfigurable logic has also been demonstrated [4]. Interest in these devices has also grown recently with the possibility of using tunnel FETs (TFET) as a replacement for MOSFETs to achieve steep subthreshold slopes, and tunnel diodes also serve as a testbed for the optimization of the TFET tunneling injection [5], [6].

A key hurdle in the development of tunneling-based devices has been the development of a manufacturable process that can be easily integrated into a standard CMOS process line. Early development of silicon tunnel diodes relied on alloying pellets of a gold–silicon eutectic containing arsenic onto boron-doped silicon to obtain the sharp highly doped diode junction. A J_p of 1000 A/cm^2 and a peak-to-valley current ratio (PVCR) of 3.9 were reported using alloying with pure Si [7]. However, this technique does not lend itself to very large scale integration with CMOS. The resonant tunneling diode (RTD), which is popularly used with III–V materials, has restricted applicability with a Si/SiGe heterojunction in a silicon-based system due to its disproportionate band offsets. A relaxed-Si/strained-SiGe RTD structure is limited to hole conduction since most of the band offset is primarily in the valence band with only a very small conduction-band offset. This system exhibited a PVCR of 2.2 at 4.2 K, but the NDR region was not observed at room temperature [8]. The heavier holes prevented satisfactory operation. However, an electron RTD was later attained using a strained-Si/relaxed-SiGe system. This required growth of a thick SiGe buffer layer atop the silicon substrate to increase the conduction-band offset up to $\sim$150 meV. A room-temperature PVCR of 1.2 with a J_p of 400 A/cm^2 was observed in this system [9], [10]. More recently, Esaki diodes have been explored again by employing proximity diffusion technique [11], and a PVCR of 2.1 with a J_p of 88 A/cm^2 was reported. A $Si_{0.74}Ge_{0.26}$ 6-nm tunneling barrier was later incorporated resulting in an increased J_p of 180 A/cm^2 with a PVCR of 2.6 [12]. Jorke *et al.* [13] first observed NDR behavior in p^+-i-n^+ structures with narrow intrinsic regions (5, 10 nm) with a maximum PVCR of 2. Improvements in epitaxial growth to obtain sharp doping profile with reduced defect density resulted in p^+-i-n^+ Esaki diodes with PVCR up to 5.05 and J_p of 4 A/cm^2 [14]. A hybrid Esaki–RTD structure that can be used to achieve high current densities with a modest PVCR in the Si/SiGe system is a resonant interband tunnel diode (RITD). Here, δ-doping is used to obtain high abrupt doping and create electron and hole quantum wells to increase the tunneling probability. Low-temperature (LT)-molecular beam

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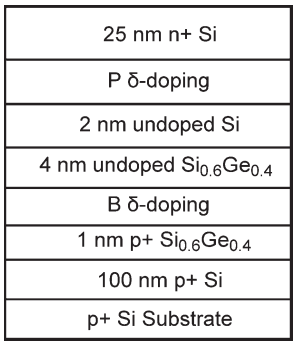

Fig. 1. Schematic diagram of the CVD-grown Si/SiGe RITD structure with a 4-nm $Si_{0.6}Ge_{0.4}$/2-nm Si tunneling barrier.

epitaxy (MBE) at 370 °C was originally used to create p^+-i-n^+ structures incorporating δ-doping with a Si/$Si_{0.5}Ge_{0.5}$/Si 1/4/1-nm barrier to attain current densities of 3.2 kA/cm^2 and a PVCR of 1.54. [15]. A postgrowth rapid thermal anneal process was found essential to reduce the point defect density introduced by the low growth temperature. The addition of SiGe within the tunneling barrier increases the tunneling probability due to the reduced band gap. However, SiGe is limited by its critical thickness, and a composite SiGe/Si tunneling barrier has to be employed. The highest reported PVCR obtained for Si/SiGe RITDs is 6 with a current density of 1.5 kA/cm^2 using a 3-nm $Si_{0.54}Ge_{0.46}$/1-nm Si barrier [16]. A pure Si RITD, avoiding the complexity of Ge incorporation, resulted in a PVCR of 2.05 [17]. More recently, a Si-only RITD with a PVCR of 2.48 and J_p of 1.5 kA/cm^2, without requiring postgrowth anneal, has been reported [18]. Current densities can be tuned with the RITD for specific applications by varying the tunneling barrier thickness, resulting in seven orders of magnitude variation of current densities from 218 to 20 mA/cm^2 for barrier thicknesses ranging from 2.5 to 16 nm [19], [20]. However, translation into a standard CMOS process line requires a higher throughput growth method, such as CVD, and the CVD technique is already incorporated into existing CMOS production lines. Recently, the first Si/SiGe-based RITD grown by CVD has been demonstrated using 200-mm wafers [21].

In this paper, further optimization in CVD growth parameters was used to obtain peak current densities up to 600 A/cm^2 and a PVCR up to 2.95. This is the highest room-temperature PVCR reported for a CVD-grown Si-based interband tunnel diode. Across-the-wafer variation in the tunneling current and PVCR was also presented for the first time.

II. Experimental Setup

Fig. 1 shows the nominal device structure layering of the RITD studied here. The epitaxial growth of the RITDs was accomplished using a standard horizontal cold wall load-locked ASM Epsilon 2000 reactor with variable pressure ranging from atmospheric pressure (AP) to reduced pressure (RP). The p and n δ-doping layers create confined quantum wells with the Si/SiGe i-layer acting as a tunneling spacer layer. Utilizing SiGe in the tunneling barrier, which has a lower band gap, increases the tunneling probability and elevates the peak current. However, its thickness is limited by the critical thickness; hence, a composite Si/SiGe tunneling spacer is employed. The use of quantum wells as the source of electrons and holes results in higher density-of-states at the tunneling energy for the system going from 3-D to 2-D and, hence, higher peak currents [22]. SiGe adjacent to the boron δ-doping also acts as a diffusion barrier suppressing outdiffusion of the δ-doping [23]. The structures were grown on a 200-mm-diameter boron-doped Si substrate. Growth was initiated with a 100-nm p^+ Si buffer layer deposited at 650 °C under RP using silane (SiH_4) and intentionally doped at a nominal level of 5×10^{19} cm^{-3} using diborane (B_2H_6). The substrate temperature was then reduced to 575 °C, and a 1-nm $Si_{0.6}Ge_{0.4}$ boron diffusion barrier layer has been grown next, followed by a sheet of boron (at least 5×10^{13} cm^{-2}) at AP. A nominally undoped composite tunneling spacer comprising of 4-nm $Si_{0.6}Ge_{0.4}$ and 2 nm of Si is deposited next at RP using silane (SiH_4) and germane (GeH_4). Finally, a phosphorus spike (at least 5×10^{13} cm^{-2}) is grown at 600 °C, and an n^+ cap layer is deposited at 675 °C using dichlorosilane. Vapor-phase doping technique is utilized to achieve the p and n δ-doping spike, wherein the dopant atoms are deposited on the wafer by thermal decomposition of diborane (B_2H_6) and phosphine (PH_3), respectively [24], [25]. A set of four wafers were grown with the boron flow varied over a factor of 6 to modify the boron content in the bottom δ-doped layer.

The device fabrication process is as follows, closely following previous reports [21]. A first photolithography step defines a series of dots with diameters of 10, 18, 50, and 75 μm, forming the cathode contact. This is followed by deposition and liftoff of Ti/Au (15/100 nm). Mesa isolation is performed by self-aligned wet etching in an $HF/HNO_3/H_2O$ (2 : 100 : 100) solution. Finally, a second lithography step defines the anode, and Pt/Au (15/100 nm) is electron-beam-evaporated to form the anode ohmic contact.

III. Results and Discussion

Fig. 2 shows the atomic doping profile obtained by secondary ion mass spectroscopy (SIMS) analysis of the four epitaxial wafers, measuring all dopants regardless of their electrical activation. An oxygen beam was used for measuring boron concentrations, whereas cesium beam was used for the phosphorus concentration. An impact energy of 250 eV was selected for both the beams to reduce knock-on effects. The boron concentration was calculated in a $Si_{0.7}Ge_{0.3}$ matrix, whereas phosphorus was calculated assuming a silicon matrix. It is observed that the boron peak doping reduces as the boron flow rate is reduced with peak values of 5.9×10^{21}, 2.9×10^{21}, 1.1×10^{21}, and 4.4×10^{20} cm^{-3} for flow rates of 6× (sample A), 4× (sample B), 2× (sample C), and baseline flow (sample D), respectively. For comparison, the solubility limit of B and P in bulk Si is 2.5×10^{20} and 1×10^{20} cm^{-3}, respectively. The phosphorous concentration remained unchanged over the four samples studies here. Fig. 2(e) shows the boron SIMS profile for the four samples overlaid on top of each other for comparison.

Room-temperature I–V characteristics measured at different locations for the as-grown samples are presented in Fig. 3. Postgrowth annealing was determined to be unnecessary for CVD-grown RITDs, unlike their MBE grown counterparts,

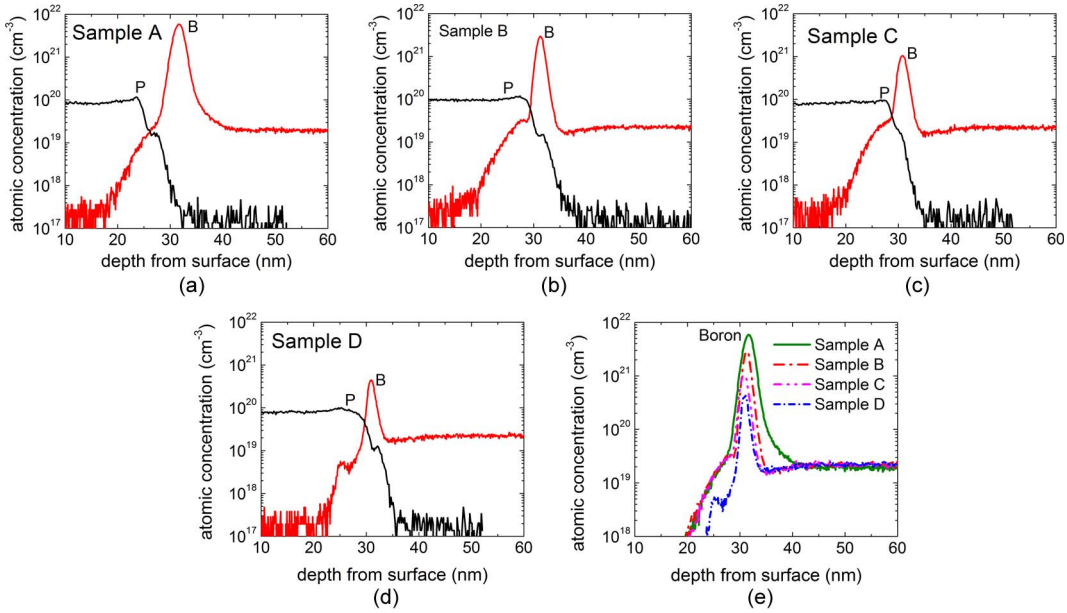

Fig. 2. SIMS profile for samples A–D with boron flow of (a) 6× baseline, (b) 4× baseline, (c) 2× baseline, and (d) baseline flow. (e) Comparison of boron SIMS profile for the four samples.

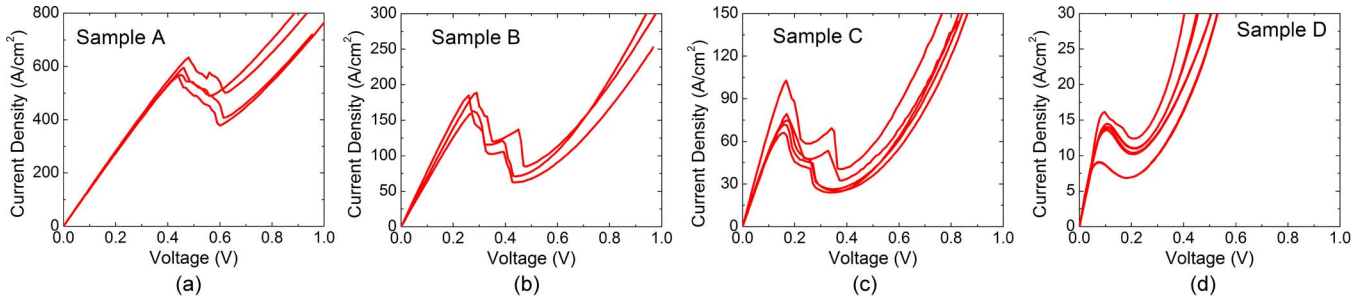

Fig. 3. Measured I–V characteristics for samples A–D. The average peak current and the PVCR are: (a) 500 A/cm^2, and 1.38; (b) 175 A/cm^2 and 2.24; (c) 70 A/cm^2 and 2.7; and (d) 15 A/cm^2 and 1.3, respectively. The maximum PVCR of 2.95 is obtained for sample C. The multiple lines in each graph correspond to measurements from various representative diodes in each sample. All measurements presented were performed on 18-μm mesa diameter diodes.

due to the higher growth temperatures employed resulting in fewer vacancy defects [21]. It is recognized that some reports of MBE-grown RITDs without postgrowth annealing have been disclosed [14], [18], but annealing always improves an MBE grown diode, regardless of its as-grown performance. All measurements presented have been performed on 18-μm dots and were performed on pieces from the center of the 200-mm wafers. The peak current density reduces with a reduction of boron doping (samples A to D) with an average current density of 500, 175, 70, and 15 A/cm^2, respectively. The PVCR increases from an average value of 1.38 for sample A to 2.24 and 2.7 for samples B and C, respectively. However, the PVCR falls back to 1.3 as the boron doping is further reduced for sample D. The highest PVCR of 2.95 is observed for sample C. In comparison, equivalent RITD structures grown by LT-MBE have exhibited a J_p of 1.9 kA/cm^2 with PVCR of 3.8 [20].

In order to interpret the results, device simulations of the CVD stack were performed using the ATLAS device simulator (version 5.16.3.R) developed by SILVACO. The device structure modeled is shown in Fig. 4(a). From the measured SIMS data (see Fig. 2), it is apparent that the doping concentration in the δ-doping region is much greater than the solid solubility limit for B in bulk $Si_{0.6}Ge_{0.4}$, assuming all electrically active species, which is 2.5×10^{20} cm^{-3}. Hence, the maximum active B doping level is assumed to be capped at 2.5×10^{20} cm^{-3} for all the samples in the simulations. Please note that there have been recent reports of enhanced boron solubility in compressive biaxially strained silicon [26]. In this structure, the boron δ-doping lies within a thin compressively strained SiGe. However, it is unclear if a similar effect manifests here. In fact, it is known that high boron doping can result in strain compensation in SiGe alloys allowing for larger critical thicknesses for a given Ge concentration [27], [28]. The δ-doping plane is modeled as a 1-nm nominal waist thickness and a Gaussian profile. With the peak doping level fixed, the width of the Gaussian is then tuned in ATLAS to match the measured peak current data obtained experimentally. The corresponding slopes of the resulting Gaussians obtained for samples A to D are 1.4, 1.05, 0.85, and 0.3 nm/dec, respectively [see Fig. 4(b)]. The corresponding values obtained from the SIMS profile are 1.9, 1.2, 1.2, and 0.6 nm/dec, respectively. It is reasonable to expect that the measured SIMS profile will be broader than

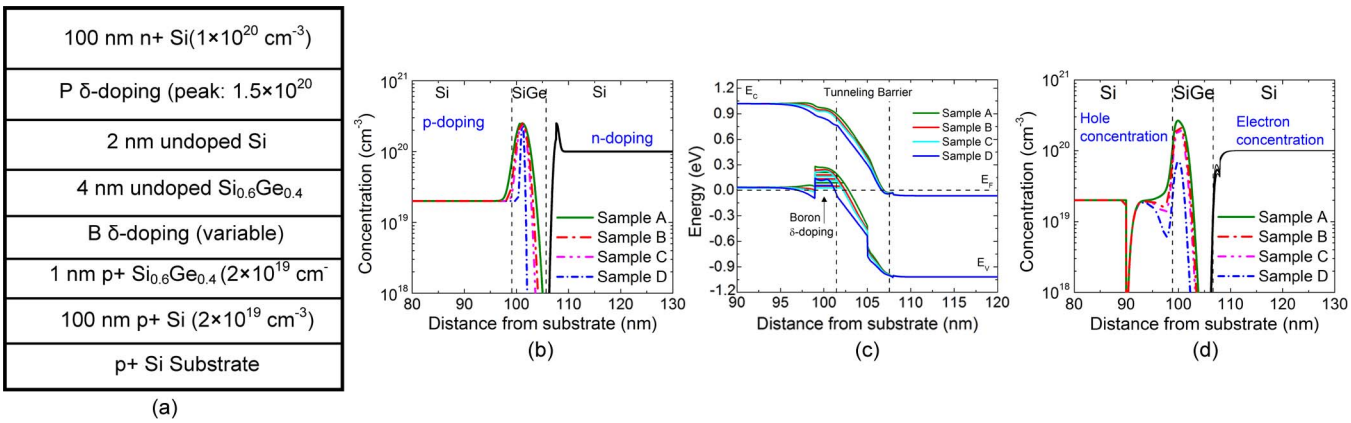

Fig. 4. (a) Device structure, (b) boron and phosphorus doping, (c) band diagram, and (d) net electron and hole concentration obtained from device simulation of the Si/SiGe RITD structure using the ATLAS device simulator.

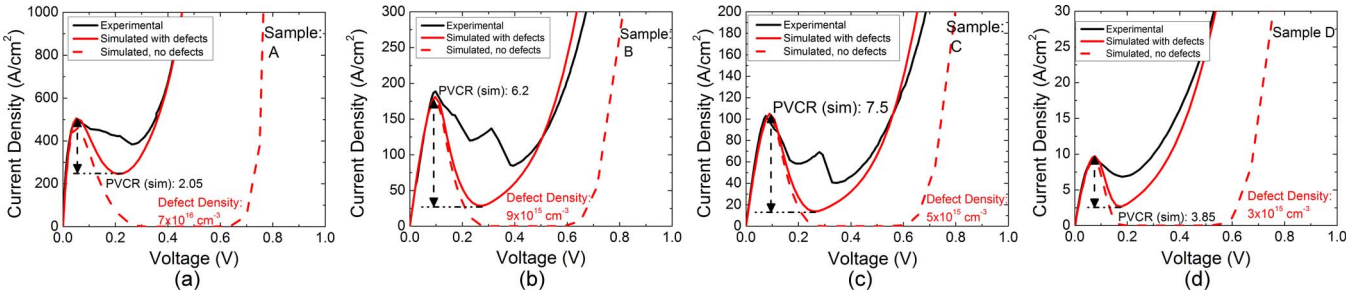

Fig. 5. (a) Representative measured I–V for samples A–D along with simulated I–V with and without inclusion of trap-assisted tunneling showing reduction in peak current and defect density as the boron δ-doping is reduced. The resultant simulated PVCR initially increases and then decreases with values of (a) 2.05, (b) 6.2, (c) 7.5, and (d) 3.85.

the actual dopant distribution due to knock-on effects and increasing surface roughness during depth profiling. However, there are several approximations in the tunneling model, i.e., the effective mass of electrons and holes used and inaccuracies in the doping density between the experimental and simulated devices. Hence, the Gaussian slope fit obtained from simulation cannot be assumed to be accurate quantitatively. It should be noted that the simulated dopant distribution models the electrically active dopants alone while the SIMS data measures both substitutional and interstitial dopant density, regardless of electrical activation.

The band diagrams at equilibrium are obtained by self-consistent solutions of Poisson and Schrödinger equations and are illustrated in Fig. 4(c). The large level of boron δ-doping results in quantum confinement, whereas no such confinement is expected for the phosphorus δ-doping plane obtained here due to its reduced doping levels (see Fig. 2). Strain in the $Si_{0.6}Ge_{0.4}$ layer results in splitting of the heavy and light hole bands. Three energy levels corresponding to two heavy hole bands and one light hole band are obtained for samples A and B. The electron and hole concentrations are determined using Fermi statistics, wave functions, and eigenenergy values [see Fig. 4(d)].

Fig. 5 shows simulated I–V characteristics obtained using SILVACO for each sample along with a corresponding representative experimental I–V curve overlaid for comparison. The experimental I–V has been corrected for series resistance, which includes ohmic contacts, bulk injector resistance, and conductance through the substrate. Tunneling current is modeled by SILVACO using a nonlocal band-to-band tunneling model with a Wentzel–Kramers–Brillouin (WKB) approximation. However, it does not account fully for indirect band-gap tunneling in Si and Ge, where phonon-assisted tunneling needs to be considered. The tunneling probability is calculated using a two-band approximation for the evanescent wave vector. The dotted lines in Fig. 5 are the resultant of currents due to tunneling and thermal diffusion components combined. However, normally, a third current component, which is called excess current, due to tunneling through defect states within the forbidden gap of the tunneling barrier, is present [29]. In order to model the defect-related current appropriately, trap levels were introduced into the band gap of the SiGe region with ATLAS modeling. Trap-assisted tunneling is modeled by including field enhancement factors in the Shockley–Read–Hall equation, which is hence incorporated into the recombination term for the carrier continuity equation. The recombination term for donor-like (R_D) and acceptor-like (R_A) traps is given as shown at the bottom of the next page, where

$\tau_{n,p}$ = electron/hole lifetime;
$\tau_{n,p}$ = $(1/\sigma_{n,p} \cdot \vartheta_{n,p} \cdot N_T)$;
$\sigma_{n,p}$ = electron/hole capture cross section;
$\vartheta_{n,p}$ = thermal velocity calculated using electron/hole effective mass;
N_T = trap density;
g = degeneracy factor (set to 2 for the simulations);
$\Gamma_{n,p}$ = Field enhancement factor for electrons/holes;

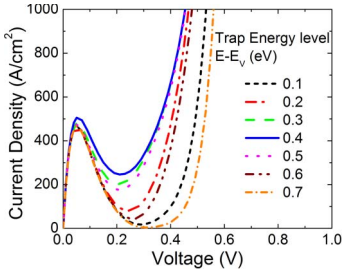

Fig. 6. Variation in valley current with location of traps within the SiGe band gap, illustrating that midgap traps result in maximum valley current. simulator.

Γ_n $= (\Delta E_n/kT_L)\int_0^1 \exp((\Delta E_n/kT_L)u - K_n u^{3/2})du$;
Γ_p $= (\Delta E_p/kT_L)\int_0^1 \exp((\Delta E_p/kT_L)u - K_p u^{3/2})du$;
$\Delta E_{n,p}$ = energy range for which tunneling can occur for electrons/holes.

$$K_{n,p} = \frac{4}{3}\frac{\sqrt{2m_0 m_{\text{tunnel}}\Delta E_{n,p}^3}}{3q\hbar|E|}. \tag{3}$$

The capture cross section is assumed to be 10^{-13} cm^2 here. The trap density is then varied to fit the valley current obtained experimentally. However, it should be clarified that the capture cross section and trap density cannot be determined independently, and an assumption has to be made for one in order to determine the other. As long as the electron/hole lifetime, which depends on the product of the capture cross section and the trap density, is constant, the valley current obtained from modeling is the same. For example, for sample A, $\sigma_{n,p}$ of 10^{-14} cm^2 and N_T of 7×10^{17} cm^{-3} result in the same valley current, as determined alternatively with $\sigma_{n,p}$ of 10^{-13} cm^2 and N_T of 7×10^{16} cm^{-3}. It should be noted that resonances in the measured NDR region may mask the true PVCR [30]. Modeling suggests that the PVCR of 2.05, 6.2, 7.5, 3.85, for samples A–D, are obtainable, respectively.

The effect of trap energy level position on the valley current is shown in Fig. 6. Doping levels commensurate to sample A are used for this study. The trap density is fixed to 7×10^{16} cm^{-3}. The trap level is then varied throughout the band gap and the I–V characteristics plotted in each case. Defects close to the conduction band have the minimum effect on valley current while midgap acceptor/donor traps exhibit maximum influence on valley current.

It is evident that as the boron δ-doping is increased, the total trap density required to obtain a reasonable valley current fit to the experimental data also increases. The total trap densities used in the modeling are 7×10^{16}, 9×10^{15}, 5×10^{15}, and 3×10^{15} cm^{-3} for samples A to D, respectively. This trend indicates boron interstitials in the SiGe region contributing

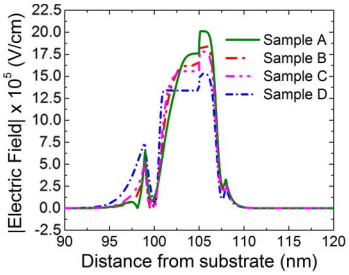

Fig. 7. Variation of the electric field within the tunneling barrier region for samples A–D. The electric field increases while the effective tunneling distance reduces due to the broadened boron δ-doping profile as boron doping is increased.

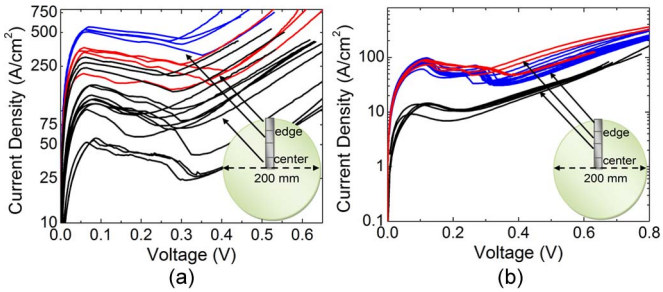

Fig. 8. Across the wafer variation of the PVCR from the center to the edge of the 200-mm wafer for (a) Sample C and (b) Sample D.

largely to the trap-assisted tunneling. Boron interstitials, being highly reactive, tend to form complexes with other impurities in silicon, such as oxygen and carbon [31]. Higher doping can also lead to formation of boron clusters and precipitation [32]. The determination of the exact nature of the defect formed will require detailed deep-level transient spectroscopy (DLTS) studies.

The increase in peak current with boron δ-doping can be explained by the enhanced boron diffusion with boron concentrations and interstitial boron formation [33]. From the electric field plot (see Fig. 7), it is evident that as the Gaussian profile for the δ-doping becomes broader, the electric field in the intrinsic region increases, and the net tunneling barrier width reduces, both leading to an increase in the tunneling current.

Thus, the boron δ-doping parameter needs to be carefully optimized to achieve high doping while keeping the defect formation to a minimum in order to obtain high peak currents concurrently with a high PVCR.

For completeness, the device performance variation across the 200-mm wafer from center to edge was also measured for samples C and D. The results (with series resistance correction) are shown in Fig. 8. The peak current shows an order of magnitude difference across the wafer. It should be pointed out

$$R_D = \frac{pn - n_{ie}^2}{\frac{\tau_n}{1+\Gamma_n}\left[p + gn_{ie}\exp\left(\frac{E_i - E_T}{kT_L}\right)\right] + \frac{\tau_p}{1+\Gamma_p}\left[n + \frac{1}{g}n_{ie}\exp\left(\frac{E_T - E_i}{kT_L}\right)\right]} \tag{1}$$

$$R_A = \frac{pn - n_{ie}^2}{\frac{\tau_n}{1+\Gamma_n}\left[p + \frac{1}{g}n_{ie}\exp\left(\frac{E_i - E_T}{kT_L}\right)\right] + \frac{\tau_p}{1+\Gamma_p}\left[n + gn_{ie}\exp\left(\frac{E_T - E_i}{kT_L}\right)\right]} \tag{2}$$

that no process optimization to improve the uniformity across the wafer has been incorporated to this process yet. However, this is a critical issue for manufacturability of tunnel diodes and will be examined in future studies.

IV. Conclusion

Si-based RITDs with an Si/SiGe composite spacer thickness of 6 nm were fabricated using CVD. The boron δ-doping flow was varied to obtain different δ-doping concentrations. A significant improvement in PVCR, i.e., 2.95, from previously reported values of 1.85 was obtained while the peak current densities averaged about 100 A/cm^2 for both diodes. Increasing the boron flow rate during δ-doping results in higher doping and increased current densities but at the cost of reduced PVCR. Device modeling indicates that the increased current density is due to higher electric fields in the spacer region as more boron is incorporated, along with reduced tunneling distance due to broadening of the δ-doped Gaussian profile. However, doping above the solid solubility limit results in increased boron interstitial defects, causing a larger increase in valley current. Thus, a net reduction in the PVCR with increased boron δ-doping is observed. The higher growth temperature required for CVD presents additional challenges in optimization to obtain sharp high-concentration δ-doping profiles.

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