Strain-Engineered Si/SiGe Resonant Interband Tunneling Diodes Grown on $Si_{0.8}Ge_{0.2}$ Virtual Substrates With Strained Si Cladding Layers

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***Abstract*—Strain-engineered Si-based resonant interband tunneling diodes grown on commercially available $Si_{0.8}Ge_{0.2}$ virtual substrates were developed that address issues of P dopant diffusion and electron confinement. Strain-induced band offsets were effectively utilized to improve tunnel diode performance versus the control device, particularly the peak-to-valley current ratio (PVCR). By growing tensilely strained Si layers cladding the P δ-doping plane, the quantum well formed by the P δ-doping plane is deepened, which concurrently increases the optimal annealing temperature from 800 °C to 835 °C and facilitates an increase in the PVCR up to 1.8× from 1.6 to 2.8 at room temperature, which is significantly better than previous results on strained substrates.**

***Index Terms*—Negative differential resistance, resonant interband tunneling diodes (RITDs), semiconductor epitaxial layers, silicon alloys, silicon germanium, strained layers, tunnel diodes.**

I. Introduction

SINCE Si-based resonant interband tunneling diodes (RITDs) grown by low-temperature molecular beam epitaxy (LT-MBE) were first demonstrated by Rommel *et al.* [1], numerous studies have been carried out to improve their dc/radio-frequency performance [2]–[7], as well as monolithic integration of RITDs with heterojunction bipolar transistors (HBTs) [8] and CMOS [9]. The RITD design and process of Rommel *et al.* combined several key points: 1) p and n δ-doped injectors to create defined quantum wells (QWs) and satisfy the degeneracy doping condition; 2) a composite i-layer inserted as a spacer layer between the δ-doped injectors to minimize dopant interdiffusion that leads to widening of the spacer and a larger tunneling distance; 3) LT-MBE to suppress segregation and diffusion; and 4) a short postgrowth rapid thermal anneal heat treatment to reduce point defects created during the LT-MBE process [10], [11] that lead to an elevated excess current via defect-related tunneling.

Recently, an interband tunnel diode (ITD) grown on a virtual $Si_{0.7}Ge_{0.3}$ substrate for the first time has been reported by Stöffel *et al.*, but it did not include some enhancements permitted, exploiting the opportunities created with a virtual substrate system [12]. The design of Stöffel *et al.* explored the potential ITD compatibility and integration with pseudomorphic modulation-doped field-effect transistors (MODFETs). Their report indicated a room-temperature peak-to-valley current ratio (PVCR) of 1.36, but did not comment on the advantages of modifying the Ge content.

One advantage offered by SiGe virtual substrates is that a higher overall Ge content can be inserted in the spacer region to increase the tunneling probability, hence raising the resistive cutoff frequency, without exceeding the critical thickness [6]. This is partially promoted by barrier lowering and greater momentum mixing induced with the added Ge content due to the decreasing energy difference between the L and Γ valleys with the increasing Ge content. Thus, enabling band-to-band tunneling is enabled sometimes without participation of a phonon. Furthermore, as the Ge content increases, the light-hole effective mass, which is involved in the interband tunneling, is greatly reduced with the increasing Ge content, which also improves the tunneling probability.

However, a second advantage created by SiGe virtual substrates is that the band offsets change in the Si/SiGe system, as reported in [13] and [14]. This property leads to tremendous flexibility in the Si-based device design and has given rise to a number of novel devices, such as MODFETs [15], [16] and resonant tunneling diodes [17]. In this letter, we report on strain-engineered Si-based RITDs grown on commercially available virtual $Si_{0.8}Ge_{0.2}$ substrates to improve the P δ-doping region of the RITD device. Previous reports of Si-based RITD improvements on Si substrates have primarily addressed the B-doped side [4]. In this letter, thin tensilely strained Si layers were inserted cladding the P δ-doping spike to modify the corresponding band diagram and act as a P diffusion inhibitor. The electrical results show the great flexibility gained in strain engineering the RITD band structure, as well as the promise of

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performance improvement of Si-based RITDs on SiGe virtual substrates.

II. Experimental

Commercial p-type $Si_{0.8}Ge_{0.2}$ virtual substrates were used here that used epitaxially deposited SiGe on a Si substrate (boron doped, 0.01–0.015 $\Omega \cdot$ cm) by the chemical vapor deposition technique. The SiGe relaxation is greater than 98%. The total threading dislocation is specified to be less than 2×10^6 cm^{-2}. The relaxed SiGe structure, as received, was capped with a thin 17.5-nm-thick Si cap layer to facilitate subsequent Si processing. The surface was characterized using atomic force microscopy. Typical values of the root-mean-square roughness $Z_{\rm rms}$ were 1.2 and 2.7 nm, which were measured over 10- and 50-μm squares. Typical values of the maximum height variation $Z_{\rm max}$ were 6 and 12 nm, which were measured over 10- and 50-μm squares.

The RITD structures were grown on these p-type $Si_{0.8}Ge_{0.2}$ virtual substrates with a molecular beam epitaxial (MBE) growth system using elemental Si and Ge in electron beam sources. Prior to growth, the wafers were cleaned with organic solvents, followed with a 10-min piranha etch ($9:2$ H_2SO_4/H_2O_2) to remove any residual organic impurities, followed by a modified RCA clean with a dilute HF last final step. The epitaxial growth was initiated at 650 °C, which is a temperature sufficiently high for the removal of the surface hydrogen. The Si and Ge growth rates were independently determined by the mass increase on test samples, which, in turn, were used to calibrate the photosensitivity of a Temescal Sentinel III growth-rate controller. The total growth rate (Si and Ge combined) was maintained at 0.1 nm/s throughout the growth. The doping levels for both n^+ and p^+ layers are 5×10^{19} cm^{-3}, whereas both the B and P δ-doping sheet carrier concentrations were maintained at 1×10^{14} cm^{-2}. The doping concentrations were calibrated on test samples using secondary ion mass spectrometry and Hall electrical measurements. The δ-doping was performed by stopping the Si and Ge deposition and only depositing the dopant. The sheet concentration of the δ-doped layers, i.e., 1×10^{14} cm^{-2}, corresponds to 16% of a monolayer. After the initiation of growth at 650 °C, the p^+ substrate contact layer was grown at 500 °C. The substrate temperature was further lowered to 320 °C during the deposition of the B δ-doped layer. This temperature was maintained throughout the remainder of the growth. Low-temperature epitaxial growth limits the adatom mobility; so the doped layers follow the surface contour of the virtual substrates. Further details of the growth process have been reported elsewhere [1], [2], [4], [7].

To study the effect of tensilely strained Si layers, two epilayer structures were designed, which are more completely discussed in the next section. Prior to device fabrication, portions of the MBE-grown wafers were annealed using a forming gas ambient (N_2/H_2) in a Modular Process Technology Corporation RTP-600S furnace at various temperatures for 1 min. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO_3 wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.

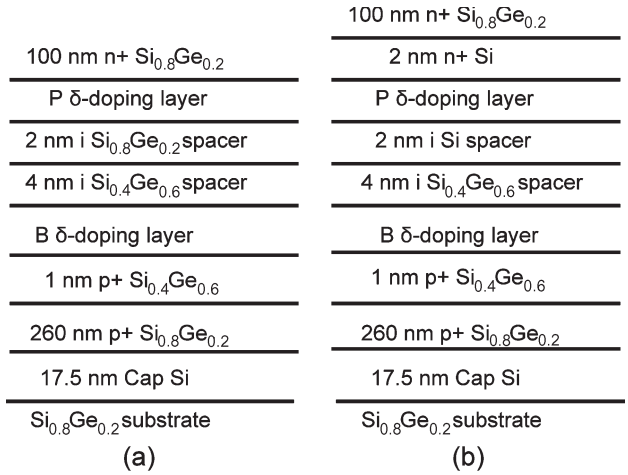

Fig. 1. Schematic of RITDs grown on $Si_{0.8}Ge_{0.2}$ substrates. (a) Structure A, the control RITD with an additional 20% Ge added to each layer. (b) Structure B, an RITD with P cladding layers using thin tensilely strained Si layers.

III. Results and Discussions

Fig. 1(a) presents the control structure (Structure A), which is similar to previous RITDs optimized on Si substrates for large PVCRs [4], except here the Ge concentration of each layer was raised by 20% to match the elevated Ge content in the virtual SiGe substrate, similar to the design of Stöffel *et al.* [12]. A larger Ge content in the spacer should reduce the tunneling barrier height, promote momentum mixing, and result in a higher PVCR, which are predicted advantages for using a SiGe substrate. Another advantage, which is investigated here through Structure B, is the inclusion of thin tensilely strained Si layers cladding the P δ-doping layer that effectively deepens the conduction band QW by creating band offsets in the conduction band. Fig. 1(b) shows the designed structure with the P δ-plane clad by two 2-nm Si layers. Fig. 2 shows the resulting band diagrams for both structures calculated using a 1-D Poisson–Schrödinger solver that self-consistently obtains a 1-D solution to the Poisson–Schrödinger equations with a finite-difference method and a nonuniform mesh size [18], [19]. Compared to the control sample, there exists a conduction band offset of 0.2 eV and a valence band offset of 0.05 eV in Structure B induced by the tensile strain in the Si layer.

Data were collected from devices of diameters 10, 18, 50, and 75 μm. No noticeable dependence of the current density and PVCR on the device size was observed. Fig. 3 shows the PVCR of each 18-μm-diameter structure annealed at various temperatures for 1 min. The highest PVCR obtained from the control RITD on $Si_{0.8}Ge_{0.2}$ is only 1.6, which is only slightly above the PVCR (1.36) of the previously reported ITD by Stöffel *et al.* grown on a virtual $Si_{0.7}Ge_{0.3}$ substrate and using a constant Ge% throughout the epilayers [12]. It is noteworthy that the PVCR obtained from the ITD grown on the virtual $Si_{0.7}Ge_{0.3}$ substrate by Stöffel *et al.* is also much lower than

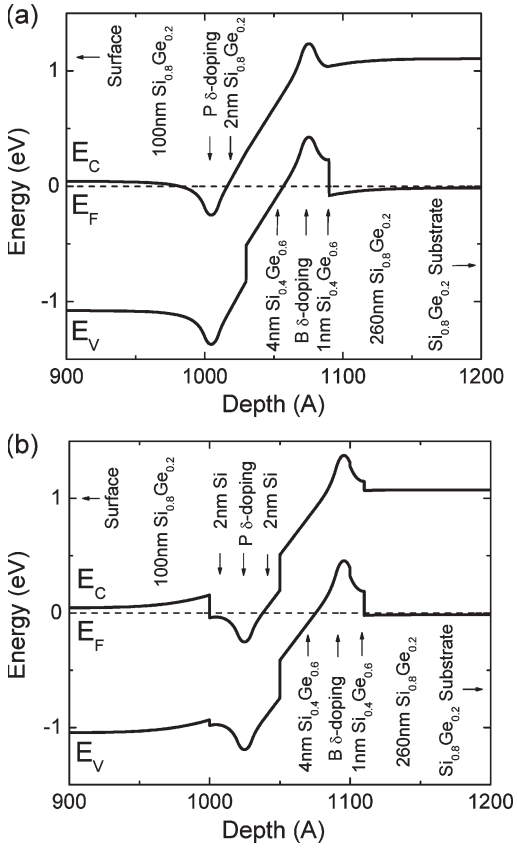

Fig. 2. Calculated band diagrams of (a) Structure A and (b) Structure B using a 1-D Poisson–Schrödinger solver.

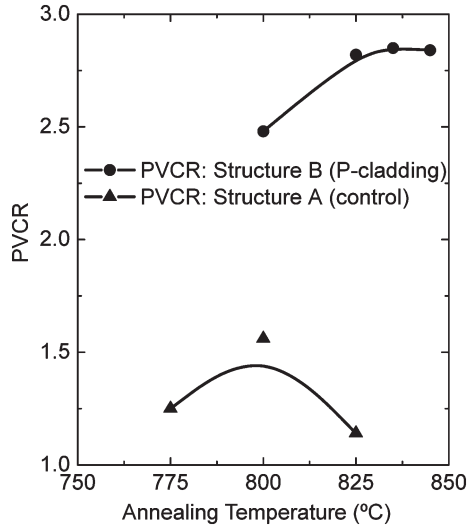

Fig. 3. Comparison of PVCR performance of RITDs with and without thin tensilely strained Si layers inserted cladding the P δ-doping spike.

their previous reports of ITDs directly grown on a Si substrate. Stöffel *et al.* attribute the discrepancy to the surface roughness of the virtual $Si_{0.7}Ge_{0.3}$ substrate [12] and may be systemic to the early-generation SiGe virtual substrates purchased for this letter too. However, it is clear that the insertion of Si cladding layers in Sample B substantially improves the PVCR to 2.8, which is a 1.8× increase compared to the baseline control Sample A.

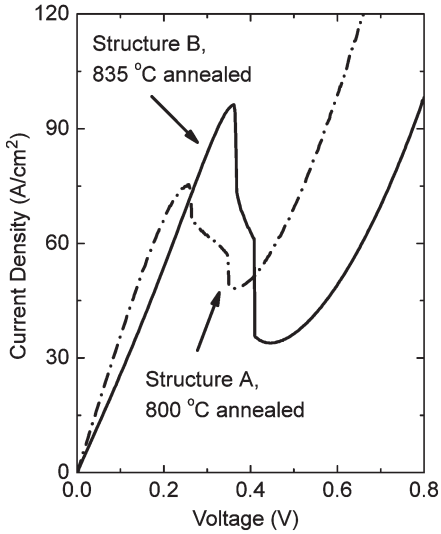

Fig. 4. Representative I–V characteristics from Structures A and B (18-μm diameter) annealed at their optimal temperatures, indicating that Structure B has a higher peak current concurrently with a lower valley current than the baseline sample.

Another significant performance difference between Structures A and B is the shift in the optimal annealing temperature to a higher temperature with Sample B. It has already been shown that higher annealing temperatures are more effective in reducing the defect-related tunneling currents that contribute to the excess current and are a major constituent of the valley current, putting a limit on the device PVCR [10], [11]. However, too high of an anneal temperature can lead to dopant interdiffusion across the narrow junction [5], [11]. The higher optimal annealing temperature of the RITD with strained Si cladding the P layer suggests that this structure is more immune to dopant diffusion at high annealing temperatures and withstands a higher thermal budget.

According to Christensen *et al.* [20], [21], P diffusivity in compressively strained $Si_{1-x}Ge_x$ only slightly increases with x because of the offsetting chemical and strain effects. Therefore, only a slight reduction in the P diffusivity is expected in the tensile strained Si layer of Sample B. The large and significant increase in electrical performance between the two structures tested cannot be explained by the slightly retarded P diffusion alone. A more complete explanation of the improved PVCR is that the strain-induced band offset also deepens the P δ-plane QW, as shown in Fig. 2. The optimal annealing temperature may also be increased because of the increasing strain-induced band offsets. Therefore, the modified RITDs of Structure B can be annealed at a higher temperature, which is more effective in reducing point defects such as vacancies, without a concurrent reduction in quantum confinement compared to the control sample, which shifts device operation to be more Esaki-like, leading to a loss in resonant interband tunneling. Fig. 4 shows the current–voltage (I–V) characteristics of the two structures annealed at their optimal temperatures. The comparison shows a higher peak current density and a lower valley current density in Structure B, hence a higher PVCR with the higher anneal temperature.

IV. Conclusion

In conclusion, Si-based RITDs grown on commercially available $Si_{0.8}Ge_{0.2}$ virtual substrates were studied. There are two advantages of using $Si_{0.8}Ge_{0.2}$ substrates: 1) the Ge content in the spacer can be increased without exceeding the critical thickness; and 2) a tensilely strained Si layer can be added, which provides flexibility in engineering the band structure of the RITD. By growing tensilely strained Si cladding the P δ-plane, the QW formed by the P δ-doping plane is deepened, and P outdiffusion possibly is suppressed, which leads to an increase in the optimal annealing temperature and greatly improved PVCRs.

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