The Effect of Spacer Thicknesses on Si-Based Resonant Interband Tunneling Diode Performance and Their Application to Low-Power Tunneling Diode SRAM Circuits

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***Abstract*—Si-based resonant interband tunneling diodes (RITD) with spacer thicknesses varying from 1 to 16 nm were grown and fabricated. The effect of spacer thickness on the peak-to-valley current ratio (PVCR), peak current density J_p, and voltage swing was studied. By increasing the tunneling spacer thickness up to 16 nm, RITDs with a J_p of as low as 20 mA/cm^2 with an associated PVCR of 1.6 were obtained, which are suitable for low-power tunnel diode SRAM applications. With the previously reported highest RITD J_p of 218 kA/cm^2, a J_p spanning nearly seven orders of magnitude can be obtained by engineering the tunneling spacer thickness and doping densities, thus demonstrating tremendous flexibility to optimize J_p for different circuit applications (logic, memory, and mixed-signal). Using a low-current-density RITD developed in this paper, a bread-boarded one-transistor tunneling-based SRAM (TSRAM) memory cell with low standby power consumption was demonstrated. This is the first report of a Si-based TSRAM memory circuit using Si-based RITDs. The result demonstrates the potential of Si-based tunnel diodes for low-power memory applications.**

***Index Terms*—Resonant interband tunneling diodes (RITD), Si, SiGe, SRAM, tunneling-based SRAM (TSRAM).**

I. Introduction

SINCE Si-BASED resonant interband tunneling diodes (RITD), which are compatible with ultralarge scale integration (ULSI) technology, were first developed by Rommel *et al.* [1], there have been a number of reported improvements in RITD dc performance [2]–[5]. Successes in their monolithic integration with CMOS [6] and Si/SiGe heterojunction bipolar transistor (HBT) [7] technologies have increased their interest as a possible thrust for extending Si technology using quantum functional circuitry. For instance, tristate logic operation has already been demonstrated by using a vertically and monolithically integrated RITD pair [8]. This paper examines Si-based RITDs for low-power memory circuits.

Prior Si/SiGe RITDs shared many key points that should be reviewed here as they will directly impact this paper: 1) p and n δ-doping injectors are used to create confined quantum wells. 2) A composite i-layer is inserted as a tunneling spacer layer between the δ-doped injectors to minimize dopant interdiffusion, which leads to a widening of the spacer and a larger tunneling distance. 3) Low-temperature molecular beam epitaxy (LT-MBE) is used to suppress segregation and diffusion. 4) A short postgrowth rapid thermal anneal (RTA) heat treatment is used to reduce point defects created during the LT-MBE process, which can lead to an elevated excess current via defect-related tunneling [9], [10].

The integration of tunneling diodes with transistors can increase circuit speed, reduce component count, and reduce power consumption [11]–[13], which are all synergistic with the goals of the International Technology Roadmap for Semiconductors (ITRS) [14]. One promising application of Si-based RITDs that is explored here is low-power tunneling-based SRAM (TSRAM) for memory circuits. TSRAM has already been demonstrated using III–V compound-based resonant tunneling diodes (RTD) [11], but this has been difficult to translate to a Si platform [15]. This paper explores the optimization of the SiGe RITD device for memory applications and applies it to the first reported Si-based TSRAM circuit prototype using RITDs.

TSRAM has the potential for compact and low-power embedded memory. Fig. 1 shows a schematic circuit of a one-transistor tunneling-based SRAM (1T TSRAM) proposed by van der Wagt [16], which consists of a pass transistor, a pair of tunnel diodes (TD), and a sensing capacitor that is inherent to the intrinsic TD. As a combination of a Goto cell [17] and a standard DRAM cell, the 1T TSRAM employs extremely low

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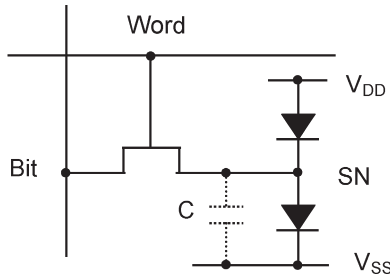

Fig. 1. Schematic of a 1T TSRAM memory circuit.

valley and peak current densities (PCD) to decrease the standby power consumption while sensing like a DRAM cell without the use of large restoring currents. This TD latch can maintain two stable storage node (SN) voltage levels as long as the cell leakage current through the transistor and capacitor is smaller than the TD peak-to-valley current difference [16].

The optimal TD for the 1T TSRAM application should have a low PCD to reduce overall power consumption and a sufficiently large peak-to-valley current ratio (PVCR) to ease the requirement for a small leakage current to ensure the latch points exist. The tunneling current decreases exponentially with the tunneling barrier thickness. A set of low-current-density RITDs with the intrinsic tunneling spacer thickness varied from 6 to 16 nm were fabricated in this study, which complements our previous work [4], where the spacer thickness was varied from 1 to 6 nm to achieve the goal of very high PCDs for high-speed mixed-signal circuit applications. We report here the dependence of J_p and PVCR on spacer thickness (1–16 nm).

For the 1T TSRAM application, the width of the TD current–voltage $(I–V)$ valley region affects the noise margin and required supply voltage, hence, the power dissipation. This width can be characterized by the voltage swing (VS), i.e., the value of V_s–V_p, where V_p is the voltage at which the peak current occurs the first time and V_s is the voltage at which the peak current is reached the second time on the upswing of the TD current, which is a combination of the forward-biased thermal diffusion current and the excess current created by defect-related tunneling and other leakage pathways. VS represents the voltage difference at the same amount of current, so it is not affected by the parasitic series resistance of the tunneling diodes. The effect of spacer thickness on VS is also studied here.

Using a 10-μm-diameter RITD with a measured PVCR of 2.2 and J_p of 0.5 A/cm^2 developed in this paper, a breadboarded 1T TSRAM cell was demonstrated with a standby power consumption of as low as 75 nW/cell. The result demonstrates the potential of this type of Si-based TDs for low-power memory applications.

II. Experimental Method

The basic structure of the Si-based RITDs, as shown in Fig. 2, is grown by LT-MBE. The spacer region, which is sandwiched between the two δ-doping layers, is comprised of two layers, namely 1) an intrinsic Si layer of thickness L that is below the P δ-doping layer and 2) a 4-nm intrinsic $Si_{0.6}Ge_{0.4}$ layer that is directly above the B δ-doping layer. The RITDs studied here varied the overall spacer thicknesses over

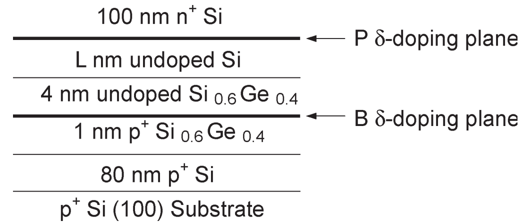

Fig. 2. Schematic of the basic Si-based RITD structures used in this paper. L is varied from 4 to 12 nm.

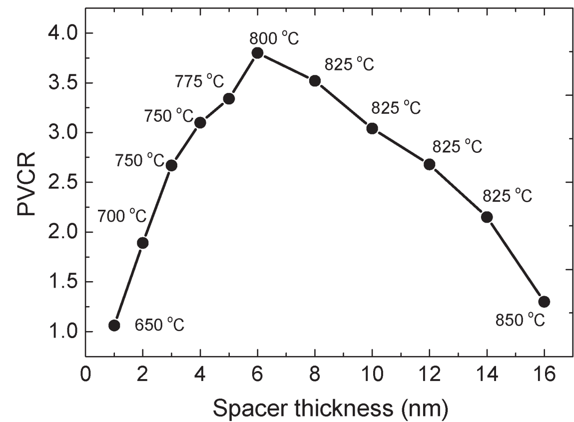

Fig. 3. Highest PVCR obtained from each RITD structure as a function of spacer thickness. The annealing temperature that yielded the maximum measured PVCR for a fixed 1-min annealing duration is also indicated.

6 $(L = 2$ nm), 8 $(L = 4$ nm), 10 $(L = 6$ nm), 12 $(L = 8$ nm), 14 $(L = 10$ nm), and 16 nm $(L = 12$ nm).

Epitaxial growth is achieved with a molecular beam epitaxy (MBE) growth system using elemental Si and Ge in electron-beam sources. The structures are grown on 75-mm B-doped $(\rho = 0.015 - 0.04\ \Omega \cdot \mathrm{cm})$ Si (100) wafers. The doping level for both n$^+$ and p$^+$ layers are 5×10^{19} cm^{-3}; the B and P δ-doping sheet concentrations are maintained at 1×10^{14} cm^{-2}. Prior to device fabrication, portions of the grown wafers were rapid thermal annealed using a forming gas ambient (N_2/H_2) in a Modular Process Technology Corporation RTP-600S furnace at various temperatures for 1 min. The tunneling diode fabrication process is described as follows. The first-level photolithography defines a photoresist mask for mesa etching of the diodes. HF/HNO_3 wet etching is then performed to isolate the diodes into mesas with various diameters. After stripping the photoresist, a photosensitive polyimide layer is spin coated on the wafer, followed by the second photomask level to define and open the contact windows for both the anode and the cathode. A third mask level is employed to define the interconnecting bond pads. A buffered oxide etch is used prior to the deposition of Pt/Al. Finally, the devices are silicided at 350 °C for 1 min.

III. Results and Discussion

A. *Effect of Spacer Thickness on PVCR*

At each spacer thickness, there exists an optimal annealing temperature for maximum PVCR [4]. Fig. 3 plots the highest PVCR obtained from each structure as a function of spacer thickness. The data for the RITDs with tunneling spacer thicknesses ranging from 8 to 16 nm are plotted together with

RITDs with spacer thicknesses ranging from 1 to 6 nm from a previous study [4]. The annealing temperatures used to obtain the PVCRs are also labeled. The graph shows that RITDs with a 6-nm spacer lead to the highest PVCR. Both decreasing and increasing spacer thicknesses will result in reduced PVCR. It is also observed that the optimal annealing temperature increases from 650 °C to 850 °C as the spacer thickness increases from 1 to 16 nm.

The current of an interband tunneling diode consists of three components, namely 1) quantum mechanical band-to-band tunneling through the barrier, 2) the excess current, principally through defects, and 3) the forward-biased thermal diffusion current. The excess current originates from electron tunneling through defects induced within the band-gap states. Chynoweth *et al.* [18] derived the excess current equation as

$$I_x = A \times D_x \exp\left\{ \left(\frac{-\alpha_x \times W \times e^{0.5}}{2}\right) \times \left[E_g - eV + 0.6e(V_n + V_p)\right] \right\} \quad (1)$$

where A is a voltage- and temperature-independent prefactor, D_x is the density of states in the band gap at a corresponding energy related to the forward bias V, α_x is a material constant containing a reduced effective mass, W is the tunneling barrier width, E_g is the band gap, e is the electron charge, V_n is the potential difference (in volts) between the Fermi level on the n-type side and the bottom of the conduction band, and V_p is the potential difference (in volts) between the Fermi level on the p-type side and the top of the valence band.

Since the thermal diffusion current contributes little to the valley current [18], the change of PVCR primarily results from the relative change between the desired band-to-band tunneling current and the excess current. Both the desired tunneling current and excess current are exponentially dependent on the tunneling barrier width according to Chynoweth's theory [18]. However, the decay rate of these two current components as the tunneling barrier width increases are likely to be quite distinct. Since the PVCR drops as the spacer thickness increases from 6 to 16 nm, it is hypothesized that the desired band-to-band tunneling current decays faster than the excess current with increasing tunneling barrier width. In other words, the tunneling selection rules are reduced for larger spacer thicknesses. The hypothesized tunneling selection rule can be validated by the fact that RITDs with thin spacers outperform RITDs with thick spacers under the same low-temperature annealing conditions. For example, an as-grown 3-nm-spacer RITD exhibits a PVCR of 1.6 with a significant number of point defects that have not yet been removed by postgrowth annealing, whereas an as-grown 16-nm-spacer RITD does not show significant negative differential resistance (NDR) until the annealing temperature is increased beyond 825 °C to remove the point defects. This fact indicates that a thin tunneling barrier intrinsically allows more desirable band-to-band tunneling current than excess current; therefore, a larger PVCR ensues. In essence, the characteristic length scale for the desired band-to-band tunneling is approximately the thickness of the tunneling barrier, whereas defect-related tunneling passes through at least one intermediary defect site within the tunneling barrier, so its effective length scale will be less.

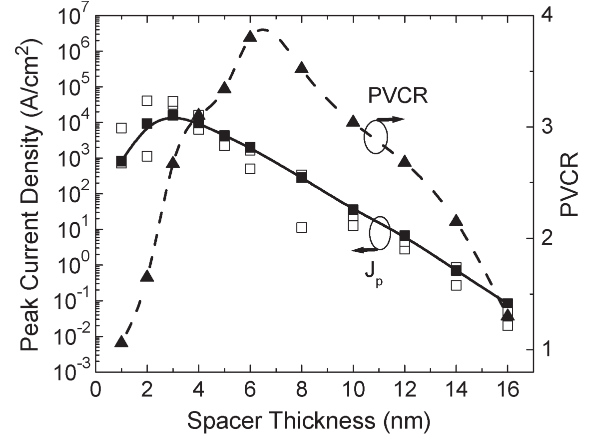

Fig. 4. Complete view of the effect of spacer thickness on PCDs and PVCR. The solid triangles (▲) indicate the maximum PVCR by varying the annealing temperature for each RITD spacer thickness. The solid squares (■) show the corresponding J_p at that optimized PVCR. The open square (□) illustrates the spread in J_p as the annealing temperature is varied. For clarity, the PVCR at different annealing temperatures is not plotted here.

When the spacer thickness is reduced from 6 to 1 nm, the PVCR decreases along with a lowering of the optimal annealing temperature, which seems to be in conflict with the hypothesized tunneling selection rules aforementioned. However, as the spacer thickness decreases for very narrow spacers, another phenomenon occurs. An increasing number of opposite carrier-type dopant pairs [18] are able to be formed within the tunneling barrier due to the close proximity of the B and P delta-doping layers, which partially interdiffuse with each other, and this is exacerbated as the tunneling spacer is reduced toward 1 nm. These dopant pairs can introduce energy states within the band gap [19], [20]; hence, they lead to a larger excess current relative to the tunneling current. Furthermore, the interdiffusion of dopants during postgrowth annealing leads to more dopant pairs being formed; therefore, RITDs with thin spacers have a lower optimal annealing temperature than RITDs with thick spacers. In another words, for RITDs with thin tunneling spacers, point defects formed during LT-MBE cannot be effectively removed because the annealing temperature has to be kept low enough so that minimal interdiffusion occurs and fewer dopant pairs are formed during the annealing process.

In general, optimal RITDs with thin spacers have more point defects and dopant pairs than optimal RITDs with thick spacers, which implies more excess current and smaller PVCR. However, the tunneling selection rules indicate that thin tunneling barriers intrinsically allow more desired band-to-band tunneling current than excess current. As a consequence of these two mechanisms, there exists an optimal spacer thickness for the highest PVCR, which occurs at 6 nm in this paper using this Si/SiGe RITD design.

B. *Effect of Spacer Thickness on PCD*

Fig. 4 plots J_p versus spacer thicknesses ranging from 1 to 16 nm. The highest PVCR obtained from each RITD structure

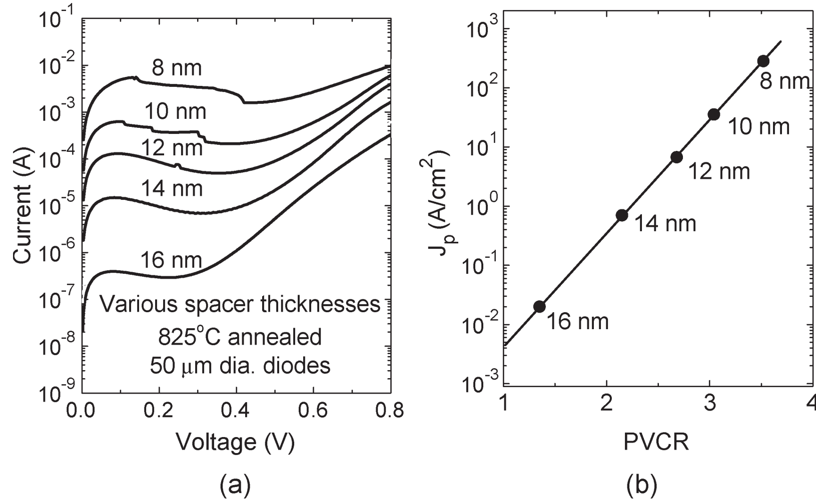

Fig. 5. (a) I–V characteristics of Si-based RITDs annealed at 825 °C with the spacer thickness varied from 8 to 16 nm on a semilog plot. (b) J_p as a function of PVCR for these RITDs.

as a function of spacer thickness is superimposed for comparison. The solid triangles (▲) indicate the maximum PVCR obtained by varying the annealing temperature for each RITD spacer thickness. The solid squares (■) show the corresponding J_p at that optimized PVCR. The open squares (□) illustrate the spread in J_p at various temperatures as the annealing temperature is varied. For clarity, the PVCRs at the different annealing temperatures examined are not plotted here. It is observed that J_p increases exponentially from 20 mA/cm^2 to 39 kA/cm^2 as the spacer thickness decreases from 16 to 3 nm, due to the decreasing tunneling barrier. Further reduction of the spacer thickness leads to a broadened depletion region due to dopant interdiffusion and a corresponding dopant compensation; therefore, J_p reduces. The relationship between J_p and spacer thickness W, in the range of 3–16 nm, can be fitted exponentially as

$$J_p = 0.996 \cdot 10^6 \cdot \exp(-0.604 \cdot W) \quad [\text{A/cm}^2]. \qquad (2)$$

By optimizing the doping density and using a P δ-peak sharpening technique, the highest J_p can be further increased to 151 kA/cm^2 with an improved PVCR of 2.0 [4]. Therefore, the J_p of Si-based RITDs can be varied nearly seven orders of magnitude from 151 kA/cm^2 down to 20 mA/cm^2, which demonstrates the tremendous flexibility in engineering J_p for different circuit applications (logic, memory, and mixed-signal).

Ideally, a low J_p could be obtained by simply increasing the spacer thickness. However, the decay of the PVCR with increasing spacer thickness sets a lower limit on J_p. Fig. 5(a) shows the I–V characteristics of the 825 °C 1-min-annealed RITDs with the spacer thickness varied from 8 to 16 nm. It clearly shows that the NDR region becomes diminished as the spacer thickness is increased. Fig. 5(b) plots the J_p as a function of PVCR for these RITDs. A linear correlation is observed between the J_p and PVCR. By extrapolating the measured data, a lower limit imposed on J_p can be projected to be about 4 mA/cm^2. An even lower J_p (< 4 mA/cm^2) might be achieved by further optimizing the RITD spacer configuration and the doping densities.

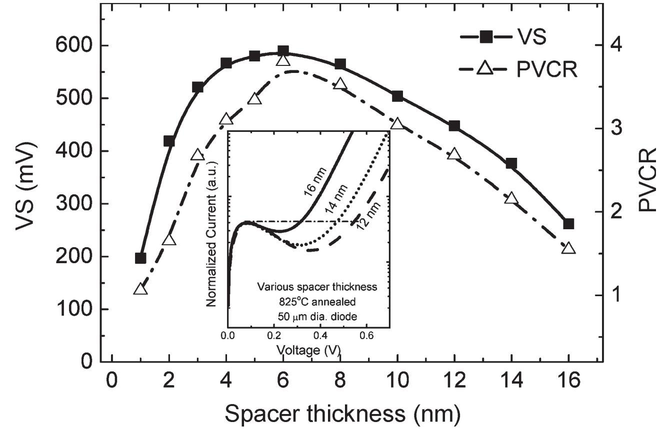

Fig. 6. VS is plotted as a function of spacer thickness. The PVCR is superimposed for comparison. The inset plots the normalized I–V characteristics of RITDs with 12-, 14-, and 16-nm spacers to illustrate the strong correlation between the PVCR and VS.

C. Effect of Spacer Thickness on VS

Like PVCR and J_p, VS depends on the annealing temperature. It is observed that the optimal annealing temperature for PVCR generally yields the highest VS. As shown in Fig. 6, which plots the highest VS and PVCR obtained from each structure versus the spacer thickness ranging from 1 to 16 nm, a good correlation between PVCR and VS is observed as the VS is generally also dependent upon the excess current [21]. For clarity, the I–V characteristics of diodes with 12-, 14-, and 16-nm spacers and annealed at 825 °C are normalized to have identical peak currents, and these are plotted in the inset of Fig. 6, which shows the strong correlation between the PVCR and VS. The I–V characteristics around the second voltage V_s appear to be a straight line when plotted on a semilog scale because the excess current dominates in this voltage

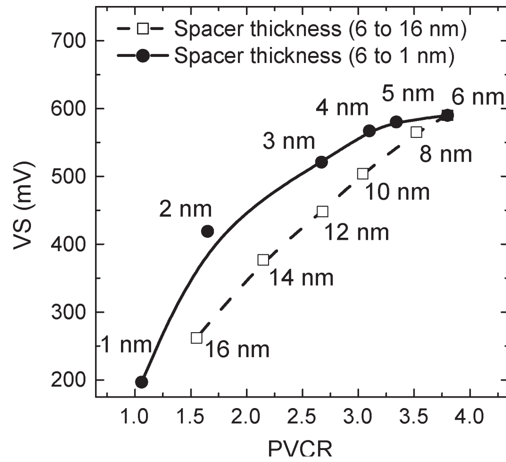

Fig. 7. VS is plotted as a function of PVCR.

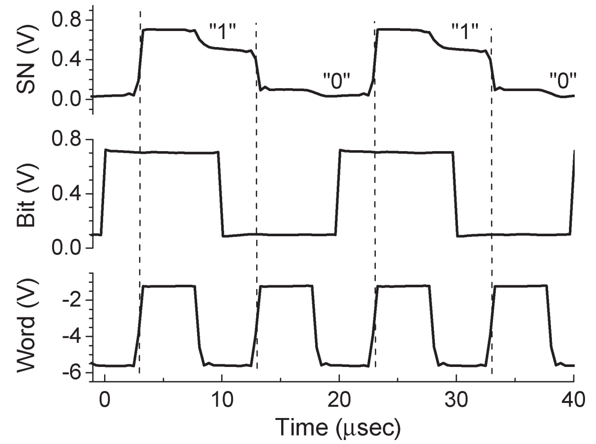

Fig. 8. Oscilloscope capture of the measured waveforms from the word line, bit line, and the resulting SN, showing the 1T TSRAM WRITE functionality.

range for a typical Si-based RITD. Assuming that the excess current components of all the diodes have the same slope in the semilog scale, i.e., $d(\log\ I)/dV$, a diode with a higher PVCR will show a larger VS because of the smaller valley current, hence, the larger VS. However, as depicted in (1), the value of $d(\log\ I)/dV$ is proportional to W, where a thicker tunneling barrier leads to a larger slope in the postvalley region on the semilog scale, as shown in Fig. 5(a). The dependence of the excess current slope on W implies that for two Si-based RITDs with the same PVCR, the RITD with a thinner tunneling barrier should exhibit a larger VS. This is verified by replotting the data of Fig. 6 into Fig. 7, where the VS is plotted as a function of PVCR instead of spacer thickness. The solid line, which represents the data from the RITDs with spacer thicknesses less than 6 nm, is above the dashed line, which represents the data of the RITDs with spacer thicknesses greater than 6 nm. Note that the solid line starts to drop sharply when the spacer thickness is reduced from 2 to 1 nm, which is indicative of the increased tunneling barrier width due to dopant interdiffusion that leads to compensation. It is also consistent with the fact that an RITD with a 2-nm spacer yields the highest J_p.

D. Demonstration of Si-Based 1T TSRAM and Comparison With Other Technologies

To demonstrate the concept of the 1T TSRAM memory cell shown in Fig. 1, a low-frequency breadboarded circuit is constructed using a commercial n-channel depletion-mode FET as the access control to the SN. To ease the requirement for small leakage current and to ensure latching characteristics, RITDs with 10-μm diameters, which exhibit a PVCR of 2.2 and a J_p of 0.5 A/cm^2, were fabricated and used in this circuit. The $V_{\rm DD}$ is biased at 0.5 V, and $V_{\rm SS}$ is grounded. Fig. 8 shows the signals of a 100-kHz word line and a 50-kHz bit line as well as the resulting waveform measured at the SN, clearly demonstrating the first Si-based tunneling-based SRAM (TSRAM) circuit. Unfortunately, the breadboarded circuit has too many parasitics to allow an accurate speed analysis.

The WRITE operation is effectively demonstrated. When the word line is high, the SN will copy the value from the bit line and keep latched until the next WRITE cycle begins. The states of 0 and 1 are 0.05 and 0.46 V, respectively. The standby power of this 1T TSRAM is estimated to be 75 nW/cell using the 10-μm diameter RITDs. Since previous Si-based RITD studies have shown no area dependence of the current density, the RITD area could be readily scaled downward accordingly, leading to a further reduction in standby power.

According to the 2005 technology node from the 2004 ITRS, a DRAM cell consisting of one transistor and one capacitor is expected to reach a size as small as 0.048 μm^2 with a minimum feature size of 80 nm. The total area required for a TSRAM cell is equivalent to a DRAM cell and occupies the space of one transistor. Since the leakage current pathway in the standby state of a TSRAM is only through the two vertically stacked RITDs in series assuming symmetric I–V characteristics [22], the relevant RITD area in calculating the power consumption is the minimum feature size, namely, 80 nm by 80 nm, needed to pattern the RITD stack atop the drain of one transistor. Thus, the standby power dissipation per TSRAM cell can then be estimated by

$$W = V_{\rm DD} \cdot I_{\rm STANDBY}. \tag{3}$$

Assuming that the 20-mA/cm^2 PCD RITD and the 2005 ITRS technology node are used for the TSRAM cell, the worst case scenario for the standby power dissipation $I_{\rm STANDBY} < I_{\rm PEAK}$, $I_{\rm STANDBY} <$ 20 mA/cm^2 is expected to be

$$\begin{aligned} W &= V_{\rm DD} \cdot I_{\rm STANDBY} \\ &= 0.5\ [\mathrm{V}] \times 1.3 \times 10^{-12}\ [\mathrm{I}] \\ &= 0.65 \times 10^{-12}\ \mathrm{W} \\ &= 0.65\ \mathrm{pW/cell}. \end{aligned} \tag{4}$$

Please note that this is an upper limit of the TSRAM power dissipation since the holding state of the TSRAM cell is not governed by the RITD peak current, but it is closer to the RITD's

valley current, where the actual latch points exist. Therefore, for 16 Mb of TSRAM, the standby power dissipation is expected to be lower than 11 μW. This compares favorably to 70 μW for 16 Mb of DRAM and 0.69 mW or 6.4 μW for 16 Mb of SRAM using low-operating-power technology or low-standby-power technology according to the ITRS [23], respectively. The RITDs have been studied over a wide temperature range in a few previous studies [24], [25]. In the RF study, only a 10% degradation in PVCR and a 22% increase in PCD was observed when the temperature changes from 20 °C up to 150 °C. It should be mentioned that more recent studies have pushed the reported Si/SiGe RITD current density up to 218 kA/cm^2 [26], and monolithically integrated TSRAM circuits operating down to 0.37 V have now also been reported, using NMOS and Si/SiGe RITDs with a 12-nm tunneling spacer [27].

IV. Conclusion

In this paper, the dependence of PVCR, J_p, and VS on spacer thickness is discussed. The highest PVCR results from a 6-nm tunneling spacer thickness. Thicker spacers lead to diminished PVCRs because the tunneling current decays faster than the excess current as the tunneling barrier thickness increases. Reducing the spacer thickness will also degrade the PVCR due to dopant pairs formed within the tunneling barrier that create energy states in the band gap. Increasing the spacer thickness from 3 to 16 nm leads to an exponentially decreasing J_p. A 16-nm tunneling spacer thickness yields the lowest J_p measured at 20 mA/cm^2. With the previously reported J_p of 218 kA/cm^2, the experimental J_p span of Si-based RITDs is nearly seven orders of magnitude. Reducing the spacer thickness to 1 nm does not yield a higher J_p because dopant interdiffusion effectively broadens the tunneling barrier. Spacer thickness affects the VS in the same way as it affects the PVCR. Furthermore, it affects the VS by changing the slope of the excess current on a semilog scale. A low-power 1T TSRAM is demonstrated using the low-current-density Si-based RITDs developed here. The results demonstrate the high potential of Si-based TDs for low-power memory applications.

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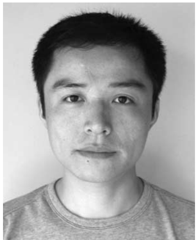

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