RF Performance and Modeling of Si/SiGe Resonant Interband Tunneling Diodes

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***Abstract*—The RF performance of two different Si-based resonant interband tunneling diodes (RITD) grown by low-temperature molecular beam epitaxy (LT-MBE) were studied. An RITD with an active region of B δ-doping plane/2 nm i-$Si_{0.5}Ge_{0.5}$/1 nm i-Si/P δ-doping plane yielded a peak-to-valley current ratio (PVCR) of 1.14, resistive cutoff frequency (f_{r0}) of 5.6 GHz, and a speed index of 23.3 mV/ps after rapid thermal annealing at 650 °C for 1 min. To the authors' knowledge, these are the highest reported values for any epitaxially grown Si-based tunnel diode. Another RITD design with an active region of 1 nm p+ $Si_{0.6}Ge_{0.4}$/B δ-doping plane/4-nm i- $Si_{0.6}Ge_{0.4}$/2 nm i-Si/P δ-doping plane and annealed at 825 °C for 1 min had a PVCR of 2.9, an f_{r0} of 0.4 GHz, and a speed index of 0.2 mV/ps. A small signal model was established to fit the measured S_{11} data for both device designs. Approaches to increase f_{r0} are suggested based on the comparison between these two diodes. The two devices exhibit substantially different junction capacitance/bias relationships, which may suggest the confined states in the δ-doped quantum well are preserved after annealing at lower temperatures but are reduced at higher temperature annealing. A comprehensive dc/RF semi-physical model was developed and implemented in Agilent advanced design system (ADS) software. Instabilities in the negative differential resistance (NDR) region during dc measurements were then simulated.**

***Index Terms*—Modeling, molecular beam epitaxial (MBE) growth, RF performance, Si/SiGe heterojunction, tunnel diodes.**

I. Introduction

Since Si-based resonant interband tunneling diodes (RITD) grown by low-temperature molecular beam epitaxy (LT-MBE) were first demonstrated by Rommel *et al.* [1], numerous studies have been carried out to improve their dc performance [2]–[5]. With recent demonstrations of monolithic integrations of RITDs with RITDs [6], HBTs [7], and CMOS [8], it is of prime interest to characterize their microwave performance, especially their resistive cutoff frequency f_{r0} and speed index s which is defined as the quotient of peak current over capacitance, for high-speed circuit applications. Microwave characterization of RITDs facilitates the establishment of an appropriate comprehensive dc/RF model that enables future RITD/transistor circuit development [9].

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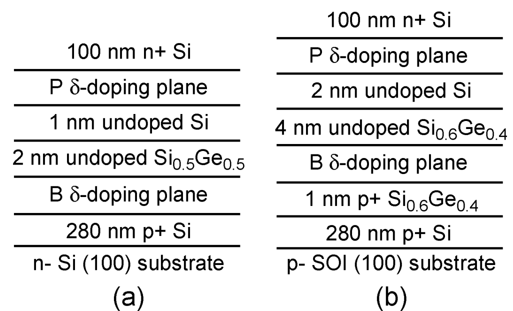

Fig. 1. Schematic of the RITD layer structures used in this paper. (a) Structure A is an RITD with a 3-nm-thick spacer. (b) Structure B is an RITD with a 6-nm-thick spacer.

For comparison, a typical 1960s Si alloyed Esaki diode exhibits a speed index of 1.2 mV/ps [10]. Recently, Auer *et al.* reported an epitaxially grown Si/SiGe ITD with a speed index of 0.5 mV/ps and an f_{r0} estimated as 1.5 GHz [11]. Dashiell *et al.* reported an epitaxially grown Si Esaki diode with a speed index of 7.1 mV/ps and f_{r0} of 1.6 GHz at 260 K [12]. In this paper, we studied the RF performance of two RITDs with different spacer configurations and annealing temperatures. The 650 °C annealed 3-nm-spacer RITD exhibits a resistive cutoff frequency f_{r0} of 5.6 GHz and a speed index of 23.3 mV/ps at room temperature, which are both the highest experimental values ever reported for any Si-based tunnel diodes. Based on the comparison of the RF performance and extracted circuit parameters of these two RITDs, several approaches are given to increase the f_{r0} of Si-based tunnel diodes. A comprehensive dc/RF tunnel diode model was developed and implemented in advanced design system (ADS) software (Agilent). DC instabilities during measurement over the negative differential resistance (NDR) region were then simulated.

II. Layer Design and Device Fabrication

Fig. 1(a) and (b) shows the schematic of the RITD structures used in this paper. Structure A used a 3-nm-thick intrinsic tunneling spacer with an active region of B δ-doped Si/2 nm

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i-$Si_{0.5}Ge_{0.5}$/1 nm i-Si/P δ-doped Si. It was designed to maximize the current density span, the difference between the peak and valley current densities. Compared to a previously reported structure showing the largest current density span of 76 kA/cm^2 [5], the Ge content was increased from 40% to 50% to reduce the tunneling barrier height and hence increase the peak current density (PCD). The increased Ge concentration also leads to better momentum mixing and less B diffusion into the tunneling barrier. The 1-nm SiGe cladding layer typically added under the B δ-doping layer [4] was removed to ensure the aggregate SiGe layer thickness did not exceed the total critical thickness. Structure B has a 6-nm-thick intrinsic spacer with an active region of 1-nm p+ $Si_{0.6}Ge_{0.4}$/B δ-doped Si/4 nm i-$Si_{0.6}Ge_{0.4}$/2 nm i-Si/P δ-doped Si, which was developed to maximize the peak-to-valley current ratio (PVCR) [4].

The two structures were grown by LT-MBE using elemental Si and Ge in electron-beam sources. The nominal doping level for both n^+ and p^+ injector layers are 5×10^{19} cm^{-3}, while both the B and P δ-doping sheet concentrations were maintained at 1×10^{14} cm^{-2}. Structure A was grown on a 75-mm P-doped (ρ = 3–7 $\Omega \cdot$ cm) Si (100) wafer, while Structure B was grown on a 100-mm B-doped silicon-on-insulator (SOI) (100) wafer.

Prior to device fabrication, portions of the as-grown wafers were rapid thermal annealed using a forming gas ambient (N_2/H_2) at various temperatures for 1 min. Arrays of diodes were fabricated using standard contact photolithography. Structure B was processed using a conventional double-mesa structure. The first mesa with a 10-μm diameter was defined by photoresist and formed by etching through the p-n junction using a $HF/HNO_3/H_2O$ (1/100/100) solution. The second mesa was aligned with the first mesa and formed by etching down to the SiO_2 layer using the same chemistry. A photosensitive polyimide layer, 800 nm thick, was then spincoated on the wafer followed by photolithography to open contact windows to both the anode and cathode. After curing the polyimide layer in a N_2 ambient, another level of lithography was performed to define the probe pads. Finally, a Ti/Al/Au (15/100/200 nm) multilayer for both ohmic contact and RF probing pads was deposited followed by liftoff. No contact annealing was performed.

The above-mentioned process is not suitable for the fabrication of Structure A due to stability issues caused by the ultrahigh PCD. To make a valid RF measurement, the tunnel diode should be stable when it is biased in its NDR region. The stability criteria [13] is

$$R < \frac{(V_v - V_p)}{(I_p - I_v)} \tag{1}$$

and

$$\frac{L}{R} < C|R_n| \tag{2}$$

where R and L are the series resistance and inductance, respectively. C is the junction capacitance and R_n is the differential resistance dV/dI. Oscillations will take place in the NDR region if either of these two criteria are not satisfied. Therefore, Structure A with an ultralarge current density span should have a very small diode size and small series resistance to satisfy the first inequality (1). A 1-metal fabrication process [11] and self-aligned Ni silicidation process was employed to fabricate Structure A. The first lithography step defines both the anode and cathode contact, as well as the probe pads, followed by deposition and lift-off of Ni/Cr/Au (6/100/200 nm) using electron beam evaporation. After lift-off, the sample was annealed at 420 °C for 5 min to form the Ni silicide. Cr prevents the interdiffusion of Au into the silicide. $KOH/IPA/H_2O$ (76/50/140) solution was used to etch through the tunnel junction. The mesas were oriented 45° to the $\langle 110 \rangle$ direction to form a vertical sidewall. The second lithography step defined a photoresist etching mask that protects the RITD mesa but defines the isolation area. The second etching step uses an $HF/HNO_3/H_2O$ (1/100/100) solution to etch down to the n- substrate. This etching step effectively isolates the active mesa from the epi-layer under the signal pad. Fig. 2(a) shows a scanning electron microscopy (SEM) photomicrograph of a representative device. The airbridge formed by the large undercut is clearly visible. Fig. 2(b) illustrates the device structure from a cross-sectional view along the finger. Note that the serially connected parasitic tunnel diode under the ground pad will be reverse biased when the device under test (DUT) is forward biased. This junction acts as an extremely small resistance due to its large size (~ 0.05 mm^2) and inherent large junction conductance resulting from the thin tunneling barrier.

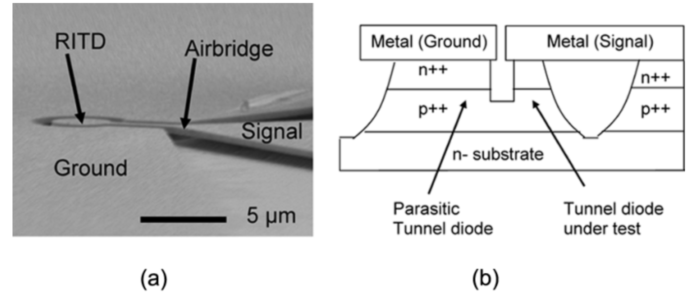

Fig. 2. (a) SEM photomicrograph of a fabricated RITD (Structure A). The airbridge is clearly visible. (b) Schematic view of the device structure.

The active mesa area of the fabricated RITD is greatly dependent on the amount of undercut created during the second etching step. To estimate the active device area, the PCD of a 5×5 μm calibration diode was measured before the second etching step. Since no clear dependence of PCD on junction area was observed, the active device area for Structure A studied in this work can then be estimated by assuming a constant PCD with high accuracy.

III. Device Performance

The room temperature dc current–voltage (*I–V*) characteristics were measured using an Agilent 4156C parameter analyzer. A detailed analysis of each sample processed was performed that tested a large number of devices and representative *I–V* characteristics recorded. Structure A, annealed at 650 °C for 1 min, resulted in a PVCR of 1.14 with a peak current of 5.4 mA (*I–V* characteristics shown in Fig. 5). The estimated PCD and junction area are 152 kA/cm^2 and 3.55 μm^2, respectively, which is comparable to the performance of a previously reported Si-based RITD annealed at 575 °C showing a record

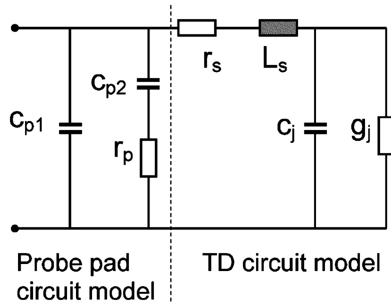

Fig. 3. Small-signal equivalent circuit of the RITDs and the probe pads.

high PCD of 151 kA/cm^2 with a PVCR of 2.0 [5]. Structure B, annealed at 825 °C for 1 min, resulted in a PVCR of 2.9 with PCD of 316 A/cm^2 (*I–V* characteristics shown in Fig. 8). Note the 6-nm spacer results in a higher PVCR but much smaller PCD than the 3-nm spacer, due to the exponential decay of current through thicker barriers and enhanced selectivity rules.

Small signal RF performance of representative devices were characterized using an Agilent 8510C network analyzer. The 50 Ω coplanar microwave probes were calibrated by the short-open-load-through method before measurements of the diodes. S_{11} of both diodes and on-wafer short- and open-pad test structures were measured from 100 MHz to 20 GHz in steps of 0.1 GHz. The bias voltage was swept from 0 mV to 0.7 V in 10 to 50 mV steps. The RF signal delivered to the diodes was estimated to be 10 mV peak-to-peak.

Although the 6-nm-spacer and 3-nm-spacer RITDs were fabricated using different methods and have different structures, their probing pads can be modeled using the same basic equivalent circuit model, shown in Fig. 3. C_{p1} and r_p represent the fringe capacitance and resistive substrate loss, respectively for both structures. C_{p2} represents the PN junction capacitance for the 3-nm-spacer RITD grown on n- type substrate and SiO_2 capacitance for the 6-nm-spacer RITD grown on p- type SOI substrate. The intrinsic RITDs were modeled with a series resistance (r_s), series inductance (L_s), junction capacitance (C_j), and junction conductance (g_j). ADS software was used to fit the measured S_{11} data to the equivalent circuit model. The pad parameters were determined by fitting the equivalent circuit model to measured open- and short-pad test structures. The intrinsic S_{11} data of the measured RITDs was then deembedded from the parasitic effects of the probe pads. The individual circuit parameters of the tunnel diode model were then determined by fitting the equivalent circuit model to the deembedded S_{11} data for each of the RITDs.

Bias dependent f_{r0} of Structure A annealed at 650 °C with an estimated active area of 3.55 μm^2 is plotted in the inset of Fig. 4. By biasing the diode at 580 mV (NDR region), the RITD exhibits a f_{r0} of 5.6 GHz, which is nearly four times higher than previously reported values [11], [12]. To the authors' knowledge, this is the highest f_{r0} ever reported for any epitaxially grown Si-based tunnel diode. The symbols in Fig. 4 represent the measured impedance of the intrinsic diode, which was computed from the deembedded S_{11}, as a function of frequency at three representative bias voltages: 500 mV (prepeak region), 580 mV (NDR region) and 700 mV (post-valley region). The solid lines in Fig. 4 are the fitted impedance, which is in very

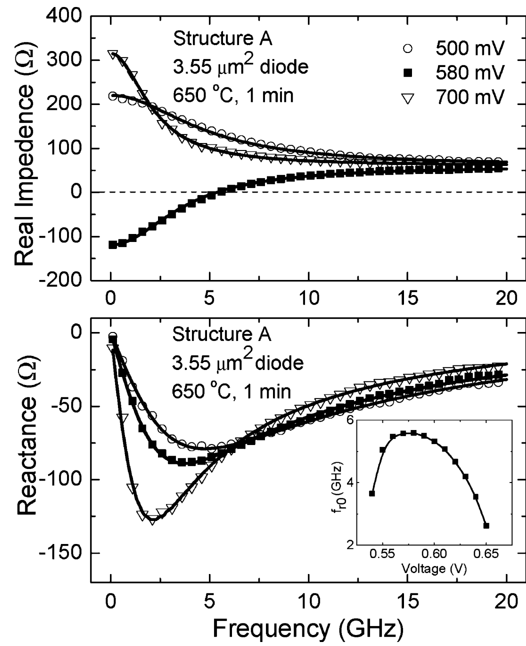

Fig. 4. Comparison of measured impedance (scattered symbols) and modeled impedance (solid lines) at 3 representative bias voltages for Structure A annealed at 650 °C. The real components are plotted in the upper figure and the imaginary components are plotted in the lower figure. The three bias voltages plotted are 500 (prepeak region), 580 (NDR region), and 700 mV (post-valley region). The inset shows f_{r0} as a function of bias voltage. The maximum f_{r0} of 5.6 GHz was obtained at a 580–mV bias voltage.

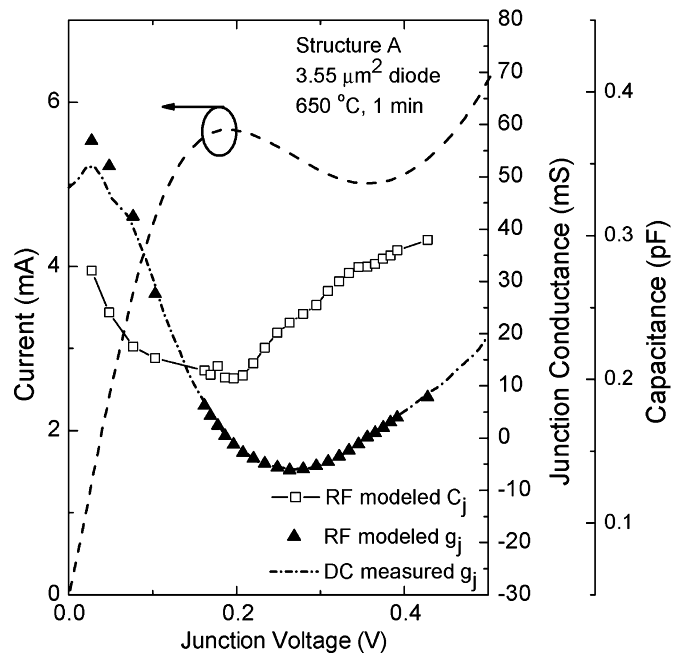

Fig. 5. Extracted g_j and C_j are plotted as a function of junction voltage for Structure A annealed at 650 °C. The intrinsic dc *I–V* characteristics are superimposed. g_j is also computed from the intrinsic dc *I–V* characteristic. Very good agreement between RF modeled and dc measured g_j is obtained.

good agreement with the measured values. The bias independent elements r_s and L_s were extracted as 60.7 Ω and 0.41 nH, respectively. Fig. 5 shows the extracted junction capacitance, C_j, as a function of the actual junction voltage, which

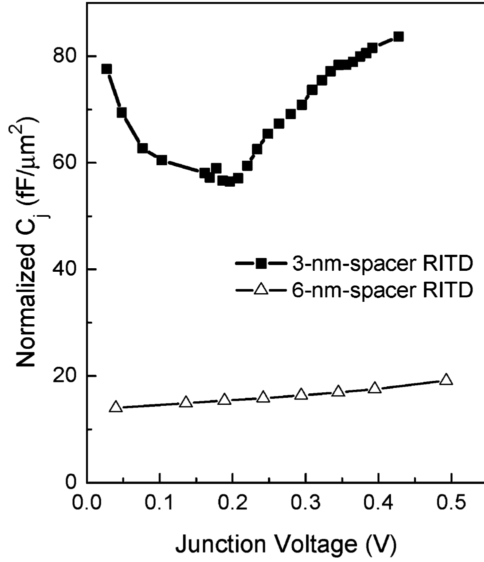

Fig. 6. Comparison of normalized C_j of Structure A annealed at 650 °C and Structure B annealed at 825 °C.

was computed by subtracting the voltage drop across r_s from the total external bias voltage. The dc *I–V* characteristic of the intrinsic tunnel diode (deembedded from r_s) is then superimposed in Fig. 5 as the dashed line. The extracted junction conductance, g_j, as a function of junction voltage is also shown in Fig. 5. The g_j was also computed by taking the first derivative of the intrinsic dc *I–V* characteristic. The computed g_j was then plotted in Fig. 6 as the dashed-dotted line. Excellent agreement between the junction conductance obtained from RF measurements and dc measurements was observed, which indicates the equivalent circuit model, shown in Fig. 3, fully describes the physical processes [14]. The excellent agreement also suggests that bias dependent g_j can be accurately computed from the intrinsic dc *I–V* characteristic without taking RF measurements. When the bias voltage is 580 mV in the NDR region (corresponding to a junction voltage of 249 mV), the extracted C_j and g_j are 232 fF and −5.6 mS, respectively. According to (3) [15], f_{r0} is calculated to be 5.4 GHz, which is in close agreement to the measured value of 5.6 GHz

$$f_{r0} = \frac{|g_j|}{2\pi C_j}\sqrt{\frac{1}{r_s|g_j|} - 1}. \qquad (3)$$

The speed index can be calculated as $s = \mathrm{Ip/C} = 5.4\ \mathrm{mA}/232\ \mathrm{fF} = 23.3\ \mathrm{mV/ps}$, which is also the highest value ever reported for any epitaxially grown Si-based tunnel diode. Table I summarizes the prior measured f_{r0} and speed index of various Si-based tunnel diodes reported by different groups.

The maximum f_{r0} of Structure B annealed at 825 °C was determined to be 0.4 GHz at a junction voltage of 196 mV for a 10 μm diameter device. The same S_{11} parameter fitting procedure was performed to extract its circuit element values. To understand the performance difference between the two RITDs, the extracted C_j, $|g_j|$, and r_s of both Structure A and Structure B at their best bias voltages were normalized with junction area and summarized in Table II with other important parameters.

TABLE I
PREVIOUSLY REPORTED PERFORMANCE OF VARIOUS EPITAXIALLY GROWN Si-BASED TUNNEL DIODES BY DIFFERENT GROUPS. NOTE, ONLY TUNNEL DIODES WITH MEASURED f_{r0} AND SPEED INDEX ARE LISTED

First Author/year	Type	Fabrication Method	f_{r0} (GHz)	Speed index (mV/ps)	PCD (kA/cm²)	PVCR
Auer [11], 2001	Si/SiGe ITD	MBE	1.5	0.45	1.52	2.1
Dashiell [12], 2002	Si Esaki	MBE	1.6	7.1	16	1.04
Yan [16], 2004	Si Esaki	RTP*	~0.45	0.23	0.27	2.15
This work	Si/SiGe RITD	MBE	5.6	24.6	152	1.14

* Rapid thermal processing

Assuming $r_s \cdot |g_j| \ll 1$, the ratio of the maximum f_{r0} of two tunnel diodes can be approximated as

$$\frac{f_{r0}^A}{f_{r0}^B} = \frac{\sqrt{|g_j^A| \cdot r_s^B} \cdot C_j^B}{\sqrt{|g_j^B| \cdot r_s^A} \cdot C_j^A}. \qquad (4)$$

With a smaller spacer thickness and lower annealing temperature, Structure A has a thinner tunneling barrier than Structure B. Also, the Ge content within the spacer layer of Structure A is higher than that of Structure B, which lowers the tunneling barrier height, increases momentum mixing, and consequently further increases the tunneling probability. These factors lead to a ~4.2 times larger normalized C_j and ~155 times higher normalized $|g_j|$, as shown in Table II. According to (4), this results in a ~3.0 times improvement of f_{r0}. Table II also shows that the normalized r_s of Structure A is significantly smaller than Structure B, which leads to a ~4.7 times improvement of f_{r0} according to (4). There are two reasons which account for the significant difference in normalized r_s: First, the Ni silicide ohmic contact is only used to reduce the series resistance for Structure A. Second, the contact resistance does not scale accordingly with area [17], i.e., Structure A will have a smaller normalized r_s even if the same Ni silicide ohmic contact is used in both diodes.

Equation (4) and the comparison between Structures A and B suggest several approaches to increase f_{r0} of Si-based tunnel diodes:

1) An ultrathin tunneling barrier is desirable for high f_{r0}, even though it will lead to a larger normalized C_j. This is because the PCD exponentially increases as the tunnel barrier thickness decreases, causing an exponential increase of normalized $|g_j|$ (even with a unfavorable PVCR drop [5]), which will outweigh the losses from the linearly increasing normalized C_j.
2) Increase the Ge content within spacer layer to enhance the tunneling probability, hence normalized $|g_j|$, with only a slightly increased normalized C_j due to higher dielectric constant of Ge.
3) Reduce contact resistance thereby normalized r_s. Extremely low contact resistance in the range of $10^{-7}\ \Omega\cdot\mathrm{cm}^2$ has already been obtained from state-of-the-art Ni silicide technology [18], [19]. The implementation of such Ni silicidation process on Structure A would result in a normalized r_s in the range of 10 $\Omega \cdot \mu\mathrm{m}^2$, which could lead to a f_{r0} of 26.6 GHz (4.7 times improvement).

TABLE II
COMPARISON BETWEEN RITDs OF STRUCTURE A AND B. THE NORMALIZED C_j, $|g_j|$ OF STRUCTURE A AND B ARE THE VALUES AT JUNCTION VOLTAGE OF 249 AND 196 mV, RESPECTIVELY

	Structure A	Structure B
Spacer thickness (nm)	3	6
Annealing temp (°C)	650	825
Ge content	50%	40%
Diode area (μm²)	3.55	78.50
PVCR	1.14	2.9
PCD (kA/cm²)	152	0.316
Speed index (mV/ps)	23.3	0.2
Maximum f_{r0} (GHz)	5.6	0.4
Normalized $\|g_j\|$ (ms/μm²)	1.55	0.01
Normalized C_j (fF/μm²)	65.3	15.4
Normalized r_s (Ω·μm²)	216	4789

4) Scaling down RITD will reduce its normalized r_s, thereby improve f_{r0}, assuming the normalized C_j and $|g_j|$ are area independent.

It is interesting to note for Structure A that C_j reaches its minimum value when the current reaches its peak value (Fig. 5). The observed capacitance–voltage (*C–V*) trend is significantly different from the *C–V* trend reported for an Esaki diode [20], in which the Esaki junction capacitance monotonically increases with the bias voltage as a result of a narrowed depletion region. The anomalous capacitance change for these Si-based RITDs may result from charge redistribution within the triangular quantum well as the bias voltage is varied. The 825 °C annealed Structure B shows a monotonically increased C_j with junction voltage (Fig. 6), which is characteristic of Esaki diodes. The different *C–V* relationship of 650 °C annealed and 825 °C annealed RITDs may suggest that annealing at too high a temperature (825 °C) will diffuse dopants enough that the δ-doped quantum wells may lose their confinement, effectively rendering the RITD structure into an Esaki diode.

IV. COMPREHENSIVE DC/RF MODEL

A comprehensive dc/RF model which incorporates both the equivalent circuit model and dc *I–V* characteristics was developed for InGaAs/InAlAs ITDs in monolithic microwave integrated circuits [9]. In this section, a similar dc/RF model for Structure B is developed.

Fig. 7 shows the comprehensive dc/RF ITD model. R_s is the series resistance determined in the small signal model. $C_j(V)$ is a fitted polynominal function of the extracted C_j. The $I_j(V)$ is the intrinsic dc *I–V* characteristics which is deembedded from the R_s effect. In the InGaAs/InAlAs ITDs dc/RF model [9], $I_j(V)$ is a polynominal fit of the measured data, which is not

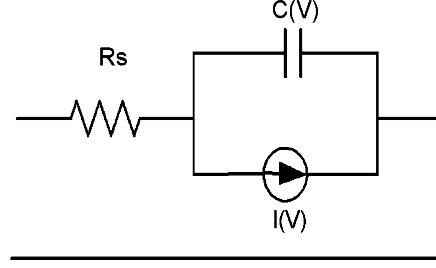

Fig. 7. Comprehensive dc/RF model of the RITDs studied here.

TABLE III
PARAMETER VALUES AFTER FITTING THE *I–V* CHARACTERISTICS FOR STRUCTURE B ANNEALED AT 825 °C

Parameter	Value
I_p	2.4×10^{-4} A
V_p	0.01 V
I_e	1.7×10^{-6} A
W	8.0
I_0	3.0×10^{-13} A
n	1.3

physically meaningful. In our semi-physical model, the forward *I–V* characteristics of the RITD was modeled by the summation of its three current components: tunneling current I_t, thermal diffusion current I_{th}, and excess current I_e.

The tunneling current can be expressed using the empirical equation [21]

$$I_t = I_p \times \left(\frac{V}{V_p}\right) \times \exp\left(1 - \frac{V}{V_p}\right) \tag{5}$$

where I_p is the peak tunneling current, V_p is the peak voltage, and V is the bias voltage. The thermal diffusion current is the standard diode equation expressed as

$$I_{\text{th}} = I_0 \times \exp\left(\frac{V}{nkT} - 1\right) \tag{6}$$

where I_0 is the reverse saturation current, n is the ideality factor, and kT is the thermal energy. Since the excess current is exponentially dependent on the bias voltage as suggested by Chynoweth [22], it can be simply expressed as

$$I_e = I_e \times \exp(W \times V) \tag{7}$$

where I_e and W are constant.

The parameters I_p, V_p, I_e, W, I_0, and n were optimized to fit the intrinsic *I–V* characteristics for Structure B using ADS software. The parameter values resulting from the optimization are listed in Table III. Fig. 8 shows the intrinsic *I–V* characteristics and the modeled *I–V* characteristics, as well as the three current components. Excellent agreement between the intrinsic and modeled *I–V* characteristics was obtained.

The comprehensive dc/RF model shown in Fig. 7 was then implemented using ADS software to simulate the instability and oscillation that are commonly observed during dc electrical measurements. The tungsten wire probe commonly used for dc measurements acts as a series inductor, which causes oscillations during dc measurements when the second stable condition (Inequality 2) is no longer met. The commonly observed

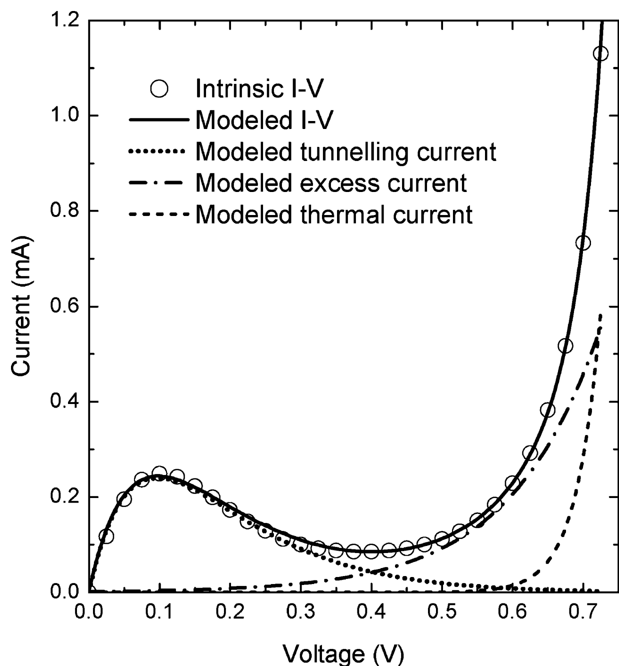

Fig. 8. Comparison of intrinsic and modeled *I–V* characteristic. The three modeled current components band-to-band tunneling, diffusion, and excess current are also plotted.

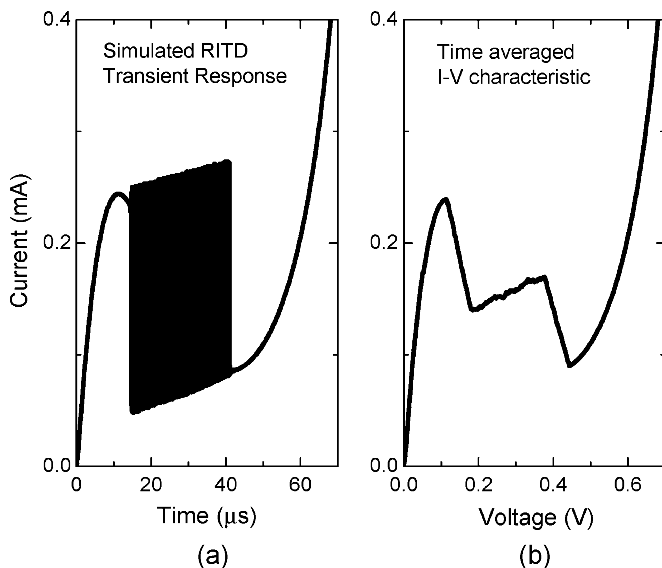

Fig. 9. (a) Simulated transient current showing strong oscillations when Structure B annealed at 825 °C is biased in the NDR region. (b) Simulated time-averaged *I–V* characteristic showing the plateau in the NDR region.

plateau, or hump in the NDR region is an indication of these oscillations and sometimes appears singly or multiply. A transient simulation was performed to emulate the response of the measured diode with a serially connected 50 μH inductor to a bias voltage ramped from 0 to 1 V in 0.1 ms. The simulated transient current was then averaged over time to mimic the integration process of the dc measurement using a parameter analyzer. Fig. 9(a) shows the simulated transient current, where strong oscillations occur when the diode is biased into its NDR region. Fig. 9(b) shows the resulting time-averaged *I–V* characteristic, a plateau in the NDR region was observed.

V. Conclusion

The RF performance of two different Si-based RITD structures were studied. Structure A annealed at 650 °C exhibits an f_{r0} of 5.6 GHz and a speed index of 23.3 mV/ps, which are both the highest values ever reported for any epitaxially grown Si-based tunnel diodes. Structure B annealed at 825 °C shows an f_{r0} of 0.4 GHz. The performance difference between these two diodes suggests thinner tunneling barrier, higher Ge content within spacer, better ohmic contact, and smaller junction area are desirable for higher f_{r0}. A f_{r0} well over 10 GHz can be obtained by optimizing the growth and fabrication process. A comprehensive dc/RF model was developed and implemented in ADS. The instabilities in the NDR region during dc measurements were simulated.

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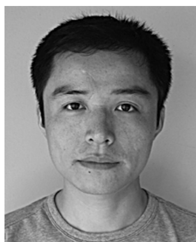

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