Capacitance-Voltage Characterization of Pulsed Plasma Polymerized Allylamine Dielectrics for Flexible Polymeric Field Effect Transistors

YIFAN XU,[1] PAUL R. BERGER,[1,3] JAI CHO,[2] and RICHARD B. TIMMONS[2]

1.—Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210. 2.—Department of Chemistry and Biochemistry, University of Texas, Arlington, TX 76019. 3.— Department of Physics, The Ohio State University, Columbus, OH 43210; e-mail: pberger@ieee.org

Polyallylamine films, deposited on Si wafers by radio frequency (RF) pulsed plasma polymerization (PPP), were employed as insulating layers of metal-insulator-semiconductor (MIS) capacitors. The insulating polymer films were deposited at plasma reactor temperatures of 25°C and 100°C. Multiple frequency capacitance-voltage (C-V) measurements indicated that an in-situ heat treatment during film deposition increased the insulator dielectric constant. The dielectric constant, calculated from the C-V data, rose from 3.03 for samples with no heat treatment to 3.55 for samples with an in-situ heat treatment. For both sample sets, the I-V data demonstrates a low leakage current value (<20 fA) up to 100 V. Capacitance-time (C-t) measurements were also used to characterize the mobile ions in the polymer that migrate over time with applied voltage. Results indicate that the polymer layers contain few electrically active defect centers and virtually no pinholes. Hysteresis in the C-V curves with differing sweep directions was more pronounced for in-situ heat-treated samples indicative of mobile charge.

Key words: Polymerized allylamine, dielectrics, Si, MIS capacitors

INTRODUCTION

Polymer electronics are gaining considerable attention, but more effort is needed to reach a satisfactory solution for an all-polymer field effect transistor (FET). Replacing the traditional silicon dioxide gate dielectric with a suitable polymer dielectric would enable flexible electronics and displays.

Synergistically, the Si complementary metal-oxide semiconductor (CMOS) community is also seeking both alternative high dielectric gate insulators to replace the traditional thermally grown SiO_2 and new low dielectric constant materials for interconnect technology. Thermally grown SiO_2 has been the most popular gate dielectric for Si metal-oxide-semiconductor FETs (MOSFETs), but it cannot satisfy the long-term needs because MOSFET critical dimensions shrink below the 130-nm node. Substitute dielectrics are needed to relax the gate dielectric thickness and to reduce the parasitic capacitive coupling overlap created by multiple interconnect levels.

Polymer FETs (PFETs) have been available for only a little more than 1 year, and most work on PFETs has focused on semiconducting polymers for the active component, often neglecting the gate dielectric material. These prior PFET investigations often adopted SiO_2 as the gate insulator due to its maturity and convenience. However, to reflect the most attractive advantage of polymeric devices, the ultimate aim is to find a flexible gate insulator. Unfortunately, most effort on alternative gate dielectrics has been driven by the Si CMOS community and focuses on advanced inorganic gate dielectrics using high-permittivity materials. These materials include Al_2O_3, Ta_2O_5, HfO_2, ZrO_2, Zr silicate, and Hf silicate.[1–3] It is clear that, whereas these high-k dielectrics may be suitable for Si CMOS applications, in view of their rigidity, they are unsuitable for flexible devices.

(Manuscript received November 22, 2003; accepted June 18, 2004)

Polymeric gate dielectrics are a natural choice for these flexible insulators. Early work on polymers only considered these materials to be insulators, until conductive polymers were discovered in 1977.[4] The long history of polymers, the wide variety of choices, and the maturity of polymer manufacturing facilitate the future commercialization of polymer electronics based on PFETs.

A few groups reported results on PFETs using polymer insulators. Garnier et al. used a sheet of commercially available polyester film polyethylene terephthalate. The film was 1.5-μm thick, and its flatness was achieved by fixing it to a frame. This method is inspiring for an all-polymer PFET, though its reliability needs to be improved.[5] Drury et al., Sirringhaus et al., and Kawase et al. all used spin-coated polyvinylphenol from either isopropanol or isopropanol:xylene solutions as the gate dielectric.[6–8] Narayan and Kumar used polyvinyl alcohol cast from an aqueous solution.[9] Solution-processed polymer insulators have obtained reasonable and controllable thicknesses for very large PFETs, but it will be challenging to achieve the ultra-thin thickness and uniformity for scaled PFETs.

Attention must also be paid to the possible intermixing of polymer dielectrics and polymer semiconductors that are solution based. It is quite possible that these two polymers would dissolve each other when deposited as an overlayer. Also, the type and amount of impurities contained in solution is difficult to control, so it is hard to predict what charges and traps will exist at/near the PFET insulator/semiconductor interface. This brings another concern to PFET performance. To produce repeatable and predictable PFETs, detailed information on the gate insulator is necessary. High homogeneity and good dielectric properties are essential in obtaining high-performance devices. However, to date, no electrical characterization of the polymer insulator or interface has been cited, except its overall thickness.

This paper describes recent progress made using radio frequency (RF) pulsed-plasma polymerization (PPP) to create suitable gate dielectrics. Fourier transform infrared spectroscopy (FTIR), capacitance-voltage (C-V), and current-voltage (I-V) characterization were employed to characterize the RF pulsed-plasma-deposited polyallylamine.

BACKGROUND

Plasma polymerization has gained increasing interest for its ability to engineer compositions of thin film materials in one relatively simple step. A wide variety of monomers are available as precursors, and the composition and structure of the deposited polymer layer can be tailored by adjusting the plasma deposition parameters, such as input power, discharge pressure, composition of the gas feeds, and the deposition temperature. A comprehensive introduction to all major aspects of plasma polymerizations has been provided by Yasuda.[10] In the present studies, an RF powdered plasma discharge, operated at a frequency of 13.56 MHz, was employed. Metal electrodes, located externally to the glass reactor to avoid metal atom contamination of the polymeric films, were used to deliver the RF power. A pulsed plasma discharge was employed in lieu of the more conventional continuous-wave operational mode. The pulsed mode was employed to provide enhanced control of film chemistry during the deposition process.[11]

Dielectric constant and breakdown electric field are the two most important electrical parameters for characterizing a dielectric material. Dielectric constants are determined from the measured capacitance data and known device dimensions. Leakage current measurements indicate the electrical integrity of the insulator. This information can be used to compute the breakdown electric field provided the insulator thickness is known. Since the insulator in the metal-insulator-semiconductor (MIS) structure essentially blocks the dc current flow between the two electrode plates (except small leakage currents), the major diagnostic technique to characterize MIS capacitors is C-V analysis. During a C-V measurement, both a dc voltage and an ac signal are necessary for the C-V measurement. A dc voltage is applied to the device to determine the base bias condition. A small-signal ac voltage is superimposed on the base bias and its variation gives rise to the variation in measured charges by modulation of the semiconductor depletion layer. The charge variation results in a detectable capacitance.[12]

In the course of exploring a new material as gate insulator, capacitance characterization is of practical importance and C-V characterization has typically been monitored. Measured C-V data and parameters extracted from the new polymer MIS structure are presented and compared to those of traditional Si MOS. As discussed below, these parameters provide quantitative measures of the advantages and disadvantages of these new materials or techniques under consideration. Note that the polymer MIS structure is built on a traditional Si wafer so that the channel occurs at the Si surface. This will facilitate comparison to known Si MOS structures by substituting only the dielectric. The actual measured data can also be compared with the theoretical data to identify deviations from the ideal in both the insulator and the semiconductor.

The application of C-V characterization has already extended into PFET research. Scheinert et al.[13] inspected the C-V characteristic of arylamino-PPV MIS capacitors to study the field effect in organic devices. In accumulation, the insulator capacitance is only found for low frequencies. At positive gate voltages, PFET inversion has not been observed. The low mobility causes a high relaxation time. The measured characteristics show a large hysteresis for different sweep directions and a shift of the curves for repeated measurements. This work shows that C-V characterization can be of great help to demonstrate the field effect in PFETs.

The main reason to look for a polymer replacement for SiO_2 in polymer devices is because of its rigidity, which contradicts the desired flexibility for PFETs. Plasma polymerization has gained large attention in new material development and treatment, but it is still new in the field of microelectronics study. Since it can be employed to deposit films on large substrates, the plasma polymer approach should find favor in large area polymer circuitry as long as electric properties of these films satisfy the requirements of gate insulators. This work explores this possibility by evaluation of pulsed RF plasma-deposited polyallylamine insulator films via detailed FTIR, C-V, and I-V characterizations.

EXPERIMENTAL METHOD

In this work, two types of polyallylamine films deposited on Si wafers by RF pulsed plasma polymerization were employed as the dielectric in the metal-polyallylamine-Si MIS structure. All insulator film thicknesses employed were approximately 2000 Å. They were deposited with the same monomer but under two different reactor conditions. Samples PA1 were deposited at room temperature, while samples PA2 underwent an in-situ heat treatment at 100°C during deposition. Both samples used an n-doped (1–10 Ω-cm) Si (100) wafer as the substrate. The substrates were processed through a strict cleaning procedure prior to polymer deposition. First, the surface oxide was removed with diluted hydrofluoric acid, then a base-peroxide ($NH_4OH:H_2O_2$) etch, followed by an acid peroxide ($HCl:H_2O_2$) etch, and finally diluted hydrofluoric acid etching again.

A fairly detailed general description of the pulsed plasma polymerization technique has been presented previously.[14] However, a significant modification in the present study was use of a bell-shaped reactor in lieu of the cylindrical reactors employed previously. The bell-shaped reactor, located inside a temperature-controlled oven enclosure, provided more uniform film thickness on the silicon substrates. A wire mesh, symmetrically placed around the top of the bell jar, served as the ground electrode. A metal plate, located under the bottom glass plate of the reactor, served as the hot electrode. Figure 1 provides an illustration of the reaction system plus associated electrical components employed in this study. Further details on the operation of this system have been provided by Sanchez-Estrada.[15]

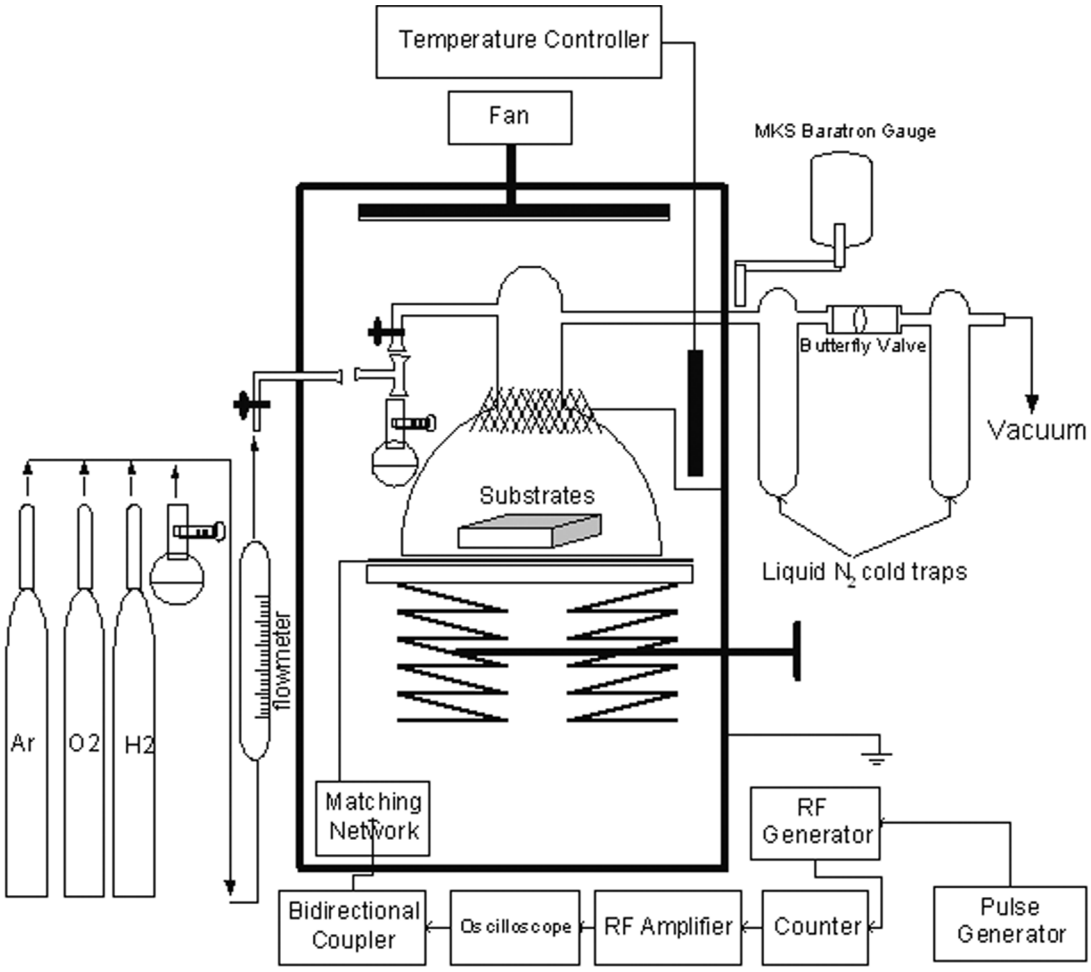

Fig. 1. A schematic of the plasma reactor system and associated electronic components used in this study.

In the present work, plasma on and off times of 3 and 10 ms, respectively, were employed during polymerization of the allylamine monomer. A peak power input of 36 W was employed during the plasma on periods. The monomer was introduced at a flow rate of 3.5 cm^3(STP)/min and the reactor pressure was adjusted to 190 mTorr. Shadow masking through a wire mesh was used to define 180 × 170 μm^2 Ti/Au rectangles atop the MIS capacitors. Backside electrical contacts were made by e-beam evaporation of Ti/Au on the back of the Si wafer. The Ti/Au metal thickness was 150 Å/1000 Å. The Ti adheres to Si better than Au, so a thin layer is added to promote adhesion.

Capacitance and conductance measurements have been carried out with an Agilent 4284A LCR meter coupled with MDC (Material Development Corporation, Chatsworth, CA) CSM/Win analysis software.[16] A family of C-V curves were measured at five different frequencies between 100 Hz and 1 MHz. Hysteresis behavior has only been demonstrated at a frequency of 1 MHz. The relation between interface trap density–bandgap energy and surface potential-voltage was calculated from the C-V data also at 1 MHz with the gate voltage sweeping –40 V to 20 V. Leakage current (I-V) curves were measured with an Agilent (Palo Alto, CA) 4156 semiconductor parameter analyzer.

RESULTS AND DISCUSSION

Figure 2 shows the FT-IR spectrum of a polyallylamine film deposited under the 3 ms on, 10 ms off duty cycle. This transmittance spectrum was recorded for a film deposited on a polished KBr disc. An important aspect of this spectrum is the large absorption peak at ~3400 cm^{-1} indicative of the presence of $–NH_2$ groups in the polymer film. Efficient retention of monomer functional groups in polymer films deposited under pulsed conditions has been demonstrated to be a consistent feature of time-modulated plasma discharges. For example, polyallylamine films deposited under the same experimental conditions noted above, but with a continuous-wave discharge instead of the pulsed mode, contained a sharply reduced $–NH_2$ group content. More details on the chemical composition and stability of plasma-generated polyallylamine films have recently been published.[17,18]

Figure 3 shows C-V responses for PA1 and PA2. The high-frequency (HF) response for both PA1 and PA2 clearly shows accumulation and depletion regions that are typical in HF Si MOSFET characteristics. For both PA1 and PA2, the capacitance tends to shift to higher values when decreasing the ac voltage frequency, and the flatband voltage is pushed toward the negative end. The condition for flatband is no band bending at the semiconductor/insulator interface. In the ideal case, the flatband condition should be reached at zero dc bias. However, nonideal interfaces allow charges to accumulate at/near the interface, which results in band bending at the interface without an applied external voltage. An external bias is needed to flatten the band bending at the interface. The measured flatband voltage depends not only on the type of charges, but also on the location of the charges within the MIS structure. The phenomenon of higher accumulation capacitance at lower ac frequency had also been reported in other polymers. It is stated in Ref. 19 that the variation in dielectric constant is attributed to the frequency dependence of the polarizable units in a

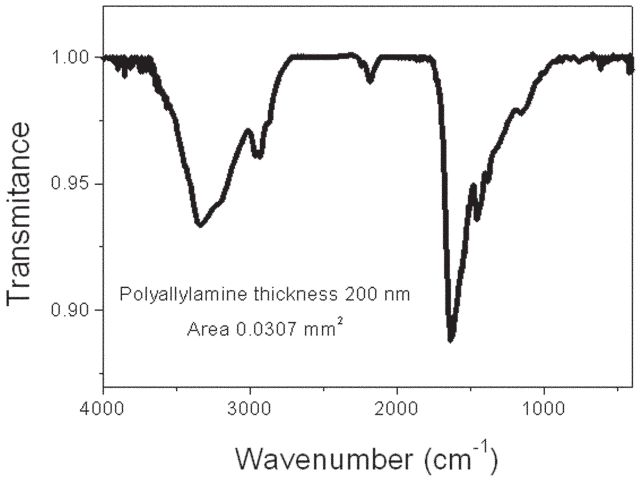

Fig. 2. FT-IR transmittance spectrum of polyallylamine film deposited under pulsed plasma of 3 ms on and 10 ms off.

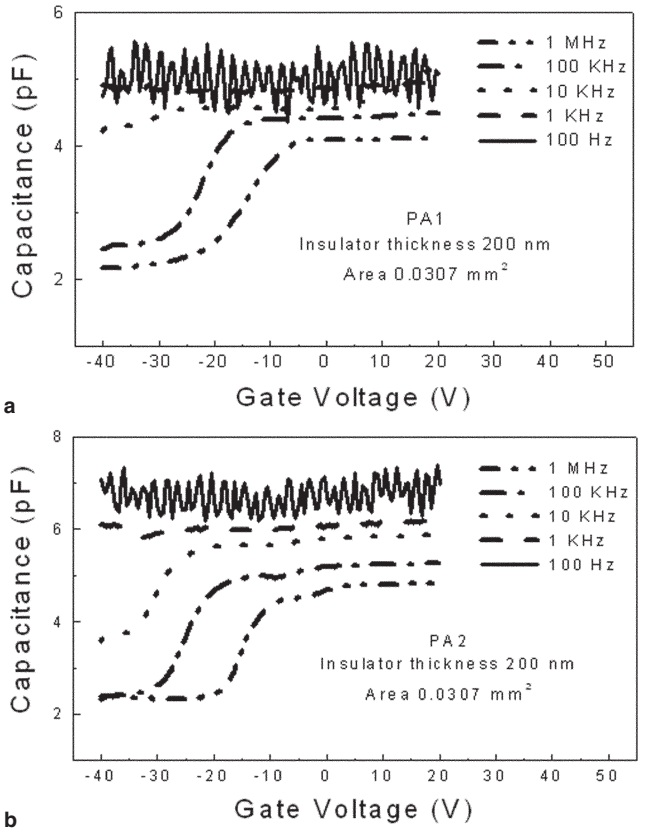

Fig. 3. Multiple-frequency C-V plots for RF pulse plasma-deposited polyallylamine films: (a) A1: sample deposited at room temperature; and (b) PA2: sample deposited at 100°C.

Table I. Materials Parameters for RF Pulse Plasma-Deposited Polyallylamine Films Studied, PA1, Deposited at Room Temperature, and PA2, Deposited at 100°C, That Were Extracted from a C-V Analysis at 1 MHz of the MIS Structures

Parameters	PA1 (No Heat Treatment)	PA2 (In-Situ Heated)
C (pF)	4.12	4.83
k	3.03	3.55
C_{inv} (pF)	2.19	2.33
W_{inv} (μm)	1	1.21
N_{sub} (cm^{-3})	7.48×10^{14}	4.9×10^{14}
C_{fb}/C_{accu}	0.833	0.807
V_{fb} (V)	−12.5	−13.0
V_t (V)	−22.9	−21.6
ϕ_{ms} (V)	0.677	0.666
N_{ss} (cm^{-2})	1.85×10^{12}	2.07×10^{12}

polymer to orient quickly enough with respect to the applied ac signal. There may also be slow states in the insulator and at the interface. They only reveal their effect on measured capacitance at lower frequencies. Depletion and inversion were not observed for frequencies lower than 1 kHz. Since the depletion and inversion regions shift toward more negative dc biases at lower frequencies, it is reasonable that the depletion and inversion regions at low frequency may have been pushed out of the measurement system's scope (−40 V to 40 V). Capacitance measurements at 100 Hz were very noisy because of the interference of room light. The noise effect diminished with an increase in the measurement frequency.

Parameters of the metal-polyallylamine-Si MIS structure extracted from the standard HF (1 MHz) C-V measurements[20] are listed in Table I. The dielectric constants determined from measured C-V characteristics at 1 MHz were 3.03 for PA1 and 3.55 for PA2. PA2, which included an in-situ heat treatment, exhibited a higher dielectric constant, presumably due to densification of the film.

The dielectric constant is calculated, based on the capacitance formula for a parallel plate capacitor, as

$$k_i = \frac{Ct}{\varepsilon_0 A} \tag{1}$$

where k_i is the relative dielectric constant of the insulator, ε_o is the permittivity of vacuum, A is the area of the MIS device, C is the measured accumulation capacitance, and t is the insulator thickness. The inversion capacitance, C_{inv}, measured from the C-V plot, is the series combination of the insulator capacitance, C, and the capacitance of the depletion layer in the substrate, C_{dpl}:

$$\frac{1}{C_{inv}} = \frac{1}{C} + \frac{1}{C_{dpl}} \tag{2}$$

Therefore, the depletion layer width in the substrate, W_{inv}, is computed from the following parallel plate capacitance relation:

$$W_{inv} = \frac{k_i \varepsilon_0 A}{C_{dpl}} \tag{3}$$

With the assumption that doping is constant throughout the depleted substrate region, the bias across the substrate, V, can be expressed in two ways:

$$V = \frac{qNW_{inv}^{\ 2}}{2k_s\varepsilon_0} \tag{4}$$

and

$$V = \frac{2kT \ln\left(\frac{N}{n_i}\right)}{q} \tag{5}$$

The voltages in the previous two expressions can be equated to give the following expression:

$$W_{inv} = \sqrt{\frac{4k_s\varepsilon_0 kT \ln\left(\frac{N}{n_i}\right)}{q^2 N}} \tag{6}$$

where k is the Boltzmann's constant, T is the sample temperature, and n_i is the intrinsic carrier concentration at temperature T. The substrate doping is the only unknown in this transcendental equation and it can easily be found using iterative numerical methods.

The specified resistivity for the Si substrate from the manufacturer was 1–10 Ω-cm. By checking known data of resistivity versus n-type doping concentration for uniformly doped silicon wafers, the doping concentration of the substrate should be between 4×10^{14} and $4 \times 10^{15} cm^{-3}$. Comparing this to the computed doping concentration from the C-V measurements, 7.48×10^{14} cm^{-3} and 4.9×10^{14} cm^{-3} for PA1 and PA2, shows relatively close agreement. This can be treated as proof to the validation of the C-V measurement data and other calculations.

Once the substrate doping is known, the Debye length, L_d, by definition is

$$L_d = \sqrt{\frac{k_s\varepsilon_0 kT}{q^2 N}} \tag{7}$$

The flatband capacitance, C_{fb}, is found from the Debye length:

$$C_{fb} = \frac{k_i\varepsilon_0 A}{t_{ox} + \frac{k_i}{k_s}L_d}. \tag{8}$$

The C-V program then uses C_{fb} and the measured C-V data to find the flatband voltage, V_{fb}, by linear interpolation. The flatband voltage shows a deviation of measured C-V curves from ideal curves because of metal work function differences and charged interface states. After finding the flatband voltage, the total insulator trap density, N_{ss}, may be found by comparing the flatband voltage with the metal-semiconductor work function, Φ_{ms}. The expression is

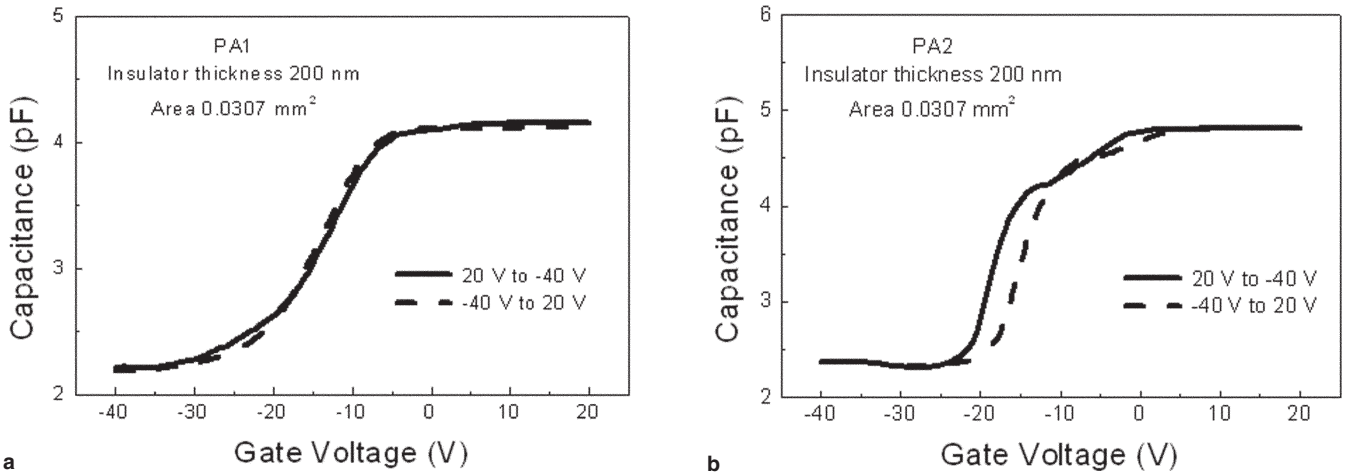

Fig. 4. Hysteresis behavior of RF pulse plasma-deposited polyallylamine films: (a) PA1: sample deposited at room temperature; and (b) PA2: sample deposited at 100°C.

$$N_{ss} = \frac{C(\Phi_{ms} - V_{fb})}{qA}. \quad (9)$$

The hysteresis behavior can be caused by either charge injected into the oxide or mobile charge within the oxide. The hysteresis direction serves as a simple check to discriminate between these two effects. Negative charge injected into the oxide gives rise to a positive flatband voltage shift between $-Vg \rightarrow +Vg$ sweep and $+Vg \rightarrow -Vg$ sweep, while positively charged mobile ions cause a negative shift. PA1 showed hardly any hysteresis while PA2 showed a flatband difference of negative 2.4 V even though the measurement was at room temperature (Fig. 4). Judging from the hysteresis direction criteria, the hysteresis of PA2 is due to mobile ions. For large positive gate voltages, mobile ions drift to the insulator-semiconductor interface. More positive charge at the insulator-semiconductor interface causes a more negative flatband voltage shift. For large negative gate voltages, the mobile charge is attracted to the gate-insulator interface where it does not affect the C-V curve.[12]

The charging and discharging of interface traps gives rise to the measured conductance; thus, the conductance of MIS capacitors depicts the interface trap density. Figure 5 shows the measured conductance curves versus gate voltage for PA1 and PA2 at a frequency of 50 kHz. The frequency of 50 kHz was chosen for highest sensitivity during the conductance measurement.[21] Although the peak conductance position shifts about 5 V, the integrated conductance magnitude remains relatively the same as a further check on the interface trap density to be similar for PA1 and PA2. This study does not include a more detailed analysis using the conductance method proposed by Nicollian and Goetzberger to determine the interface trap density, since this study focuses upon the new polymer dielectric material.[22]

It is observed that the in-situ heat treatment leads to a higher dielectric constant. Both samples went through exactly the same sample preparation,

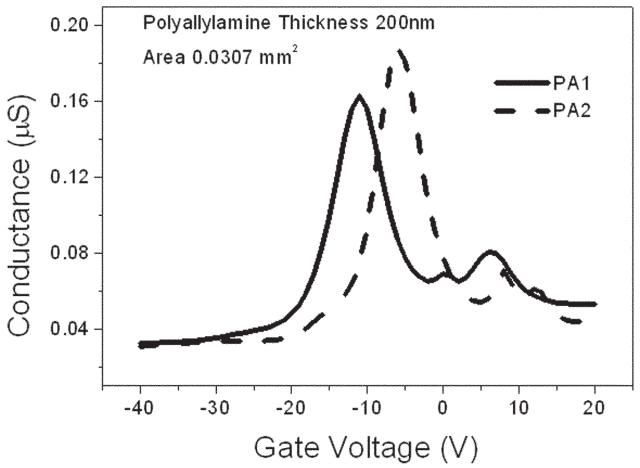

Fig. 5. Conductance versus gate voltage plot at 50 kHz to compare RF pulse plasma-deposited polyallylamine films, PA1, deposited at room temperature, and PA2, deposited at 100°C.

and thus the most likely measured differences are related to the in-situ heat treatment, which occurred under vacuum conditions. The most direct result of this heating is likely a denser structure in sample PA2. It is hard to predict if it is the temperature itself or the denser structure that leads to interface property alternation between PA1 and PA2. High temperature normally anneals the sample and lowers the interface trap density, but 100°C is far too low to effectively anneal the sample.[20] On the other hand, it cannot be ruled out that temperature brings about some other modification to the interface. Further research is needed to discover the impact of in-situ heat treatment on insulator/semiconductor interface.

The interface trap density versus bandgap energy curve examines the trap densities near the polymer-Si interface and can highlight any defects formed by the deposition process (Fig. 6). The interface trap density of PA2 increases more rapidly toward mid bandgap while the curve for PA1 remains lower. Starting from the conduction band edge, PA2 has a

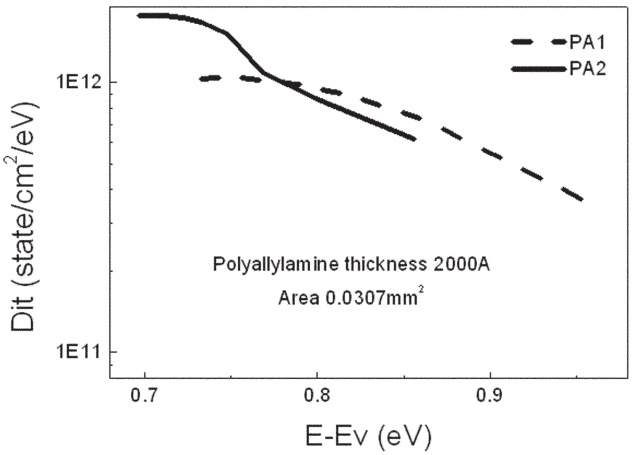

Fig. 6. Calculated interface trap density of RF pulse plasma-deposited polyallylamine films, PA1, deposited at room temperature, and PA2, deposited at 100°C as determined from C-V analysis.

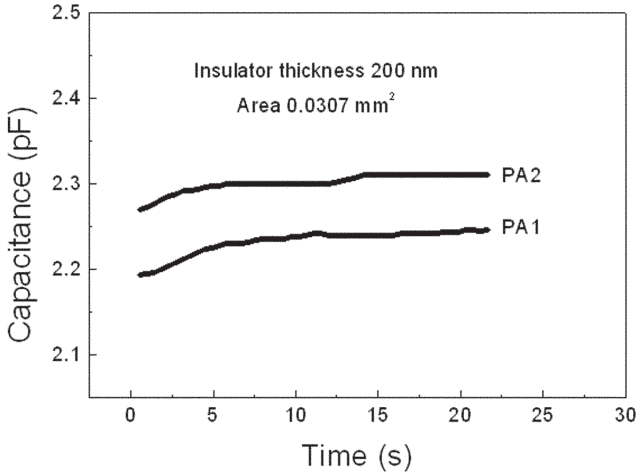

Fig. 7. Capacitance versus time plot of RF pulse plasma-deposited polyallylamine films, PA1, deposited at room temperature, and PA2, deposited at 100°C.

lower initial interface trap, and ends up with a higher number density as the energy approaches mid-bandgap, than PA1. The energy levels of the interface traps can be depicted as more concentrated in a smaller range at the interface of PA2, and that for PA1 is more diffuse. Thermally grown SiO_2 on Si typically generates approximately 10^{11} to 10^{12} states/cm^2-eV interface traps at mid-bandgap.[20] This number decreases to less than 10^{10} states/cm^2-eV after annealing in the presence of hydrogen.[20] Compared to those Si/SiO_2 interface trap density data, the quality of the Si/polyallylamine interface, with an approximately 10^{12} states/cm^2-eV trap density, is reasonable since no precautions were taken under a clean room environment and there was no after growth annealing treatment.

Capacitance changes over time provide an indication of some possible failure mechanisms that involve mobile charges within the polymer insulator that move over time with the application of an applied voltage leading to a memory effect. The amount of mobile charge can be obtained from

$$Q_m = \Delta C \times V \quad (10)$$

The capacitance-time (C-t) response was measured at a gate voltage of 15 V. For the unheated sample PA1, the capacitance change over a time period of 22 sec is 0.05 pF. Knowing that the area of the capacitor is 0.0307 mm^2 and the charge of each carrier is 1.6×10^{19} C, the calculated mobile charge is 1.53×10^{10} cm^{-2}. Compared to the total measured insulator charge of 1.85×10^{12} cm^{-2}, the mobile charge determined from the capacitance-time method contributes less than 1% to the total insulator charge. By performing the same calculation for PA2, a value of 1.22×10^{10} cm^{-2} is obtained. This number is also less than 1% of the total insulator charge for the unheated sample. Since the mobile charge occupies less than 1% in the total insulator trapped charges, the majority of the charges detected in the C-V measurement are mainly fixed charge. However, this result should be interpreted with caution. The C-t measurement was conducted at room temperature, while some mobile charges may only move at slightly elevated temperatures. Another concern arises from the comparison between the number of charges in polyallylamine and that in conventional thermally grown SiO_2. The number of mobile and other trapped charges within the insulator will likely drop if the plasma deposition is performed in a cleanroom environment. Although some mobile charge is evident from C-t analysis, the data indicate mobile charge is not a major concern at room temperature due to the relatively flat responses over time (Figure 7).

Leakage current versus gate voltage measurements determine the amount of current able to conduct vertically through the MIS capacitor. A small leakage current implies the polymer layers contain few electrically active defect centers and virtually no pinholes. Both samples showed leakage currents below 20 fA up to 100 V bias, resulting in a leakage current density of 6.51×10^{-11} A/cm^2 at an electric field strength of 5 MV/cm for a 200-nm-thick film. The leakage current density of thermally grown SiO_2 at 5 MV is about 10^{-9} A/cm^2 for a 100-nm-thick oxide,[23] which is more than 10 times higher than that of RF pulsed plasma polyallylamine. This is an extremely small leakage current and clearly shows the electrical integrity of PPP polyallylamine films. No electrical breakdown in either PA1 or PA2 was observed up to the measurement limitation of a 100 V applied gate voltage. This data indicate that the breakdown of the electric field must exceed 5 MV/cm.

CONCLUSIONS

Metal-insulator-semiconductor capacitors have been fabricated using pulsed RF plasma polymerized allylamine as the insulator. Both C-V and I-V measurements indicate that the polymerized allylamine films have a very high breakdown field of $>5 \times 10^6$ V/cm. The two samples, PA1 with no heat

treatment and PA2 deposited at 100°C, have measured dielectric constants of 3.03 and 3.55, respectively. Further, in-situ heat treatment appears to elevate the dielectric constant. The high performance of polyallylamine films (good dielectric constant and high breakdown field) makes it a promising insulator for future all-polymer circuits.

REFERENCES

1. M. Aguilar-Frutis, M. Garcia, and C. Falcony, *Appl. Phys. Lett.* 72, 1700 (1998).
2. D. Park, H. Cho, K. Lim, C. Lim, I. Yeo, J. Roh, and J. Park, *J. Appl. Phys.* 89, 6275 (2001).
3. D. Park, K. Lim, H. Cho, J. Kim, J. Yang, J. Ko, I. Yeo, J. Park, H. Waard, and M. Tuominen, *J. Appl. Phys.* 91, 65 (2002).
4. H. Shirakawa, E.J. Louis, A.G. MacDiarmid, C.K. Chiang, and A.J. Heeger, *J. Chem. Soc. Chem. Comm.* 579 (1977).
5. F. Garnier, R. Hajlaoui, A. Yasar, and P. Srivastava, *Science* 265, 1684 (1994).
6. C.J. Drury, C.M.J. Mutsaers, C.M. Hart, M. Matters, and D.M. de Leeuw, *Appl. Phys. Lett.* 73, 108 (1998).
7. H. Sirringhaus, T. Kawase, R.H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E.P. Woo, *Science* 290, 2123 (2000).
8. T. Kawase, H. Sirringhaus, R. Friend, and T. Shimoda, *Adv. Mater.* 13, 1601 (2001).
9. K.S. Narayan and N. Kumar, *Appl. Phys. Lett.* 79, 1891 (2001).
10. H. Yasuda, *Plasma Polymerization* (Orlando, FL: Academic Press, 1985).
11. L.M. Han, R.B. Timmons, W.W. Lee, Y. Chen, and Z. Hu, *J. Appl. Phys.* 84, 439 (1998).
12. D.K. Schroder, *Semiconductor Material and Device Characterization* (New York: Wiley, 1998), pp.41–58.
13. S. Scheinert, G. Paasch, S. Pohlmann, H. Horhold, and R. Stockmann, *Solid-State Electron.* 44, 845 (2000).
14. V. Panchalingam, X. Chen, C.R. Savage, R.B. Timmons, and R.C. Eberhart, *J. Appl. Polym. Sci., Appl. Polym. Symp.* 54, 123 (1994).
15. F.S. Sanchez-Estrada (Ph.D. Thesis, University of Texas at Arlington, 2002).
16. B. Gordon, *Semiconductor Measurement System, Model CSM/Win, Operator's Manual* (Chatsworth, CA: Materials Development Corporation, 1996).
17. H. Schoenherr, M.T. van Os, R. Foerch, R.B. Timmons, W. Knoll, and G.J. Vancso, *Chem. Mater.* 12, 3689 (2000).
18. J.G. Calderon, A. Harsch, G.W. Gross, and R.B. Timmons, *J. Biomed. Mater. Res.* 42, 597 (1998).
19. J.O. Simpson and A.K. St.Clair, *Thin Solid Films* 308, 480 (1997).
20. R.F. Pierret, *Semiconductor Device Fundamentals* (New York: Addison-Wesley Publishing Company), 1996, pp. 584–586, 665–667.
21. E.H. Nicollian and J.R. Brews, *Metal Oxide Semiconductor Physics and Technology* (New York: Wiley-Interscience, 1982).
22. E.H. Nicollian and A. Goetzberger, *Bell System Technol. J.* 46, 1055 (1967).
23. C. Yeh, T. Chen, C. Fan, and J. Kao, *J. Appl. Phys*. 83, 1107 (1998).