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High electric-field effects on short-channel polythiophene polymer field-effect transistors

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The field-effect mobility (FEM) in polythiophene (PT) polymer field-effect transistors (PFETs) increases with reduced channel lengths during high driving forces across the source and drain, which is contradictory to the decrease in mobility caused by short-channel effects in amorphous Si thin-film transistors. The longitudinal electric-field (across source and drain) dependence of the FE mobility is believed to create the rise in mobility once the longitudinal electric field exceeds a critical value of 10^5 V/cm. The high longitudinal electric field also modulates the influence of the gate bias upon the FEM in PT PFETs. With increased longitudinal electric field, the correlation between FEM and gate bias is largely enhanced. © *2004 American Institute of Physics.*
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INTRODUCTION

Polymer field-effect transistors (PFETs) have received tremendous attention lately for their potential application in flexible displays and foldable logic using solution-processible polymers. Vacuum-deposited oligomers are a second type of organic semiconductor that has been implemented as organic FETs (OFETs). High channel mobilities have been demonstrated up to 1 $cm^2/V\,s$ for pentacene OFETs by vacuum deposition of single-crystal active layers, sacrificing flexibility for rigidity.[1–3] Even though reported channel mobility of PFETs is one order of magnitude lower than that of crystalline pentacene, solution-processible polymers are drawing further interest for their potential to scale up to cheap reel-to-reel batch processing.[4–6] The advantage of solution processibility makes semiconducting polymer electronics attractive for large-area and low-cost applications. Research on PFETs has caught up quickly, even though the first OFETs were based on sublimed oligomer electroactive materials. Already PFETs have been monolithically integrated with polymer light-emitting diodes (PLEDs) as drivers.[7,8]

The FE mobility (FEM) is the central figure-of-merit for overall current drive capability. Unlike inorganic thin-film transistors (TFTs), the drift mobility in OFETs are gate and source/drain (S/D) bias dependent. It was reported in 1995 that in vacuum-evaporated oligothiophene FETs, the FE mobility depended upon longitudinal electric fields across the source and drain when the field exceeds 10^5 V/cm.[9] Later work described a gate-voltage-dependent mobility in oligomer and polymer FETs.[10,11] The dependence of FEM on gate voltage in highly ordered OFETs is not the same as for amorphous OFETs. Experimental results showed that the FEM was quasilinearly dependent on gate bias in sublimated oligothiophene FETs.[10] On the other hand, a theoretical study found that in amorphous OFETs, the gate-voltage dependence followed a power law, and good agreement between theory and experiment data was obtained in amorphous polythienylene vinylene and pentacene.[11] In this article, we examine the mobility variation with channel length in poly(thiophene-2,5-diyl) (PT) PFETs. It is unexpected that higher mobility is obtained with shorter channel lengths and at high S/D voltages, which is opposite to the trend in amorphous Si TFTs,[12,13] due probably to the electric-field dependence of mobility in organic semiconductors. For higher $|V_{DS}|$ or lower channel length, the superlinear trend in gate bias dependence of mobility becomes obvious. Since the PT used in this study is noncrystalline, the relationship between mobility and gate bias is expected to follow the power law.

EXPERIMENTAL METHOD

In this work, PFETs with channel lengths ranging from 7 μm down to 1 μm in 1 μm decrements have been fabricated in a coplanar configuration. The active channel is composed of the conducting polymer, PT. As sketched in Fig. 1, a layer of SiO_2 with a thickness of about 1 μm has been thermally grown on a piece of Si substrate. This layer of SiO_2 provides electrical isolation between the Si wafer substrate and the rest of the PFET structure. In most published work, the conductive Si wafer serves the dual function of a supporting substrate and the gate at the same time. The function of the Si substrate is different in this experiment where the Si wafer is capped with an insulator, so that a metal gate can be deposited onto it. Although doped Si is quite conductive, its conductivity is still a few orders of magnitude lower than that of metal. Using a metal gate can minimize the power dissipated within the gate material itself. A gate metal (Ti/Au) was electron-beam evaporated on top of the thermally grown SiO_2 layer, which isolates the Si substrate and the PFET structure. With the PFET structure in this study, the substrate can be glass, or even plastic which is the preferred substrate material for flexible electronics. The Si wafer is used only as the support substrate in this experiment. Due to the device configuration of our PFET design, the gate insu-

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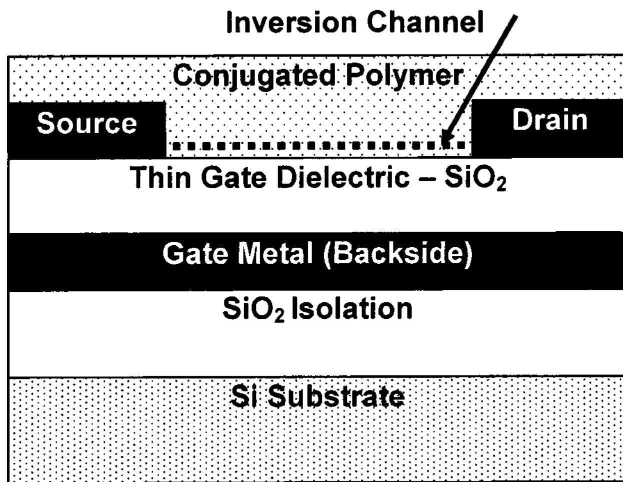

FIG. 1. Schematic of the upside-down PFET structure with an underlying metal gate used in this study.

lator needs to be deposited on top of the gate metal instead of Si, which prevents the use of thermally grown SiO_2. To solve this problem, a SiO_2 gate dielectric was electron-beam evaporated. The thickness of the gate dielectric was 2500 Å. The tradeoff is that e-beam SiO_2 does not have as a high breakdown voltage as thermally grown SiO_2, but it is effective enough as a gate insulator here. Interdigitated source and drain electrodes were defined by standard lift-off photolithography. The PFETs had multiple S/D spacings leading to multiple channels, and each channel was 75 μm wide. Interdigitated configurations are widely used in power transistors to handle large currents generated due to the large gate-width/length (W/L) ratio. One of the intended applications of PFETs is to drive PLEDs, which requires an output current on the order of milliamperes. The interdigitated configuration is a good choice for high driving power capability. The size of the PFETs is denoted by $W\times(L\times n)$ where W is the gate width, L is the gate length, and n is the number of channels. After source and drain contact metal lift-off, the commercial grade PT was applied in solution form (about 0.5% in the solvent xylene) by spin coating at 4000 rpm for 30 s. The PT solution was filtered with a 1 μm pore size to reduce impurity concentrations. The PT PFETs were characterized with an Agilent HP 4156 parameter analyzer using a Cascade probe station.

RESULT AND DISCUSSION

The $I_{DS}-V_{DS}$ characteristics were determined with applied drain–source voltage ranging from 0 to -40 V with gate biases varying from 0 to -16 V. The test results showed a slight deviation in the $I_{DS}-V_{DS}$ relationships from the expected ideal case. For devices with channel lengths above 3 μm, I_{DS} demonstrates reasonable saturation. Figure 2 shows the gradual loss of saturation as channel lengths are reduced from 7 to 1 μm in 1 μm decrements. Similar behavior was observed in oligothiophene OFETs and short-channel (SC) effects cause the deviation.[9] SC effects were also described in amorphous Si TFTs.[12–14] The effect of decreasing channel lengths on I_{DS} saturation is observed in Si TFTs, oligomer TFTs, and polymer TFTs, which implies that the channel-length effect on I_{DS} saturation is device structure rather than semiconductor material related. The PT PFETs studied here can also operate in depletion mode, as in the PFETs based on poly(3-hexylthiophene).[6] The PT PFETs require at least 20 V gate bias to completely turn the channel off, due probably to charged residual impurities in the commercial polymer (Fig. 3).

To compare the different sized PFETs, the measured current I_{DS} was normalized, defined as I_{DS}/n, with n being the corresponding number of multiple channels per PFET structure. Figure 4 shows an increase in the normalized I_{DS} with decreasing channel length. This can be explained by the reduction in channel resistance with decreasing channel length. As the gate voltage decreases, the normalized I_{DS} drops for the increased channel resistance. However, this observation is opposite for amorphous Si TFTs. The reduction in drain current with decreasing channel length in amorphous Si TFTs was due to the increased role of parasitic resistance compared to the intrinsic channel resistance at low dimensionality.[12] The parasitic resistance decreases with increased S/D to gate overlap.[12] In the oligothiophene FET study by Torsi *et al.*, who also used an unpatterned gate, similar to this work, it was found that the parasitic resistance is more than ten times lower than the total resistance of the device due to a very large S/D to gate overlap.[9] Therefore, the role of the parasitic resistance should be less sensitive to the change in channel length if the parasitic resistance is low while the channel resistance is high, which is true for semiconductor polymers. This reasoning could explain the increased drain current in PFETs but decreased current in amorphous Si TFTs when channel lengths are shorter.

The channel mobility is extracted from I_{DS} versus V_{DS} plot at varying V_{DS}. When $|V_{DS}|<20\,\mathrm{V}$, the PT PFETs with all seven sizes exhibit linear behavior. The channel mobility is calculated for each channel length from the linear equation

$$\mu=I_{DS}L/C_{ox}WV_{DS}(V_{GS}-V_{th}-V_{DS}/2). \qquad (1)$$

Once $|V_{DS}|$ is increased to over 20 V, the larger channel transistors enter the saturation region. At $V_{DS}=-40\,\mathrm{V}$, all PT PFETs with channel lengths greater than 3 μm achieve I_{DS} saturation. For these cases only, the channel mobility is calculated from the saturation equation

$$\mu=2I_{DS}L/C_{ox}W(V_{GS}-V_{th})^2. \qquad (2)$$

The data at $V_{DS}=-10\,\mathrm{V}$, -20 V, and -40 V are used to calculate PT PFET channel mobility, as just discussed, and the results are summarized in Fig. 5. The mobility of 1 μm PT PFETs shows the lowest value at $V_{DS}=-10\,\mathrm{V}$, whereas the mobility of other sizes are slightly higher and similar [Fig. 5(a)]. The intrinsic semiconductor material is likely the major cause of the observed differences. Doped Si has a much higher conductivity than semiconducting polymers, so that a PT channel must have a much higher total resistance than an amorphous Si channel. Since the channel resistance is already so high, the effect of contact resistance is likely masked. Previous Si TFT work showed that by getting rid of the S/D series resistance, the apparent FEM was independent of channel length.[13,15] However, the high polymer resistance

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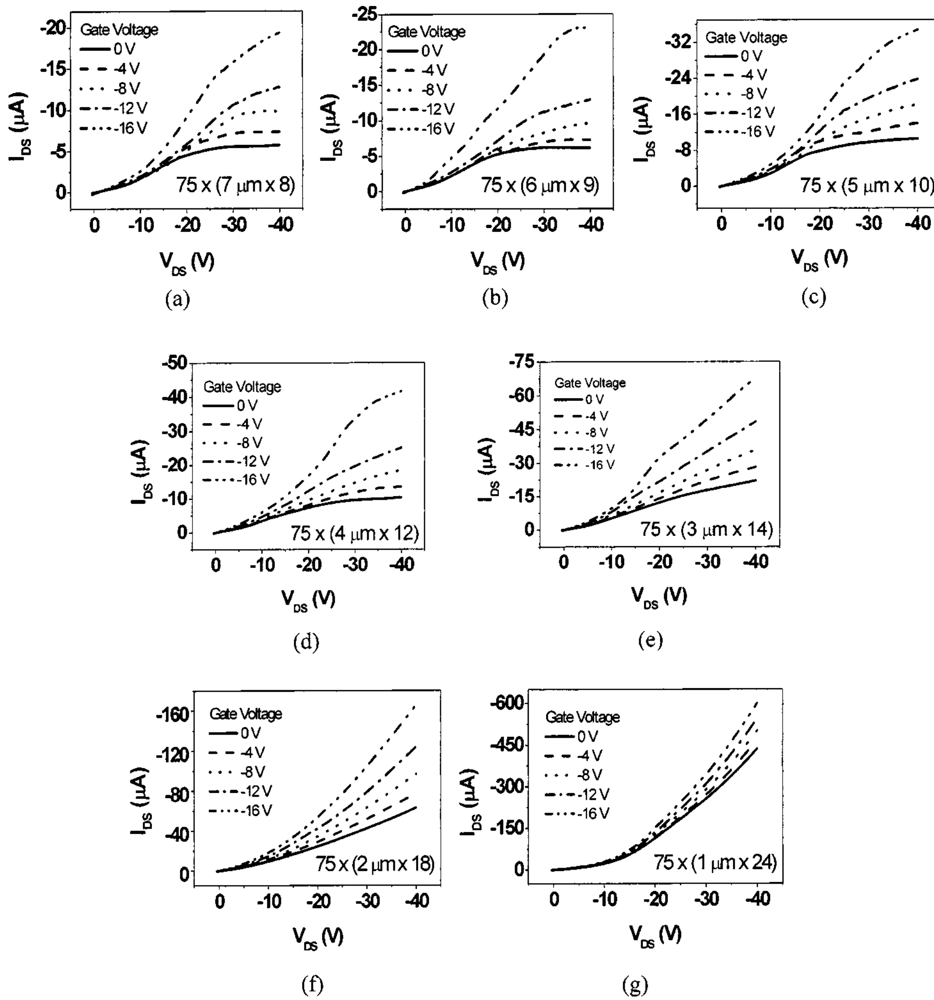

FIG. 2. Measured $I_{DS}-V_{DS}$ curves for V_{DS} up to -40 V and V_{GS} up to -16 V with channel lengths varied from (a) 7 μm to (g) 1 μm.

only reduces the effect of S/D series resistance, rather than eliminating the effect. The PFETs with 5, 6, and 7 μm channel lengths exhibit higher extracted mobilities than smaller gate lengths. This result is consistent with previous results in amorphous Si TFTs.[12] Reduced channel lengths lower mobilities because the S/D contact series resistance has a larger effect on SC devices. At $V_{DS}=-20$ V, the extracted channel mobility for PT PFETs with channel lengths 2, 3, and 4 μm still remains lower than with channel lengths 5, 6, or 7 μm. However, the channel mobility of 1 μm PFETs is no longer the smallest. It rises to a commensurate level with larger channel lengths [Fig. 5(b)]. The extracted channel mobility at high V_{DS} (-40 V) continues this trend and is even more contradictory to the previous results in SC amorphous Si TFTs.

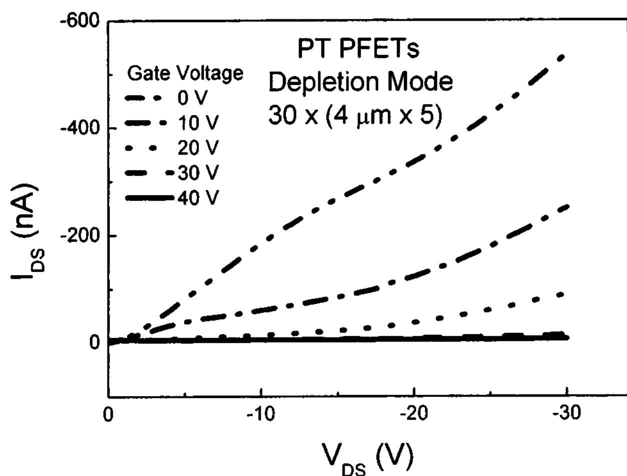

FIG. 3. Measured $I_{DS}-V_{DS}$ curves for polythiophene PFETs operated in depletion mode.

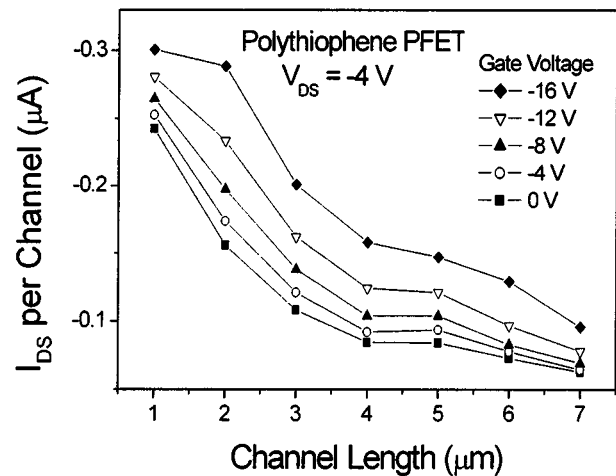

FIG. 4. Extracted I_{DS} per channel for PFETs with various channel lengths L, at different V_{GS} biases.

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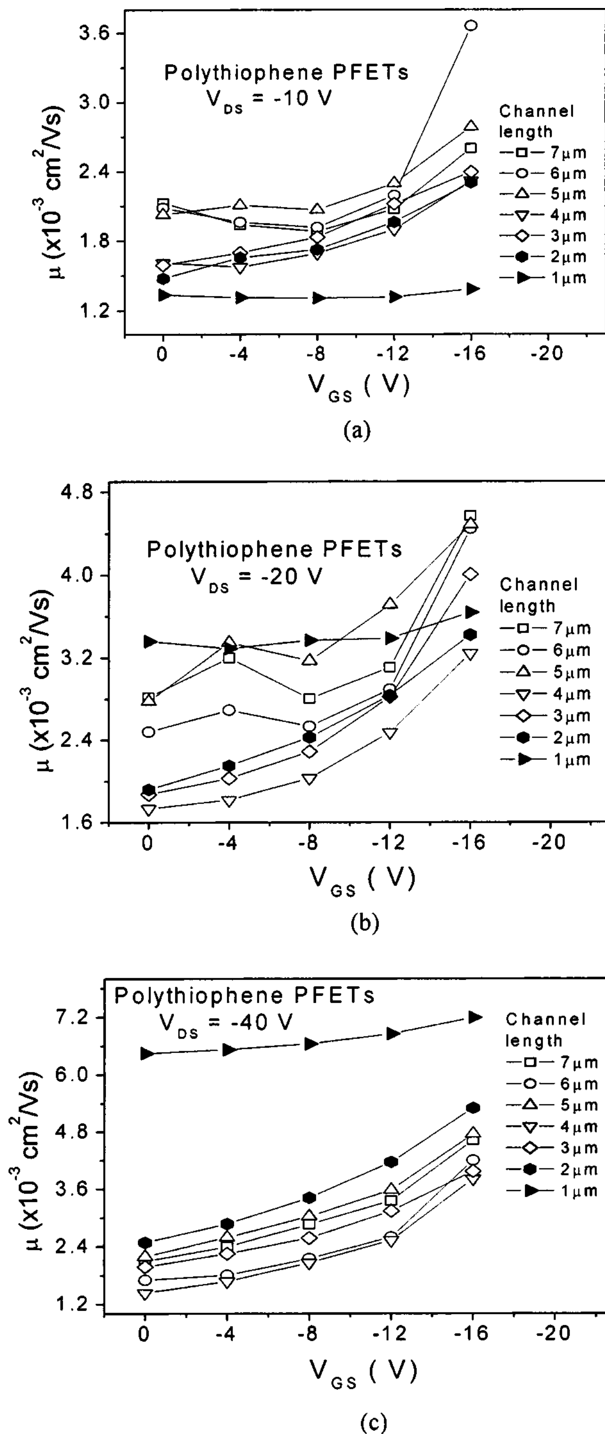

FIG. 5. Calculated channel mobility dependence on gate bias at various V_{DS} biases for PFETs with different channel lengths. (a) $V_{DS} = -10$ V, (b) $V_{DS} = -20$ V, and (c) $V_{DS} = -30$ V.

As illustrated in Fig. 5(c), the PFETs with 1 μm channel lengths now have the highest extracted channel mobility, which is above the mobilities for longer channel PFETs. In addition, at this drain bias, PFETs with 2 μm channel length have the second highest extracted mobility. However, the extracted channel mobilities of the remaining sized PFETs are closely spaced and indistinguishable.

Based on the comparisons shown in Figs. 5(a), 5(b), and 5(c), it is clear that some factor other than S/D resistance is influencing the mobility dependence on channel length in PFETs. This factor becomes stronger as $|V_{DS}|$ increases and surpasses any SC effects eventually. The high intrinsic resistance of polymers can weaken the effect of S/D contact resistance to some extent, but it is difficult to completely cancel the contact resistance effect. The intrinsic resistance of polymers is also not likely to change with V_{DS} at a set gate bias. However, the longitudinal electric field changes proportional to V_{DS}. It is known that the drift mobility in many organic materials exhibits an electric-field dependence, although the origin of the field-dependent mobility is not quite clear as yet. The drift mobility increases significantly when the longitudinal electric field across source and drain exceeds a critical value of 100 kV/cm.[9] By dividing the applied V_{DS} with the channel length, it is easy to determine that at $V_{DS} = -10$ V, only the PFETs with 1 μm channel lengths are at the edge of this high longitudinal electric field. At $V_{DS} = -20$ V, the 1 μm PFETs measured here have a longitudinal electric field of 200 kV/cm, so their channel mobility is more greatly influenced by this high field than other sized PFETs. The 1 μm PFETs acquire a 400 kV/cm longitudinal electric field at $V_{DS} = -40$ V, and the corresponding 2 μm devices have 200 kV/cm at this bias. The very high longitudinal electric field explains why 1 and 2 μm PT PFETs possess the highest and second highest extracted channel mobility at $V_{DS} = -40$ V, respectively. It is interesting to note that even when the longitudinal electric field is slightly higher than 100 kV/cm, the shortest channel PFETs still have lower channel mobilities than longer channel PFETs. Only when the longitudinal electric field reaches a sufficiently high value ($\geqslant$200 kV/cm) will the mobility of the SC PFETs rise above longer channel PFETs. These results indicate that the increasing longitudinal electric field gradually cancels out and eventually surpasses any SC effects.

Finally, it is observed that the channel mobility can also increase with increasing gate bias. The gate bias dependence of mobility has already been reported in pentacene and a series of oligothiophenes. The gate bias may have the effect of lowering the activation barrier for carrier hopping.[16] An alternative explanation for the gate-voltage dependence of the mobility would be related to the charge concentration, which increases with the gate voltage.[10] As already mentioned in the introduction, for amorphous organic transistors, the gate bias dependence of mobility follows a power law $\mu_{FE} = \alpha V_G^{\beta}$, and the expressions for constant α and exponent β can be found in Ref. 11. The semiconductor layer in this work was an amorphous PT film spin coated from solution, and the mobility data obtained fits a power law. However, the degree of fitting seems to be different for PFETs with varying S/D bias (V_{DS}) and channel lengths. It appears that at higher $|V_{DS}|$, the channel mobility is more sensitive to the gate bias and therefore their extracted channel mobility fits the power law theory more clearly. In other words, the mobility becomes more strongly gate bias dependent with increasing longitudinal electric field. Therefore, this work illustrates that the longitudinal electric field also modulates the dependence of channel mobility on gate bias.

By fitting the mobility and gate bias data into a power law, the exponent, which is related to the operating tempera-

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ture and activation energy for carriers to hop according to Ref. 11, can be obtained. A threshold voltage is included in the fitting process to justify the factor that when $V_{GS}=0$ V, the FETs are actually on. The threshold voltage was determined by plotting the square root of the saturation current of $I_{DS}^{1/2}$ versus V_{GS}. An average threshold voltage of 68 V is obtained and used in the power-law fitting. Since the whole process of sample preparation and characterization was in ambient and no surface passivition was employed, the PT PFETs in this experiment had a relatively high threshold voltage. However, the high value does not affect its validity in power-law-fitting calculation. Only when $V_{DS}=-40$ V are trends for all seven mobility curves clear, so that power-law fitting is performed with only this data. The exponents for the 1 to 7 μm PFETs obtained by power law fitting are 0.007, 0.047, 0.043, 0.059, 0.047, and 0.054, respectively. No trends are found between the power-law exponent and channel length, at least among these available exponents. It is not surprising because the exponent is related to the device operating temperature and carrier activation energy. Higher current densities at smaller channel lengths do cause some localized heating in the device, but there exist too many unknowns to evaluate the importance of local heating to the exponent value. It is hard to define the relationship between the activation energy and channel length or longitudinal electric field at this point, but by observation it is very clear that a high longitudinal electric field enhances the correlation between FEM and gate bias for amorphous organic transistors.

CONCLUSION

In conclusion, this work presents some unique features of PT PFETs with short-channel lengths at high electric fields. Due to the high longitudinal electric field, the field-effect mobility can increase rather than drop at SC lengths due to SC effects. Nevertheless, short channel effects do result in the lack of I_{DS} saturation in PT PFETs with channel lengths lower than 3 μm. The relationship between FEM and gate bias follows a power law in amorphous PFETs. A final discovery in this study is that the high longitudinal electric field enhances the dependence of FEM on gate bias.

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